Low Power Variable Latency Multiplier With Ah Logic

V.SRIKANTH

B.SUDARSHAN

ABSTRACT: Low power design has been an important part in VLSI system design. Digital multipliers are most critical functional units ofdigital filters. The overall performance of digital filters depends on the throughput of multiplier design. Aging problem of transistorshas a significant effect on performance of these systems and in long term, the system may fail due to delay problems. Aging effect can bereduced by using over-design approaches, but these approaches leads to area, power inefficiency. Moreover, timing violations occurwhen fixed latency designs are used. Hence to reduce timing violations and to ensure reliable operation under aging effect, low powervariable latency multiplier with adaptive hold logic is used. This multiplier design can be applied to digital filter so as to enhance itsperformance. The VHDL language is used for coding, synthesis was done by using Xilinx ISE.

(1)INTRODUCTION

Filters are widely used in signal processing andcommunication systems. Digital finite impulse response(FIR) filters are the basic building block of many digitalsignal processing systems. In signal processing, the functionof a filter is to remove unwanted parts of the signal, such asrandom noise, or to extract useful parts of the signal, such asthe components lying within a certain frequency range. Themain objectives of digital FIR filter are to filter outundesirable parts of the signal, shape the spectrum ofsignals in communication channels, signal detection oranalysis in radar applications.An analog filter uses analog electronic circuits made up fromcomponents such as resistors, capacitors and op-amps toproduce the required filtering effect. Such filter circuits arewidely used in such applications as noise reduction, videosignal enhancement, graphic equalizers in hi-fi systems, andmany other areas. A digital filter uses a digital processorto perform numerical calculations on sampled values of thesignal. The processor may be a general-purpose computer, ora specialized DSP (Digital Signal Processor) chip. Digitalfilters are more advantageous when compared with analogones. Digital filters are easily designed, tested andimplemented on a general-purpose computer or workstation.Multiplication is an essential arithmetic operation forcommon DSP

applications, such as filtering and fastFourier transform (FFT). To achieve high execution speed,parallel array multipliers are widely used. These multiplierstend to consume most of the power in DSP computations,and thus power-efficient multipliers are very important forthe design of low-power DSP systems. The throughput ofdigital filter systems depends on these multipliers, and if themultipliers are too slow, the performance of entire circuitswill be reduced.Furthermore, negative bias temperature instability (NBTI)occurs when a PMOS transistor is under negative bias, resultsin aging effect. Aging effect degrades transistor speed byincrease in threshold voltage, which results in real time delay problems. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. Traditional methods to reduce this aging effect were area and power inefficient [1].

Traditional circuits are based on fixed latency design. Infixed latency design, critical path delay as the overall circuit clock cycle in order to perform correctly. However, the probability that the critical paths are activated is low. For these noncritical paths, using the critical path delay as the overall cycle period will result in significant timing waste. Hence, the variable-latency design was proposed to re- duce the timing waste of traditional circuits. In variable-latency design, shortest paths are assigned to be executed within one cycle and longest paths within two or more cycle. When shorter paths are activated frequently, the average latency of variable-latency designs is better than that of fixed latency designs [1].

Main objective of the work is to design a digital filter usinglow power variable latency multiplier with AH logic. Low power variable latency multiplier is designed so as to ensure minimum performance degradation. The coding can be synthesized by the Xilinx ISE Design Suite.

(2). Methodology

Performance of digital filters depends on throughput ofmultipliers. The primary objective is power reduction withsmall area and delay overhead. Low power Variable latencymultiplier design with AH logic introduces a multiplier, inwhich AHL circuit associated with it adjusts the circuit whentiming delays occurs so as to ensure minimum performancedegradation.

2.1 Low Power Variable Latency Multiplier With AH Logic

The basic block diagram for low power variable latencymultiplier with AH logic is shown in Figure 1, whichincludes two m-bit inputs (m is a positive number), one 2mbitoutput, one column-bypassing multiplier, 2m 1-bit Razorflip- flops, and an AHL circuit. Clock is provided by theAND gate at the input.

The overall working of variable latency multiplier is asfollows: when input patterns arrive, the column-bypassingmultiplier and the AHL circuit execute simultaneously.Depending on the number of zeros in the multiplicand,the AHL circuit decides number of clock cycles required forthe current input pattern. If the input pattern requires twocycles to complete, the AHL will output 0 to disable theclock signal of the input flip-flops. Otherwise, the AHL willoutput 1 for normal operations.
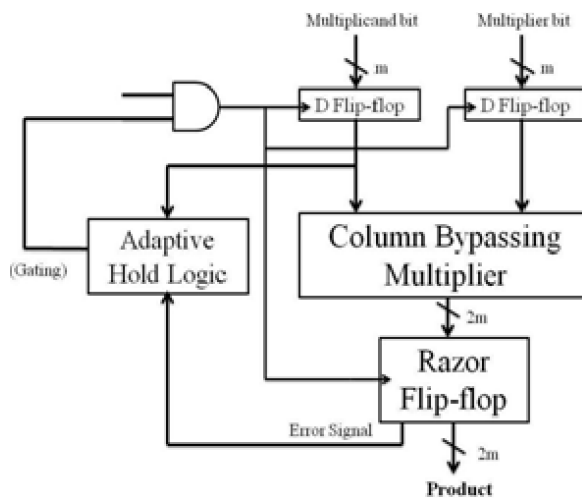

Figure 1: Low Power Variable Latency Multiplier With AHLogic

In this paper, we propose an aging-aware reliable multiplierdesign with novel adaptive hold logic (AHL) circuit. Themultiplier is based on the variable-latency technique and canadjust the AHL circuit to achieve reliable operation underthe influence of NBTI and PBTI effects. To be specific,

thecontributions of this paper are summarized as follows:

1) Novel variable-latency multiplier architecture with anAHL circuit. The AHL circuit can decide whether theinput patterns require one or two cycles and can adjustthe judging criteria to ensure that there is minimum performance degradation after considerable aging occurs;

2) Comprehensive analysis and comparison of the multiplier's performance under different cycle periods to showthe effectiveness of our proposed architecture;

3) An aging-aware reliable multiplier design method that issuitable for large multipliers. Although the experiment is performed in 4- and 16-bit column multipliers, our proposedarchitecture can be easily extended to large designs;

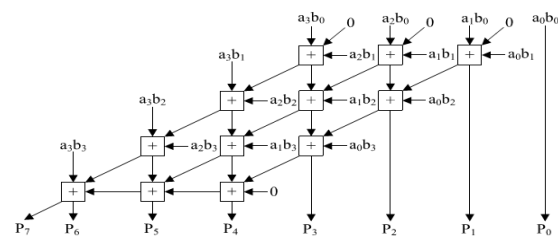**(3)Proposed of Column-Bypassing Multiplier**

Fig. 2. 4×4 normal AM.

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The AM is a fast parallel AM and is shown in Fig. 2. The multiplier array consists of $(n-1)$ rows of carry save adder (CSA), in which each row contains $(n-1)$ full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation. The FAs in the AM are always active regardless of input states. In a low-power column-bypassing multiplier design is proposed in which the FA operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 3 shows a 4×4 column-bypassing multiplier. Supposing the inputs are $1010_2 * 1111_2$, it can be seen that for the FAs in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product $a_i b_i$. Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA.
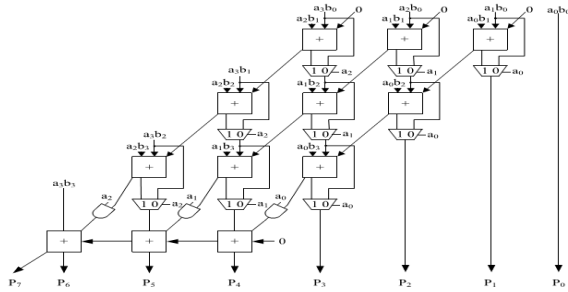
Fig. 3. 4 × 4 column-bypassing multiplier.

Hence, the FA is modified to add two tristate gates andone multiplexer. The multiplicand bit ai can be used as theselector of the multiplexer to decide the output of the FA, andai can also be used as the selector of the tristate gate to turn off the input path of the FA. If ai is 0, the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If ai is 1, the normal sum result is selected. More details for the column-bypassing multiplier can be found.
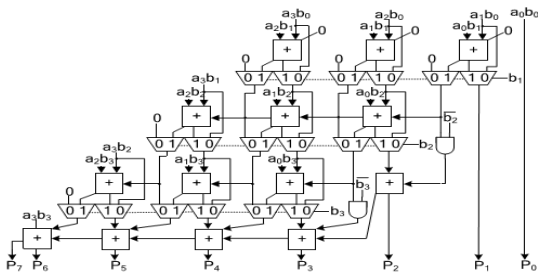
(4) EXTENSION OF ROW MULTIPLIER

Fig. 4. 4 × 4 row-bypassing multiplier.

A low-power row-bypassing multiplier [23] is also proposedto reduce the activity power of the AM. The operation ofthe low-power row-bypassing multiplier is similar to that ofthe low-power column-bypassing multiplier, but the selectorof the multiplexers and the tristate gates use the multiplicator.Fig. 4 is a 4 × 4 row-bypassing multiplier. Each input isconnected to an FA through a tristate gate. When the inputsare 11112 * 10012, the two inputs in the first and second

Rows are 0 for FAs. Because b1 is 0, the multiplexers inthe first row select aib0 as the sum bit and select 0 as thecarry bit. The inputs are bypassed to FAs in the second rows,and the tristate gates turn off the input paths to the FAs.Therefore, no switching activities occur in the first-row FAs;in return, power consumption is reduced. Similarly, because b2is 0, no switching activities will occur in the second-row FAs.However, the FAs must be active in the third

row because theb3 is not zero. More details for the row-bypassing multiplier can also be found.

For example, Fig. 5 is an 8-bit variable-latency ripple carryadder (RCA). A8–A1, B8–B1 is 8-bit inputs, and S8–S1 are
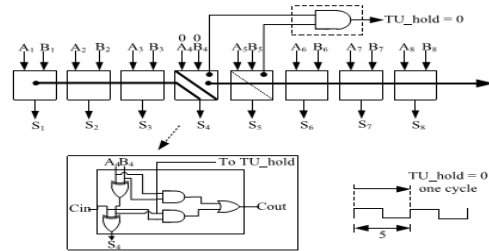

Fig. 5. 8-bit RCA with a hold logic circuit.

(5) RESULTS

The design entry is modeled using VHDL in Xilinx ISE Design with the projectStarter Kit Board, to obtain the synthesis report. The simulation of the design is performed using XILINX 12.1. Structural model of fixed latency multiplier and low power variable latency multiplier with AH logic in Column 4x4, 16x16 is developed. The low power variable latency multiplier with AH logic contains modules such as a column bypassing multiplier, the razor flip-flop and an adaptive hold logic. The simulation results for the bypassing based multipliers are shown in Table 1.

Similarly in the case of delay, variable latency basedmultipliers has less delay when compared with fixed latencyones. Based on the circuit area, power and delay comparison,the 16x16 variable latency based multiplier with AH logic isthe most efficient one and the 4x4 variable latency basedmultiplier with AH logic is the least efficient one. Hence,16x16 variable latency multiplier with AH logic can beapplied to digital FIR filter design so as to enhance itsperformance.
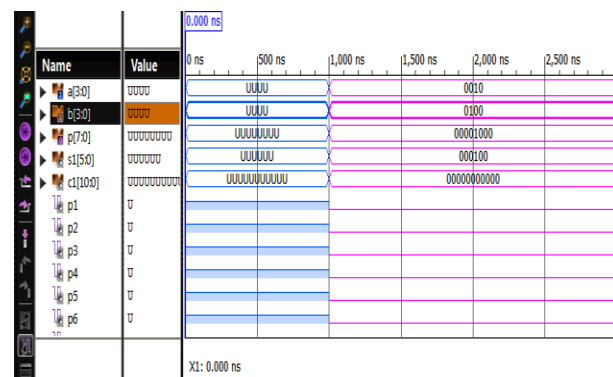
Figure5 Normal 4x4 Multiplier Result
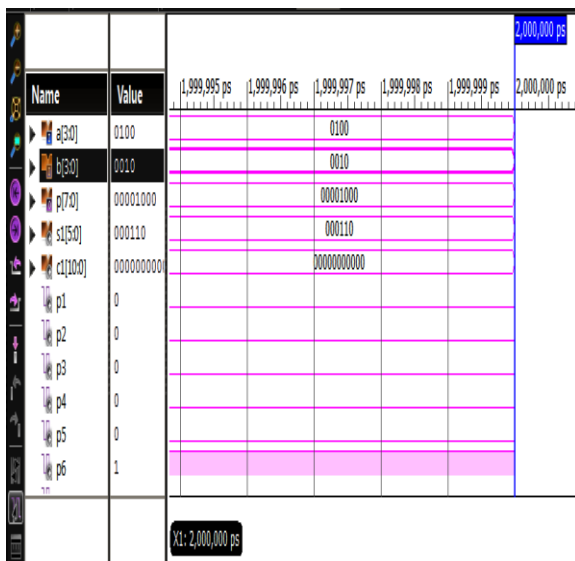

Figure4 Normal 16x16 Multiplier Result

Fig6: column multiplier 4x4 Result
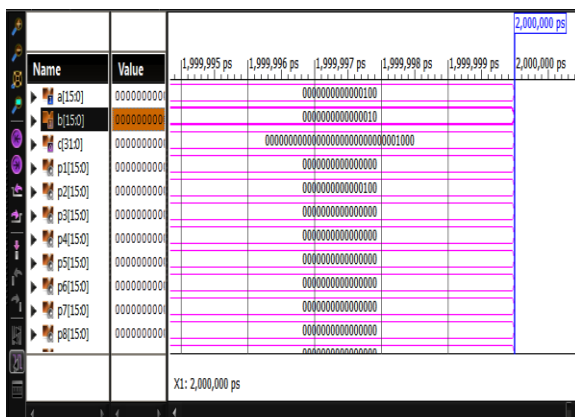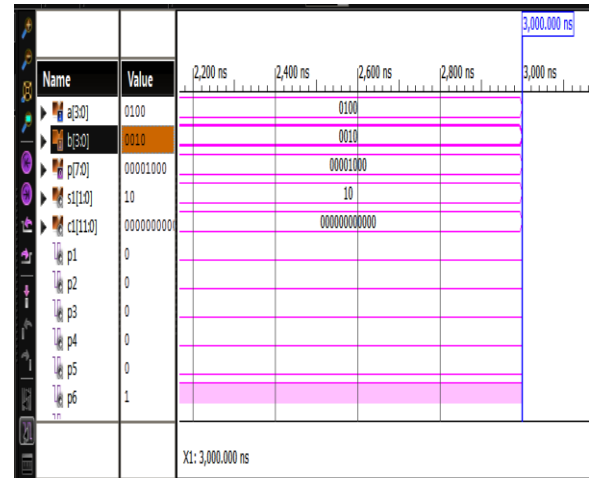

Fig8: column multiplier 16x16 Result

Fig10: row multiplier 4x4 Result

(6) CONCLUSION

Low power utilization is the most important criteria for thehigh performance DSP system. High feat system can beachieved by reducing the dynamic power which in turnreduces the total power dissipation. Low power Variablelatency multiplier design with the adaptive hold logic is ableto adjust the adaptive hold logic to mitigate performancedegradation due to delay problems. Variable-latency designminimizes the timing waste of the noncritical paths. TheRazor flip-flops detect the timing violations and re-executethe operations using two cycles. Variable-latency design canadjust clock cycle required by input patterns to minimizeperformance degradation. And hence variable latencymultipliers have less performance degradation whencompared with traditional fixed latency multipliers, whichneeds to consider the degradation by both the NBTI effectand use the worst case delay as the cycle period. Therefore,performance of digital FIR filters using low power variablelatency multiplier with AH logic, can be enhanced byreduced delay, area and power.

REFERENCES

[1] Ing-Chao Lin, Member, IEEE, Yu-Hung Cho, and YiMing Yang, "Aging-Aware Reliable Multiplier DesignWith Adaptive Hold Logic" IEEE Transactions On VeryLarge Scale Integration (VLSI) Systems.

[2] Prabhu E, Mangalam H, Saranya K, "Design of LowPower Digital FIR Filter based on BypassingMultiplier", International Journal of ComputerApplications (0975 – 8887) Volume 70–No.9, May2013

[3] J.Sudha Rani, D.Ramadevi, B.Santhosh Kmar,JeevanReddy K, "Design of Low Power Column bypassMultiplier using FPGA", IOSR Journal of VLSI andSignal Processing (IOSR-JVSP),Vol.1, Issue 3 (Nov. -Dec. 2012).

[4] Yu-Shih Su, Da-Chung Wang, Shih-Chieh Chang,Member, IEEE, and Malgorzata Marek-Sadowska,"Performance Optimization Using Variable-LatencyDesign Style", IEEE Trans-actions On Very Large ScaleIntegration (VLSI) Systems, Vol. 19, No. 10, October2011.

[5] N.Ravi, Dr.T.S.Rao, Dr.T.J.Prasad," PerformanceEvaluation of Bypassing Array Multiplier withOptimized Design," International Journal of ComputerApplications, Vol. 28, No.5, August 2011

AUTHOR'S DETAILS:

1.V.SRIKANTH M.TECH,VLSI DESIGN

NOVA COLLEGE OF ENGINEERING AND TECHNOLOGY

JAFERGUDA(V),HAYATHNAGAR(M),RANG AREDDY(D)-501512

2014-2016

MAIL ID :SRIKANTHMUDIRAJ073@GMAIL.COM

2.B.SUDARSHAN

DESGNATION: ASSISTANT PROFESSOR

M.TECH

MAIL ID : SUDARSHAN.BANDI@GMAIL.COM