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The Context of an Application Filter System Same for Various Signal Processing

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ABSTRACT:

Over the years, many techniques that exploit the filters' structure and properties to achieve fault tolerance have been proposed. The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in some applications. Digital filters are widely used in signal processing and communication systems. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented. In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost. This new scheme allows more efficient protection when the number of parallel filters is large.

Keywords: Error correction codes (ECCs), filters, and soft errors.

I. INTRODUCTION

A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality. This need is

further increased by the intrinsic reliability challenges of advanced CMOS technologies that include, e.g., manufacturing variations and soft errors [1]. Electronic circuits are increasingly present in and space applications where reliability is critical. In those applications, the circuits have to provide some degree of fault tolerance. To add redundancy, a general technique known as triple modular redundancy (TMR) can be used. The detailed study of the effect of these small errors on the signal to noise ratio at the output of the filter is left for future work. When the circuit to be protected has algorithmic or structural properties, a better option can be to exploit those properties to implement fault tolerance. The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in some applications. One example is signal processing circuits for which specific techniques have been proposed over the years. Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. Most of them have focused on finite-impulse response (FIR) filters. For example, the use of reduced precision replicas was proposed to reduce the cost of implementing modular redundancy in FIR filters. A relationship between the memory elements of an FIR filter and the input sequence was used to detect errors. Other schemes have exploited the FIR properties at a word level to also achieve fault tolerance. Finally, the use of different implementation structures of the FIR filters to correct errors with only one redundant module has also been proposed. The use of residue number systems and arithmetic codes has also been proposed to protect filters. In all the techniques mentioned so far, the protection of a single filter is considered. However, it is increasingly common to find systems in which several filters operate in parallel. This is the case in filter banks and in many modern communication systems. For those systems, the protection of the filters can be addressed at a higher level by considering the parallel filters as the block to be protected. This idea was explored, where two parallel filters with the same response that processed different input signals were considered [2]. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was

obtained. In this brief, a general scheme to protect parallel filters is presented. As parallel filters with the same response that process different input signals are considered. The new approach is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in and ECC code word. This is a generalization of the scheme presented and enables more efficient implementations when the number of parallel filters is large [3]. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules.

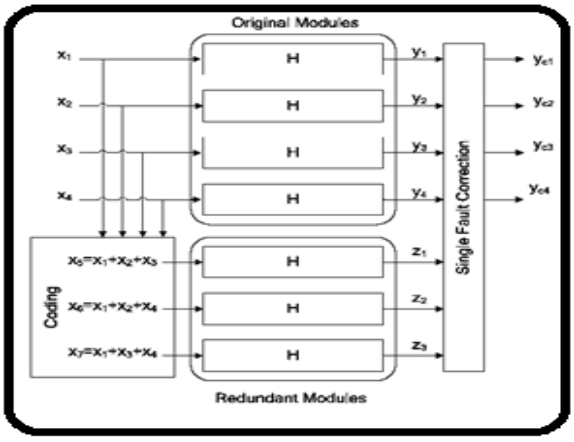

Fig.1.Framework of Filters & Hamming code.

II. PROPOSED SCHEME

The parallel filters are found in some communication systems that use several channels in parallel. In data acquisition and processing applications is also common to filter several signals with the same response. The new technique is based on the use of the ECCs. A simple ECC takes a block of *k* bits and produces a block of *n* bits by adding *n*−*k* parity check bits. The parity check bits are XOR combinations of the *k* data bits. By properly designing those combinations it is possible to detect and correct errors. The data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done byre computing the parity check bits and comparing the results with the values stored. The overall scheme, it can be observed that correction is achieved with only three redundant filters. For the filters, correction is achieved by reconstructing the erroneous outputs using the rest of the data and check outputs. It is important to note that due to different finite precision effects in the original and check filter implementations, the comparisons can show small differences [4]. Those differences will depend on the quantization effects in the filter implementations that have been widely studied for different filter structures. Therefore, a threshold must be used in the comparisons so that values smaller than the threshold are classified as 0.

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This means that small errors may not be corrected. This will not be an issue in most cases as small errors are acceptable. The detailed study of the effect of these small errors on the signal to noise ratio at the output of the filter is left for future work. In the discussion, so far the effect of errors affecting the encoding and decoding logic has not been considered. The encoder and decoder include several additions and subtractions and therefore the possibility of errors affecting them cannot be neglected. The final correction elements such as that need to be tripled to ensure that they do not propagate errors to the outputs. However, as their complexity is small compared with that of the filters, the impact on the overall circuit cost will be low. To evaluate the effectiveness of the proposed scheme, a case study is used [5]. A set of parallel FIR filters with 16 coefficients is considered. The input data and coefficients are quantized with 8 bits. The filter output is quantized with 18 bits. The first evaluation is to compare the resources used by the proposed scheme with those used by TMR, the protection method proposed, and by an unprotected filter implementation.

SIMULATION RESULTS:

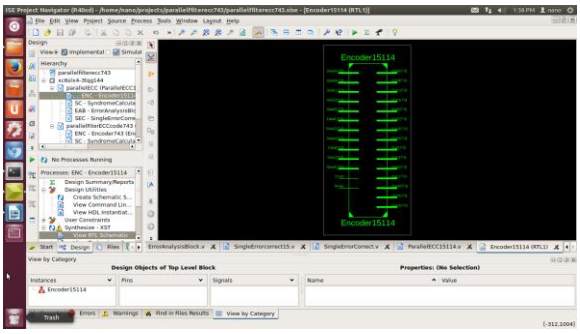

Fig: Encoder

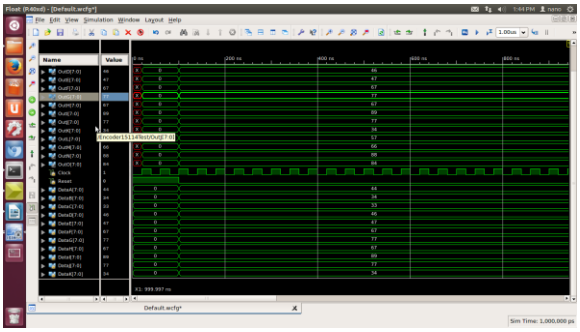

Fig : Simulation Form

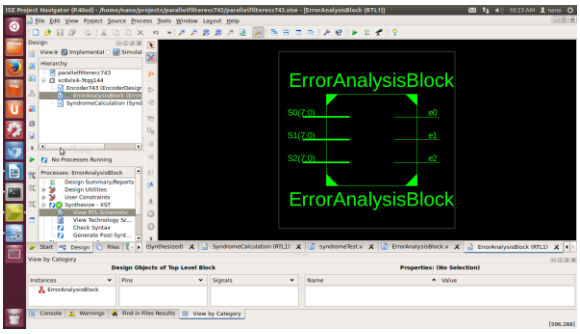

Fig: Error Analysis Block

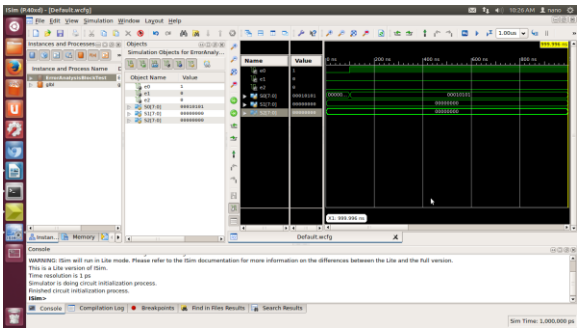

Fig: Simulation Result

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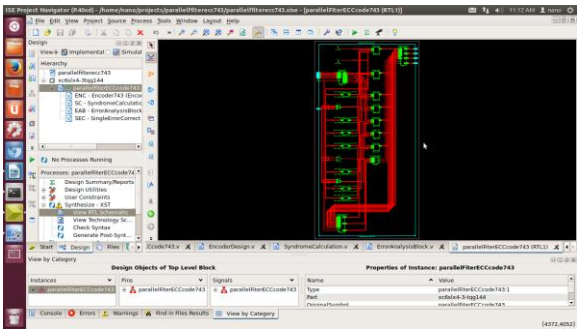

Fig: Parallel Filter

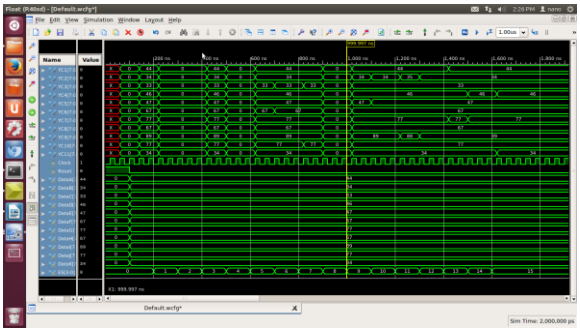

Fig: Simulation Form

III. CONCLUSION

A case study has also been discussed to show the effectiveness of the scheme in terms of error correction and also of circuit overheads. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. This brief has presented a new scheme to protect parallel filters that are commonly found in modern signal processing circuits. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was obtained. In this brief, a general scheme to protect parallel filters is presented. The technique provides larger benefits when the number of parallel filters is large. The proposed scheme can also be applied to the IIR filters. Future work will consider the evaluation of the benefits of the proposed technique for IIR filters. The extension of the scheme to parallel filters that have the same input and different impulse responses is also a topic for future work. The proposed scheme can also be combined with the reduced precision replica approach presented, to reduce the overhead required for protection. Another interesting topic to continue this brief is to explore the use of more powerful multipath ECCs, such as Bose–Chaudhuri–Hocquenghem codes, to correct errors on multiple filters. This will be of interest when the number of parallel filters is small as the cost of the proposed scheme is larger in that case.

IV. REFERENCES

[1] P. Reviriego, C. J. Bleakley, and J. A. Maestro, “Strutural DMR: A technique for implementation of soft-error-tolerant FIR filters,” *IEEE Trans. Circuits Syst., Exp.*

Briefs, vol. 58, no. 8, pp. 512–516, Aug. 2011.

[2] A. V. Oppenheim and R. W. Schafer, *Discrete Time Signal Processing*. Upper Saddle River, NJ, USA: Prentice-Hall 1999.

[1] M. Nicolaidis, "Design for soft error mitigation," *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 3, pp. 405–418, Sep. 2005.

[3] T. Hitana and A. K. Deb, "Bridging concurrent and non-concurrent error detection in FIR filters," in *Proc. Norchip Conf.*, 2004, pp. 75–78.

[4] A. Sibille, C. Oestges, and A. Zanella, *MIMO: From Theory to Implementation*. San Francisco, CA, USA: Academic Press, 2010.

[5] R. W. Hamming, "Error correcting and error detecting codes," Bell Syst. Tech. J., vol. 29, pp. 147–160, Apr. 1950.