The Reliability of Low Power Design Multiplier Using a Replica of the Vision Continued Collective Redundancies

[1] DasariNavya, [2] Mr. MorasaguruRajesh

[1] PG Scholar, Department of ECE, Nova College Of Engineering And Technology Jafferguda(V), Hayathnagar(M), Rangareddy(D)-501512

[2] M.Tech, Assistant Professor, Department of ECE, Nova College Of Engineering And Technology Jafferguda(V), Hayathnagar(M), Rangareddy(D)-501512

ABSTRACT:

In this paper, the area of efficiency multiplier put a sign suggests a fixed width through a replica redundancy through adoption My tolerance for noise (ANT) architecture with a multiplier of fixed width to build a redundancy version precision cutting Masa (RPR). ANT proposed architecture can meet the demand for high precision, low power consumption, and region Efficiency. RPR fixed-width design with error compensation through the circles of the possibilities and statistical analysis. use the When a partial product of the correct input vectors and vectors fixed in the palace and put in place to reduce truncation errors, hardware Failure holding circuit can be simplified compensation. The multiplier ANT 16 × 16 bits, the circuit area in our RPR fixed width It may be less, energy consumption in the design of ants can be saved as compared with the ANT state of the art design.

Keywords: Algorithmic Noise Tolerant (ANT), Fixed-Width Multiplier, Reduced-Precision Replica (RPR), Voltage Over Scaling (VOS), Error Tolerant Adder(ETA),Main Digital Signal Processing(MDSP)

INTRODUCTION:

The rapid growth of mobile and wireless systems In recent years, the need for systems pushing ultra-low energy. To reduce power dissipation, and measuring the voltage. [1] It is widely used as a technology of low energy efficient, and Power consumption in CMOS circuits game The square of the supply voltage. However, in the semi-depth micrometer process technologies, has raised the problems of noise interference Difficulty in design and efficient reliable microelectronic Systems, and therefore, design techniques to improve the noise Tolerance has developed a large scale [2] - [8]. Aggressive low energy technology, referred to as the voltage across the dimensioning (VOS), and aim to reduce the supply volt age out critical supply voltage without sacrificing productivity. However, VOS lead to a sharp deterioration in the signal to noise ratio, Ratio (SNR). My novel noise tolerant (ANT) The combination of technology VOS main block with low resolution Copy (RPR), who is struggling with software bugs effectively, while Achieve significant energy savings. Some

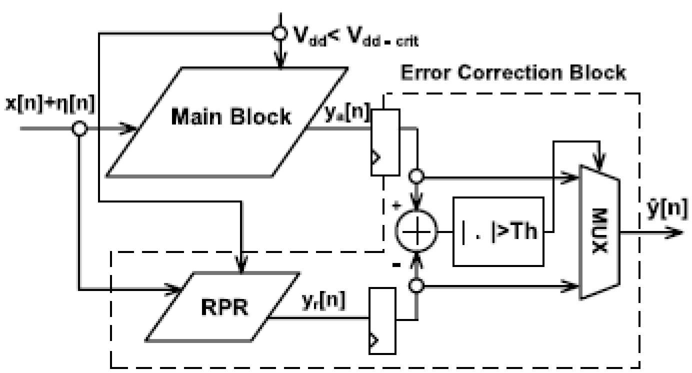

Fig. 1. ANT architecture [2].

ANT deformation The designs presented in [5] - [9] The design concept is ANT Extended system level. However, the design of RPR ANT is intended, and that is not easy Adopted and repeatedly. RPR designs in ANT designs can work on Too fast, but the hardware complexity is also Complex as shown in Figure 1. As a result, the design RPR ANT design design is still the most popular because of its Simplicity. However, with the adoption of RPR must still pay In the additional area and power consumption. In this work, We also suggest an easy way by using a fixed-width RPR To replace the block RPR full width. The use of a fixed width RPR, a miscalculation can be corrected with low Energy consumption and low overhead region. we use Probability and statistics, and a partial analysis of the product weight Finding a company about compensation for greater accuracy RPR design. In order not to increase the critical path delay, Restricting compensation circuit in the RPR should not be Located on the critical path. As a result, we can achieve ANT is designed with the small area of the circle, low power Consumption, supply voltage and less critical

ANT multiplier design proposed US-ING A fixed-width RPR

In this paper, we have proposed, and the width RPR-fixed Rip place a total width of blocks RPR ANT design [2], It is shown in Figure 2, which can not only provide the highest Account accuracy, low power consumption, low Above the area of the

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RPR, but also carried out with high SNR, The effective area and the tension of the lower layer sup operation and low power consumption to achieve more ANT architecture. We demonstrate our wide design based on RPR fixed ANT ANT multiplier. Constant width designs usually DSP applications applied to prevent the

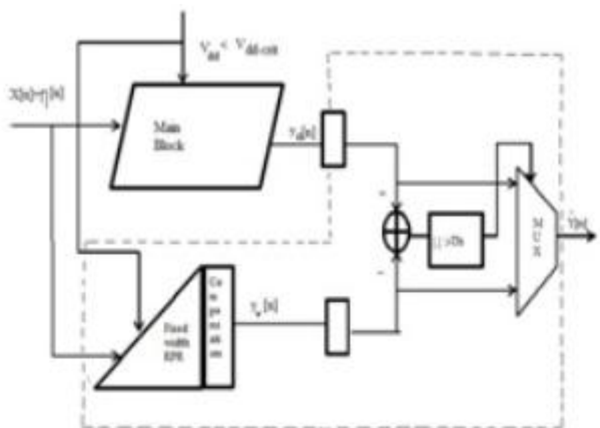

Fig.2. Proposed ANT Architecture with fixed width RPR.

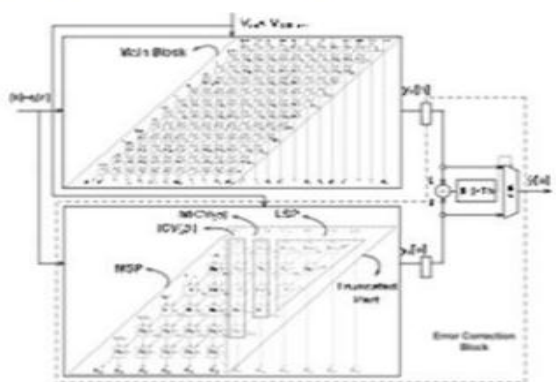

Fig.3.16 × 16 bit ANT multiplier is implemented with the 8-bit fiixed width Replica redundancy block.

growth of countless little

To show. Court n bits least significant bit (LSB) output is popular solution for the construction of a fixed width with n bits DSP The inputs and outputs n bits. Hardware complexity and power DSP consumption of a fixed width is usually about half One full length. However,truncated LSB results pane In rounding error, you need to compensate specifically. Many of Arts offer to reduce truncation Error correction with the value of continuing with the correct variable Value. The complexity of the circuit to compensate for a fixed The corrected value can be simpler than the variable Correction value. However, approaching the correct variable Usually more accurate, method of compensation is truncation error compensation between longitudinally Multiplier and fixed-width multiplier. However, in RPR has a fixed width of the multiplier ANT, compensation A mistake we have to correct is the general truncation error MSDP mass. On the contrary, we have a method of compensation for truncation error compensation between longitudinally MSDP multiplier and fixed-width multiplier RPR. Currently, there are a lot of fixed width multiplier Designs applied to the complications of full width. However, there It is not yet fixed width design RPR applied to the ANT multiplexed designs. To achieve more accurate Error Compensation, which offset truncation error with variable correction value. Error building compensation circuit especially the use of terms of partial products With more weight in less than a big slice. The The algorithm error compensation benefits from the possibility, Statistics, linear regression analysis to find The approximate amount of compensation [16]. To save the hardware Complexity, partial compensation carriers Product What has the greatest weight in less than a big slice And it is injected directly into the fixed RPR offer, which does not Need more logic gates compensation [17]. For more with less Error compensation, but must also take into account the impact of Truncated with the second most important bits products Error compensation. We propose a compensation error Circuit using the simple vector corrected minor tickets He remained offset error. In order not to increase critical path delay, and we are in a position Compensation Service in noncritical path of RPR fixed width. Compared to RPR complete design introduced in [15] and proposed a fixed width RPR multiplier leads not only with high SNR but also Circuits with low area and low power consumption. An error in the static screen proposed correction vector minutes ANT design highlighted in the design, function RPR To correct the errors that occur at the start and MSDP Maintaining the SNR of the entire system during cutting supplies Aalkahrby effort. If a fixed-width RPR is used to ANT Architecture, and it went for a smaller circuit area and power Consumption, but also accelerate the speed of calculation, Compared to traditional total length of the RPR. But nevertheless, We need huge compensation truncation error due to cut Stop many hardware elements of the MSDP LSB. At MSDP n bits ANT POV-multiplier and the Crown group, two for And it can be expressed in a signed n-bit input X and Y as he (/ 2 N) all Baugh- bit width and partial Crown unsigned product Group can be divided into four sub-groups, which are the most A large part (MSP), correct input vector [ICV (SS)].

Fault tolerant application AD-DER

In digital signal processing In photos and many other DSP processing applications, Fast Fourier Transform (FFT) is very important Function. FFT calculation involves a A number of additions and strokes. It is therefore A good platform to include our pro-ETA raised. to try Viability of ETA, which put all the common Extras involved in the normal track algorithm with our French Federation It was suggested that the account is added. As we all know, the digital image Represented by the matrix in the DSP system, each element Matrix represents the color of a single pixel of the image. To compare the quality of the images and processed by each of the Traditional French Federation French Tennis Federation minutes of tennis, which housed ETA have proposed, we have created the following Experience. The image has been translated for the first time in the form of a matrix It is sent through the standard system that made use of the usual French Tennis Federation and the French Union of reverse normal tennis. This output matrix The system then turned back to the image and the screen In Figure 3. It was also treated the same image matrix in FFT system used accurate and inaccurate vice FFT, where both 16-bit multiplier FFT include It is described in section, with the image processed form. 4 (b). Although the two matrices derived from the same image They are different, and the two images that have been obtained (see Figure 4) are Often the same thing. Figure 4 (b) is a little darker and has a horizontal bands of different shades of gray

CONCLUSION

In this paper, it is to introduce the concept of tolerance in error VLSI design. A new species of snake, and the snake error tolerant, That sells a certain amount of Milan-pastor of the importance of Save energy and improve performance, and propose. Wide comparisons with conventional digital hoses It was shown that the proposed multiplier exceeded Traditional power consumption and speed snakes Performance. Potential applications for the fall of the multiplier Especially in areas where there are no strict requirements Accuracy or where ultra-low power consumption and high speed Accuracy is more important than performance. One An example of these applications in the application of DSP portable devices such as mobile phones and laptops.

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