

# A Novel Architecture For High Performance T.L - Multiplier

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**ABSTRACT:** This paper presents the design an triginic logic [T.L] multiplier for 32\*32 bit number multiplication. Modern system of computer is a unique multiplier which is a very high speed and dedicated. Therefore, this paper presents the design an triginic logic multiplier. The proposed system generates M,N and interconnected blocks. By extending bit of the operands and generating an additional product the triginic logic multiplier is obtained. Multiplication operation is performed by the triginic logic is efficient with the less area and it reduces delay i.e., speed is increased.

**Keywords:** T.L, partial products, triginic logic unit.

## INTRODUCTION

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have long latency, consume considerable power and large area. Therefore low-power multiplier design has been an important part in the system of VLSI of low-power. There has been extensive work on low-power multipliers at technology, physical, circuit and levels of logic.

The performance of a system is determined in general by the performance of the multiplier because the multiplier is generally the slowest element in the system.

Furthermore, it is generally the most area consuming. Hence, optimizing the multiplier's area and speed is a major issue in design. However, area and speed are usually conflicting constraints to improve the results of the speed typically in larger areas. As a result, a whole spectrum of multipliers with different speed-area constraints designed with entirely parallel.

The high speed multipliers and pipelined multipliers are used for the applications of digital signal processing (DSP) such as for multimedia and communication systems. The applications of high speed DSP computation such as Fast Fourier transform (FFT) require additions and multiplications. The conservative Modified Booth Encoding (MBE) generates the partial product which is irregular array because of the extra partial product bit at the smallest amount of significance at each of the row product bit position. Therefore papers [4] presents a simple approach to be generated fewer partial product rows as a regular partial product array with and negligible overhead, thereby lowering the complexity of the product of partial

reduction and reducing the area, delay, and power of MBE multipliers. But the drawback of this particular multiplier is that it will be functioned only for number of signed operands.

A column-bypassing multiplier is an improvement of the normal of multiplier of array (AM). The array multiplier consists of  $(n-1)$  rows of carry save adder (CSA), in which each of row will contain  $(n - 1)$  full adder (FA) cells. Each of the FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit which goes to the FA's lower left. The very last row is a ripple adder for carry propagation.

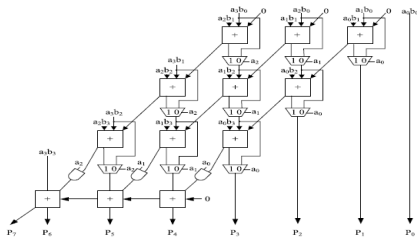


Fig 1 column-bypassing multiplier.

**PROPOSED SYSTEM:**

The gates in the trigic logic [T.L] multiplier are always active regard of input logics. In, trigic logic [T.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 2 shows a  $N \times N$  trigic logic [T.L] multiplier, it can be seen that the  $M_0, M_1, \dots, M_n$  done their outputs and the operations have been passed to interconnected.

Block and N-Block simultaneously. Depends on the preference of operation the trigic logic gives the N-block output to interconnected block and vice versa. Therefore, adders output is in both diagonals is 0, and the output sum bit is simply equal to the third bit. The above fig. 2 shows the  $4 \times 4$

high performance trigic logic multiplier reduced the timing waste occurring in traditional circuits that usage of the critical path of the cycle as an cycle period of execution. The basic concept is to execute a shorter path using trigic logic. Since most of the paths execute in a period of cycle that is much smaller than the critical path delay. The same architecture is extended up to  $32 \times 32$  bits.

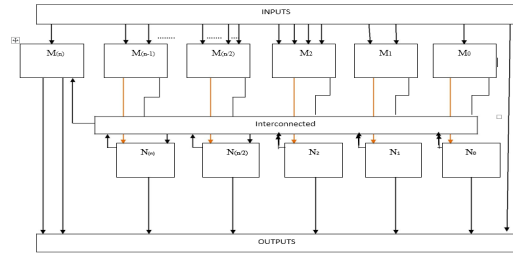


Fig. 2 4 x 4 HIGH PERFORMANCE TRIGIC LOGIC

Trigic logic widely been adopted in multipliers since it can be reduced to the number of rows of partial product to be added, thus reducing the size and enhancing the speed of the tree which is in reduction. The slightest major position of bit of each partial product row encoding, leading to an irregular array of partial product and reduction tree which is complex. Therefore, the trigic logic multipliers with partial product array produce a very high speed.

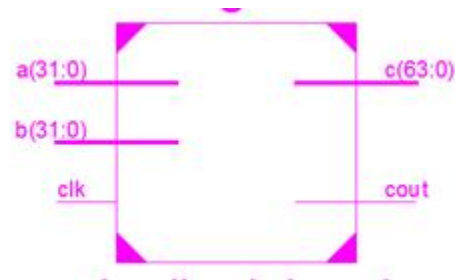


Fig. 3 R.T.L Schematic

The above fig. 3 shows the R.T.L schematic of high performance trigic logic multiplier

and fig. 4 shows the technical schematic one of the LUT block of high performance trigic logic multiplier.

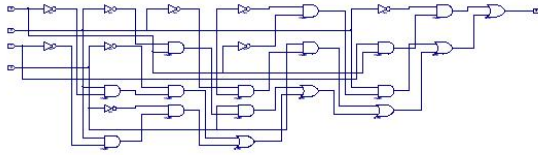


Fig. 4 LUT in technical Schematic

The below figure 5 shows the output waveform of 32\*32 bit trigic logic multiplier.

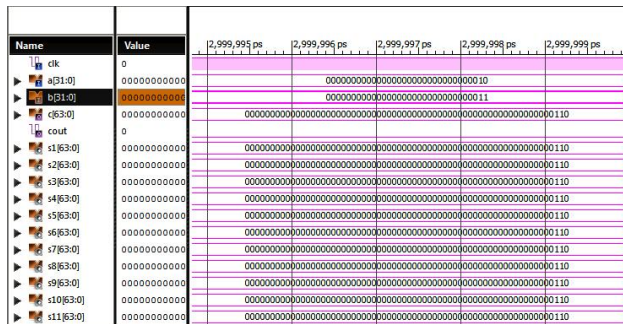


Fig. 5 OUTPUT Waveforms

The below table 1 shows the comparison of existed system and proposed system with area and delay

System/parameter	Area[kb]	Delay[ns]
Existed System	382256	110
Proposed system	243824	42

Table.1 comparison table

The above table of comparison shows the proposed system of the area is less than existed system and delay is also efficient. The representation of graphical of the parameters are shown below

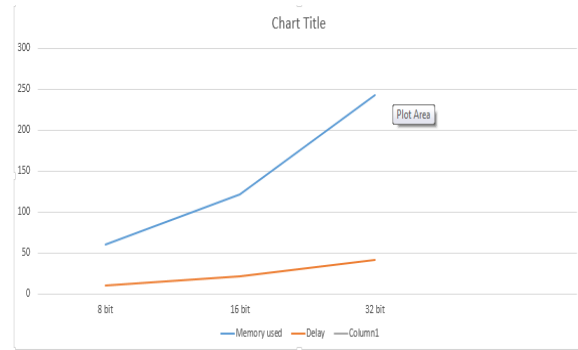


Fig. 6 graphical representation

The blue line shows the area and the additional shows the delay.

### CONCLUSION

The system which was proposed generates M, N and interconnected block. The each and every block consists the gates and the architecture of the row is lesser than existed multiplier. By generating an product with trigic logic multiplier is obtained. Multiplication operation is performed by the trigic logic unit is better presentation than that of multiplier which is already existed. The required hardware and the chip memory reduces and it reduces delay i.e., speed is increased.

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