Design of Fastest Multiplier Using Delay Efficient Carry Skip Adder

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ABSTRACT: Design of a high performance and high density multiplier is presented. This multiplier is constructed by using the Delay efficient carry skip adder. In previous we read about the designing of multipliers using the ripple carry adders and carry select adders. By using the ripple carry adders and carry select adders the propagation delay is high. In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying concatenation and increment schemes to improve the efficiency of the conventional CSKA (Conv-CSKA) structure. In addition, instead of utilizing multiplexer logic, the proposed structure makes use of AND-OR- Invert (AOI) and OR-AND-Invert (OAI) compound gates for the skiplogic. The structure may be realized with both fixed stage size and variable stage size styles, where in the latter further improves the speed and energy parameters of the adder. The proposed multiplier design involves significantly less delay than the recently proposed multipliersusing carry select adders. Also, the results of multipliers designed by using both carry skip adderand carry select adder are compared. The results are synthesized using Xilinx 13.2 Software and simulated using Model sim Software.

INTRODUCTION

ADDERS are a key building block in arithmetic andlogic units (ALUs) [1] and hence increasing their speedand reducing their power/energy consumption strongly affectthe speed and power consumption of processors. There aremany works on the subject of optimizing the speed andpower of these units, which have been reported in [2]–[9].

Obviously, it is highly desirable to achieve higher speeds atlow-power/energy consumptions, which is a challenge for the designers of general purpose processors.

One of the effective techniques to lower the powerconsumption of digital circuits is to reduce the supply voltagedue to quadratic dependence of the switching energy onthe voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through thedrain-induced barrier lowering effect [10]. Depending on theamount of the supply voltage reduction, the operation ofON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakagepowers compared with the near/sub threshold regions.

In the sub threshold region, the logic gate delay and leakage powerexhibit exponential dependences on the supply and thresholdvoltages. Moreover, these voltages are (potentially) subject toprocess and environmental variations in the nano scale technologies. The variations increase uncertainties in the aforesaidperformance parameters.

In addition, the small sub threshold current causes a large delay for the circuits operating in the sub threshold region [10].Recently, the near-threshold region has been consideredas a region that provides a more desirable trade off point between delay and power dissipation compared with that of the sub threshold one, because it results in lower delay compared with the sub threshold region and significantly lowersswitching and leakage powers compared with the super threshold region. In addition, near-threshold operation, whichuses supply voltage levels near the threshold voltage of transistors [3], suffers considerably less from the processand environmental variations compared with the sub threshold region.

The dependence of the power (and performance) on thesupply voltage has been the motivation for design of circuitswith the feature of dynamic voltage and frequency scaling.In these circuits, to reduce the energy consumption, the systemmay change the voltage (and frequency) of the circuit basedon the workload requirement [5]. For these systems, thecircuit should be able to operate under a wide range of supplyvoltage levels. Of course, achieving higher speeds at lowersupply voltages for the computational blocks, with the adderas one the main components, could be crucial in the design ofhigh-speed, yet energy efficient, processors.

To improve the performance of the adder structures at low supply voltage levels, some methods have been proposed in [7]–[9]. In [7]–[9], an adaptive clock stretching operation has been suggested. The method is based on the observation that the critical paths in adder units are rarely activated. Therefore, the slack time between the critical paths and the off-critical paths may be used to reduce the supply voltage. Notice that the voltage reduction must not increase the delays of the noncritical timing paths to become larger than the period of the clock allowing us to keep the original clock frequency at a reduced supply voltage level. When the critical timing paths in the adder are activated, the structure uses two clock cycles to complete the operation. This way the power consumption reduces considerably at the cost of rather small throughput degradation. In [7], the efficiency of this method for reducing the power consumption of the RCA structure has been demonstrated.

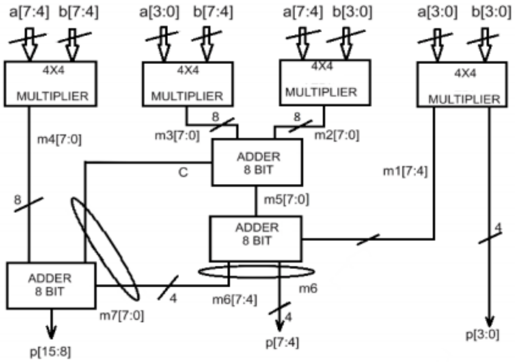


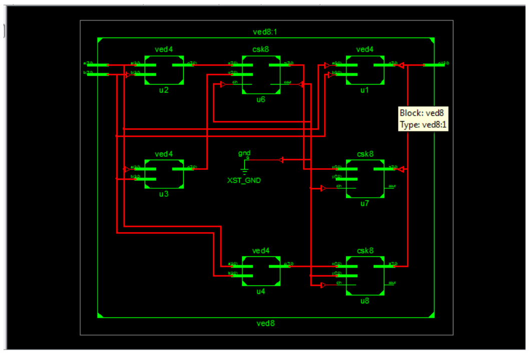
FIGURE.1 PROPOSED SYSTEM

In electronics, Multiplication is the most important arithmetic operation in signal processing applications. All the signal and data processing operations involve multiplication. As speed is always a constraint in the multiplication operation, increase in speed can be achieved by reducing the number of steps in the computation process. The speed of multiplier determines the efficiency of such a system. In any system design, the three main constraints which determine the performance of the system are speed, area and power requirement. In arithmetic operation, adder is the basic hardware unit. So adder performance affects the overall system-performance. Carry Select Adder (CSLA) is widely used in many data processors for high speed application and in digital circuits to perform arithmetic operations.

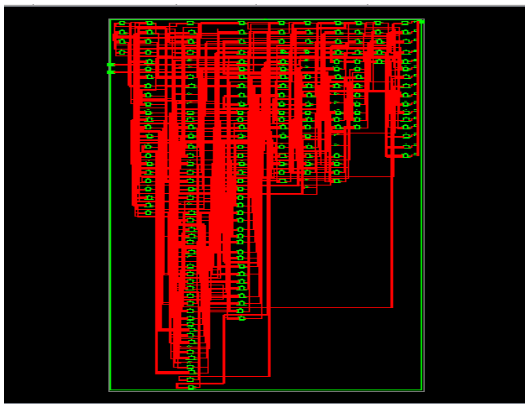
The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry-in being zero and the other assuming it will be one.

The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that of the multiplexer chain leading into it, so that the carry out iscalculated just in time. The delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

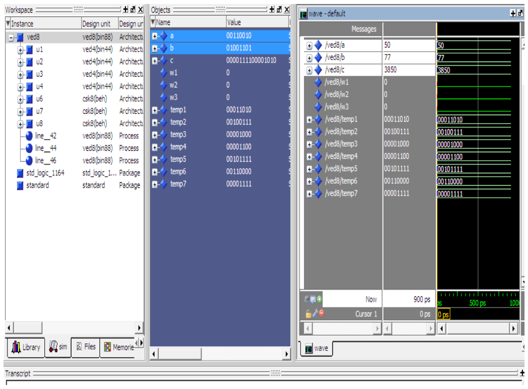
The R.T.L schematic diagram of 8x8 multiplier with carry skip adder is shown in below figure.



The technology schematic of 8x8 multiplier with carry skip adder is shown in below figure. It consists of LUT'S.



The output of 8x8 multiplier with carry skip adder in below figure.



Instance	Design unit	Design ur
ved8	ved8(bin88)	Architectu
u1	ved4(bin44)	Architectu
u2	ved4(bin44)	Architectu
u3	ved4(bin44)	Architectu
u4	ved4(bin44)	Architectu
u6	csk8(beh)	Architectu
u7	csk8(beh)	Architectu
u8	csk8(beh)	Architectu
line__42	ved8(bin88)	Process
line__44	ved8(bin88)	Process
line__46	ved8(bin88)	Process
std_logic_1164	std_logic_1...	Package
standard	standard	Package

Name	Value
a	00110010
b	01001101
c	0000111100001010
w1	0
w2	0
w3	0
temp1	00011010
temp2	00100111
temp3	00001000
temp4	00001100
temp5	00101111
temp6	00110000
temp7	00001111

wave - default

Messages		
/ved8/a	50	50
/ved8/b	77	77
/ved8/c	3850	3850
/ved8/w1	0	
/ved8/w2	0	
/ved8/w3	0	
/ved8/temp1	00011010	00011010
/ved8/temp2	00100111	00100111
/ved8/temp3	00001000	00001000
/ved8/temp4	00001100	00001100
/ved8/temp5	00101111	00101111
/ved8/temp6	00110000	00110000
/ved8/temp7	00001111	00001111
Now	900 ps	
Cursor 1	0 ps	0 ps

CONCLUSION:

This multiplier is constructed by using the Delay efficient carry skip adder. In previous we studied about the designing of multipliers using the ripple carry adders and carry select adders. By using the ripple carry adders and carry select adders there are some disadvantages. In this paper, we present a carry skip adder (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. The speed enhancement is achieved by applying innovative techniques. The proposed multiplier design involves significantly less delay than the recently proposed multipliers using carry select adders. Also, the results of multipliers designed by using both carry skip adder and carry select adder are compared. The results are synthesized using Xilinx 13.2 Software and simulated using Modelsim Software.

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