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Low Latency Low Complexity Compare and Decode Architecture for LTE Turbo Codes

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ABSTRACT: Another building design to matching those information secured for an error-correcting code will be exhibited in this short to decrease inactivity What's more multifaceted nature. In light of the way that the codeword of an ecc will be typically quell to An precise manifestation comprising of the crude information and the equality majority of the data produced Toward encoding, the suggested building design parallelizes those correlation of the information Also that of the equality majority of the data. Will further lessen those inactivity Furthermore complexity, to addition, another butterfly-formed weight gatherer will be suggested for those productive calculation of the turbo separation. Grounded on the BWA, the recommended building design looks at if those approaching information matches the saved information whether a sure amount about wrong odds would remedied. The recommended building design diminishes those inactivity and the fittings unpredictability by, compared for the practically later execution. The suggested construction modeling lessens those inactivity and the fittings multifaceted nature Eventually Tom's perusing ~33% Furthermore 10%, respectively, compared with those practically late usage.

Keywords: Reduce the latency, less complexity, High-speed access, Communication Decoding system.

1. INTRODUCTION

Information correlation will be generally utilized within registering frameworks on perform a number operations for example, the tag matching over a reserve memory and the virtual-to-physical address interpretation to An interpretation gaze a side cushion (TLB). Those information correlation normally resides in the discriminating way of the parts that need aid concocted on expand those framework performance, e. G. , caches What's more TLBs, whose outputs determine the stream of the succeeding operations over An pipeline. Those circuit, therefore, must a chance to be outlined with need Likewise low inactivity as possible, alternately the parts will a chance to be disentitled from serving Likewise accelerators and the generally execution of the entire framework might a chance to be extremely deteriorated.

As recent computers employ error-correcting codes (ECCs) to protect data and improve reliability, complicated decoding procedure, which must precede the data comparison, elongates the critical path and exacerbates the complexity overhead. Despite the need for sophisticated designs as described, the works that cope with the problem are not widely known in the literature since it has been usually treated within industries for their products. Recently, however, trigered the attraction of more and more attentions from the academic field. The most recent solution for the matching problem is the direct compare method, which encodes the incoming data and then compares it with the retrieved data that has been encoded as well. Therefore, the method eliminates the complex decoding from the critical path. In performing the comparison, the method does not examine whether the

retrieved data is exactly the same as the incoming data. Instead, it checks if the retrieved data resides in the error correctable range of the codeword corresponding to the incoming data.

codeword is usually represented in a systematic form in which the data and parity parts are completely separated from each other. In addition, as the SA always forces its output not to be greater than the number of detectable errors by more than one, it contributes to the increase of the entire circuit complexity.

2. LITERATURE REVIEW

The decode-and-compare architecture, the n-bit retrieved codeword should first be decoded to extract the original k-bit tag. The extracted k-bit tag is then compared with the k-bit tag field of an incoming address to determine whether the tags are matched or not. As the retrieved codeword should go through the decoder before being compared with the incoming tag, the critical path is too long to be employed in a practical cache system designed for high-speed access. Since the decoder is one of the most complicated processing elements, in addition, the complexity overhead is not negligible. The following section will point out the evolution of the proposed project's work and research till date:

I Performance evaluation of turbo codes using hard decision viterbi algorithm in vhdl

Susrutha Babu Sukhavasi, Suparshya Babu Sukhavasi, Dr.Habibulla Khan, IEEE Chiranjeevi Pilla/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 2, Issue 3, May-Jun 2012

We first briefly describe the algorithms of convolution encoder and hard decision Viterbi decoder. The focus of this work is towards developing an application specific design methodology for low power solutions. The methodology starts

As the checking necessitates an additional circuit to compute the Turbo distance i.e. the numbers of different bits between the two code words, the saturate adder (SA) as a basic building block for calculating the Turbo distance. However, a practical ECC from high level models which can be used for hardware solution and proceeds towards high performance hardware solutions. The methodology starts from algorithmic level, concentrating on the functional correctness rather than on implementation architecture. The effect on performance due to variation in parameters like frame length, number of iterations, type of encoding scheme. Turbo codes are used for error protection, especially in wireless systems.

II Reed-Solomon Turbo Product Codes for Optical Communications: From Code Optimization to Decoder Design

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The field of channel coding has undergone major advances for the last twenty years. With the invention of turbo codes followed by the rediscovery of low-density parity check (LDPC) codes, it is now possible to approach the fundamental limit of channel capacity within a few tenths of a decibel over several channel models of practical interest. Although this has been a major step forward, there is still a need for improvement in forward-error correction (FEC), notably in terms of code flexibility, throughput, and cost.

III Turbo and Turbo-Like Codes: Principles and Applications in Telecommunication

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France Manuscript received August 24, 2006; revised December 20, 2006.

For decades, the de facto standard for forward error correction was a convolution code decoded with the Viterbi algorithm, often concatenated with another code (e.g., a Reed–Solomon code). But since the introduction of turbo codes in 1993, much more powerful codes referred to collectively as turbo and turbo-like codes have eclipsed classical methods. These powerful error-correcting techniques achieve excellent error-rate performance that can closely approach Shannon's channel capacity limit. The lure of these large coding gains has resulted in their incorporation into a widening array of telecommunications standards and systems.

IV Cascaded feed forward architectures for parallel viterbi decoding

G. Fettweis and H. Meyr, "Cascaded feedforward architectures for parallel Viterbi decoding," in Proc. IEEE Int. Sym. Circuits Syst., May 1990, pp. 978–981.

The Viterbi-Algorithm (VA) is a common application of dynamic programming. Since it contains a nonlinear feedback loop (ACS-feedback, ACS: add-compare-select), this loop is the bottleneck in high data rate implementations. In this paper we show that asymptotically the ACS-feedback no longer has to be processed recursively, i.e. there is no feedback, resulting in negligible performance loss. This can be exploited to derive purely feed forward architectures for Viterbi decoding, such that a modular cascadable implementation results. By designing one cascadable module, any speedup can be achieved simply by adding modules to the implementation. It is shown that optimization criteria, e.g. minimum latency or maximum hardware efficiency, are met by very different architectures.

3. PROBLEM DEFINITION

In the decode-and-compare architecture, the n-bit retrieved codeword should first be decoded to extract the original k-bit tag. The extracted k-bit tag is then compared with the k-bit tag field of an incoming address to determine whether the tags are matched or not. As the retrieved codeword should go through the decoder before being compared with the incoming tag, the critical path is too long to be employed in a practical cache system designed for high-speed access. Since the decoder is one of the most complicated processing elements, in addition, the complexity overhead is not negligible.

Note that decoding is usually more complex and takes more time than encoding as it encompasses a series of error detection or syndrome calculation, and error correction.

- The critical path is too long
- Most complicated processing elements
- More complexity

4. RESEARCH METHODOLOGY

In the SA (saturate adder)-based architecture, the comparison of two code words is invoked after the incoming tag is encoded. Therefore, the critical path consists of a series of the encoding and the n-bit comparison. However, it did not consider the fact that, in practice, the ECC codeword is of a systematic form in which the data and parity parts are completely separated. As the data part of a systematic codeword is exactly the same as the incoming tag field, it is immediately available for comparison while the parity part becomes available only after the encoding is completed.

The proposed architecture grounded on the data path design is shown in Fig. 1. It contains multiple butterfly-formed weight accumulators (BWAs) proposed to improve the latency and complexity of the Turbo distance computation. The basic function of the BWA is to count the number of 1's among its input bits.

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- **SYSTEM BLOCK DIAGRAM:**

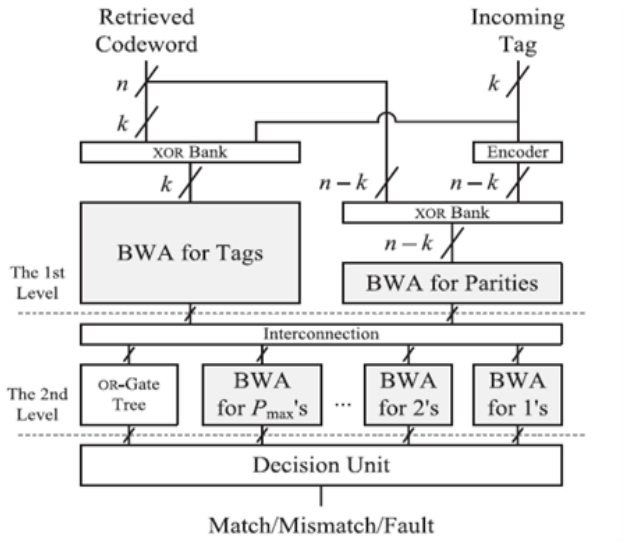

Fig. 1 Proposed architecture optimized for systematic code words

5. IMPLICATION

For a set of four codes including the (31, 25) code quoted, We measured the metrics at the gate-level first and then implemented the circuits in a 0.13-μm CMOS technology to provide more realistic results by deliberating some practical factors, e.g., gate sizing and wiring delays. The latency is measured from the time when the incoming address is completely encoded. As the critical path starts from the arrival of the incoming address to a cache memory, the encoding delay must be, however, included in the latency computation. performing post layout simulations and equivalent gate counts are measured by counting a two-input NAND as one.

The latencies of the SA-based architecture and the proposed one are dominated by SAs and HAs, respectively. As the bit-width doubles, at least one more stage of SAs or HAs needs to be added. Since the critical path of a HA consists of only one gate while that of a SA has several gates, the proposed architecture achieves lower latency than its SA-based counterpart, especially for long codewords.

The realization of this project will solve most of the difficulties discussed above and in the problem definition section. This project will have following results:

- Reduce the latency
- Less complexity
- High-speed access
- Communication Decoding systems

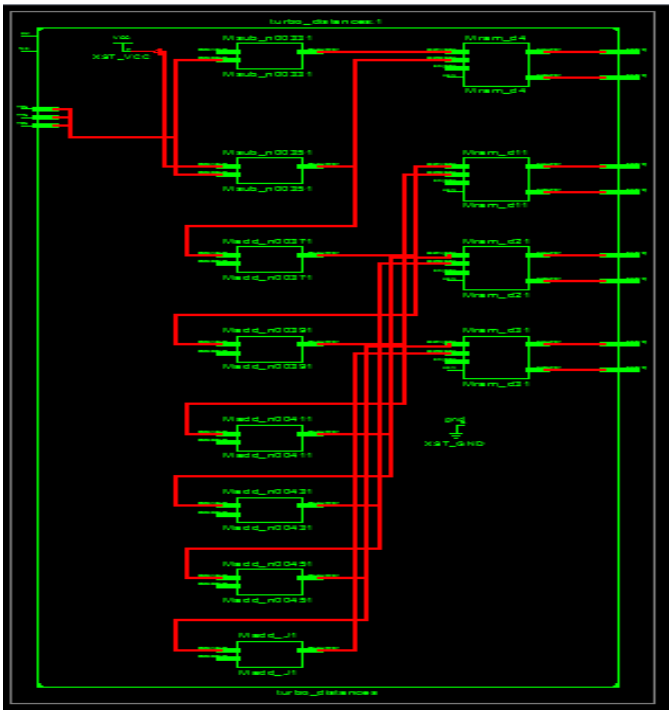

Fig. 2 turbo distances

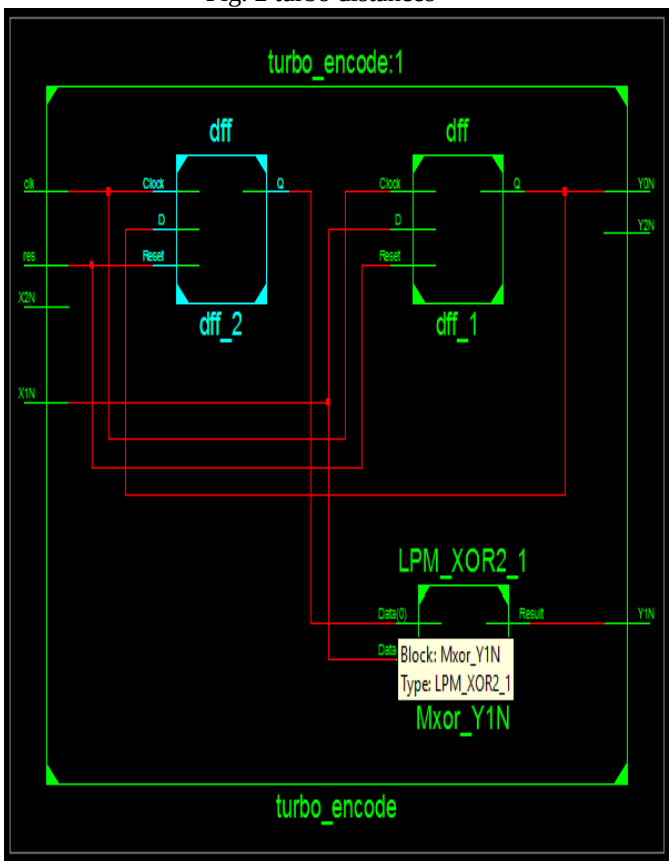

Fig. 3 turbo encoder

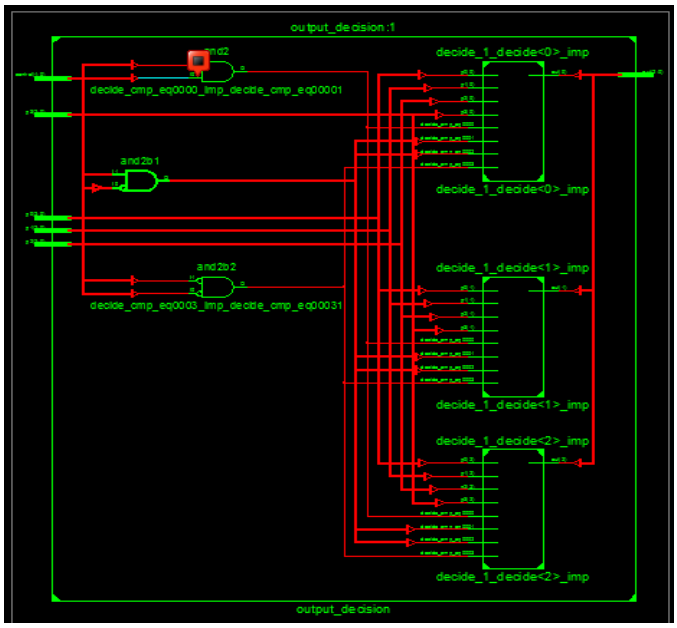

Fig. 3 turbo decoder

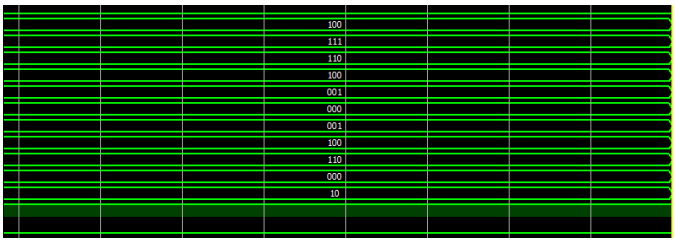

Fig. 4 Simulation result

Sr. no	X_n^1	X_n^0	Y_n^2	Y_n^1	Y_n^0
0	0	0	0	0	0
1	0	1	0	0	1
2	1	0	1	0	0
3	1	1	1	0	1

Table 5.1 a sequence of transmitted signals for the (a) Turbo encoder (b) Turbo encoder

Y_n^2	Y_n^1	Y_n^0	X_n^1	X_n^0	7-seg display
0	0	0	0	0	d
0	0	1	0	1	d
1	0	0	1	0	d
1	0	1	1	1	d
0	1	1	-	-	E

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