# A CMOS Based Balanced Differential Amplifier with MOS Loads

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*Abstract*— **The Balanced Differential Amplifiers play a most important role as basic building block in instrumentation amplifier circuit. One of the characteristic of a differential amplifier, the common mode rejection ratio (CMRR) is most important. The active load used for balanced differential amplifier is going to affect differential gain, thus CMRR of the circuit. The active load used can be a diode connected load or current source load. Though the differential gain is limited by nonlinearity of MOSFET, optimum differential gain can be obtained by combination of both active loads.**

*Keywords*——**CMOS, PMOSFET, NMOSFET, BALANCED DIFFERENTIAL AMPLIFIER (BDA), COMMON MODE REJECTION RATIO (CMRR), DIODE-CONNECTED LOAD, CURRENT SOURCE LOAD, SLEW RATE, GAIN, TANNER TOOL.**

## I. INTRODUCTION

The Balanced Differential Amplifier has been a versatile building block in analog circuits like instrumentation amplifier [5]. The instrumentation amplifier has been used in several applications as a signal conditioning circuit. However in order to use it in biomedical applications, it is required to amplify small high frequency differential signal in presence of strong common mode noise. It is needed to built instrumentation amplifier with improved CMRR and bandwidth together [2].

This paper presented the design and implementation of balanced differential amplifier with active loads: diode connected, current-source and combination of both. It implied that with combination of both loads optimum differential gain can be obtained. The current in source circuitry is taken to be current mirror source to provide biasing current 60μA [1].

### A. *Balanced differential amplifier with diode-connected load.*

In BDA the differential gain depends directly on load resistance connected. To achieve higher differential gain load resistance needed to be increase. In CMOS technologies, it is difficult to fabricate resistors with reasonable physical size. It is desirable to replace load with a MOSFET. A MOSFET with gate and drain shorted becomes a diode and offers a small signal resistance. This configuration behaves like a two-terminal resistor. As gate and drain is shorted the transistor is always in saturation. The impedance offered by diode can be obtained by replacing MOSFET by its small signal equivalent circuit. The impedance of diode becomes $(1/gm)\|r_d \approx 1/gm$. Where gm is a trans-conductance and $r_d$ is output resistance of MOSFET. If body effect is considered additional trans-conductance, $g_{mb}$ gets added to gm.

The transconductance gm is directly proportional to aspect ratio of MOSFET (W/L). As aspect ratio is reduced, gm gets reduced with increase in gain of MOSFET amplifier at the cost of reduced drain current and output swing. The small signal differential gain of BDA as shown in Fig. 1 has been derived using the half circuit concept. Here in differential mode it was assumed that sources of M1 and M2

were at virtual ground (AC ground). The diffrential gain comes out to be [6]

In the circuit of Fig. 1, the diode connected loads consume the biasing votage which creates trade off between gain, output voltage swing and input common mode voltage range.
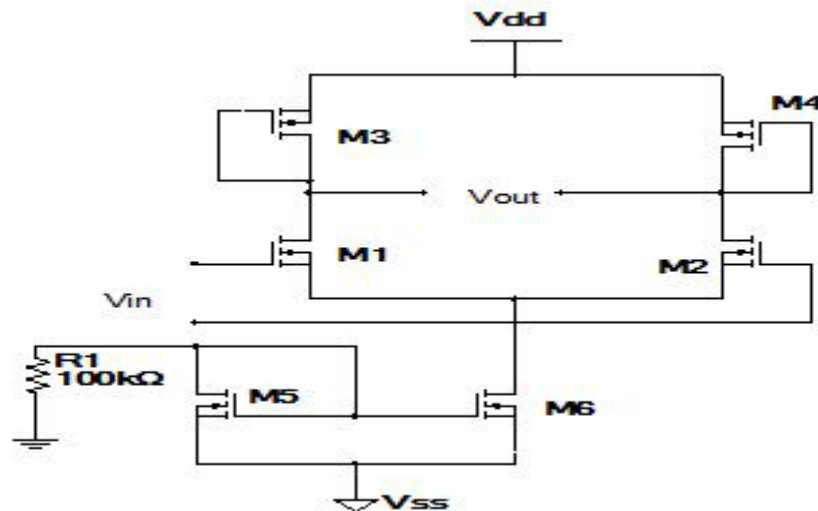
Figure 1. Balanced diffrential amplifier with diode-connected load

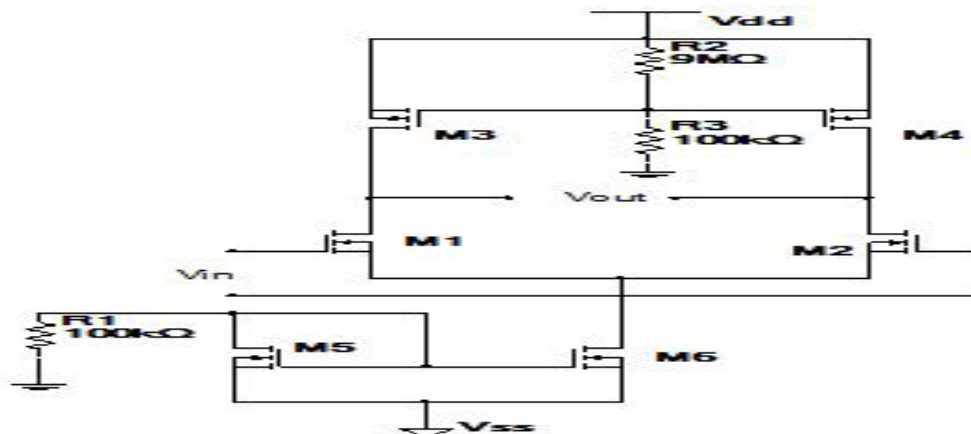## B. Balanced differential amplifier with current-source load.



**Figure 2. Balanced diffrential amplifier with current-source load**

The drawbacks of diode connected load can be minimized by replacing it with current source load [3], [4]. Here PMOS devices M3 and M4 operate in saturation and provide constant current to M1 and M2. The saturation of M3 and M4 is assure by resistors R2 and R3. Now the total impedance seen at output

node is $r_{d1}$ parallel $r_{d3}$, and using half circuit concept the differential voltage gain becomes

$$A_v = -g_m\left(r_{d1} \| r_{d3}\right)$$

The advantage here is that the output impedance and biasing voltage of M3 are less strongly coupled as compared to resistive load. The biasing voltage of M3 can be reduced b increasing width (W). The rd3 can be increase by increasing W and L of M3 but at the cost of large capacitance introduced, thus reducing bandwidth.

## C. Balanced differential amplifier with combination of diode-connected and current source load.

The difficulties with the above circuits can alleviated by supplying considerable part (80%) of bias current of M1 and M2 by current sources and remaining (20%) by diode connected load. The idea here is to lower the gm of diode connected load devices by reducing their current instead of their aspect ratio. If M7 and M8 carry 80% of drain current of M1 and M2 the current through M3 and M4 is reduced by 5 times. For given biasing conditions, this reduces transconductance of M3 and M4 by 5 times. The differential gain now becomes approximately 5 times greater than with only diode connected load. The resistors R2 and R3 would be replaced by MOSFETs or in some of the circuits the current handled by current sources is dependent on bias voltage [7][8].

The frequency response of differential amplifier will depend on length of channel (L) selected. If lower L is selected MOS capacitances will have lower value thus increasing the bandwidth. The reduction in L is also going to limit current handling capability of MOSFETs. Thus selection of L will be tradeoff between bandwidth and current handling capability that is output power.
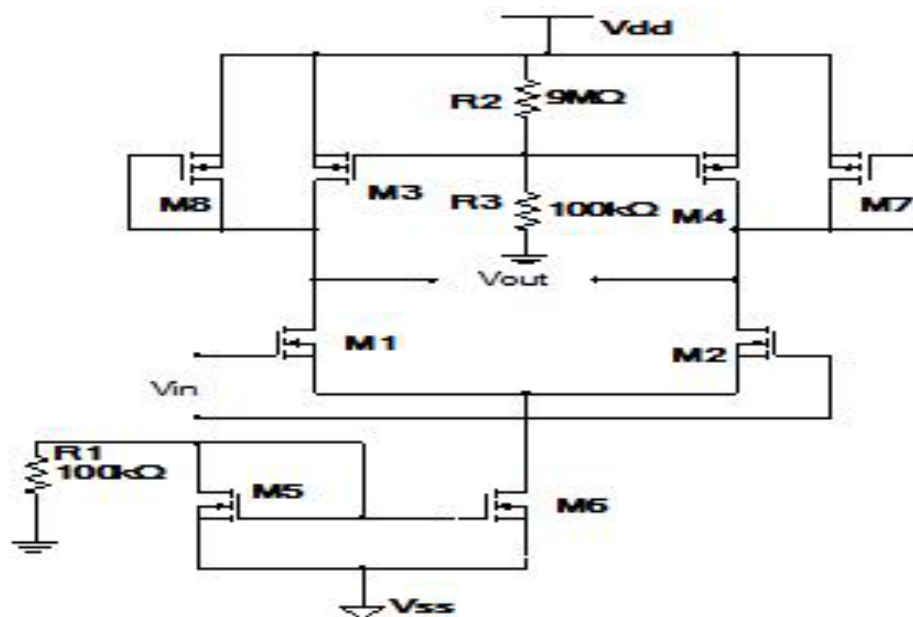


Figure 3. Balanced diffrential amplifier with combination of diodeconnected and current-source load

The proposed circuits were simulated using EDA tool Tanner V14.1 with 0.25μ CMOS technology. The simulated results agree with theory discussed as above. The MOSFETs were selected with different dimensions and results were simulated. One of the combination of suitable dimensions of load MOSFETs is presented here. The supply voltage selected was 2.5V with 60μA bias

current, thus total quiescent power consumption was 3mW.

### TABLE I. SIMULATED RESULTS

| parameter | Simulated Result | | |
|:---:|:---:|:---:|:---:|
| | **Figure 1** | **Figure** | **Figure 3** |
| $A_D$ | 7.15 | 3.05 | 2.3 |
| $A_C$ | 0.067 | 0.055 | 0.06 |
| CMRR | 40.56 dB | 34.87 dB | 51.67 dB |

## CONCLUSIONS

The differential gain of combined load balanced differential amplifier gets increased. The differential voltage gain BDA with combined load came out to be less than 5 times the gain as that of diode connected load, that was due to channel length modulation which becomes significant for short channel MOSFETs. The experimental results verifying the operation of the proposed circuits are provided.

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