International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

Reduction of harmonics with 9 level inverter for single phase grid connected system

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Abstract**:** Multilevel inverter has emerged recently as a very important alternative in the area of high-power medium voltage energy control. This project present cascaded multi cell with separate DC sources. Multilevel inverters are promising they have nearly sinusoidal output-voltage waveforms, output with better harmonic profile, less stressing of electronic components. The conventional is a single-phase seven-level inverter for grid connected photovoltaic systems, with a novel pulse width-modulated (PWM) control scheme .In a conventional concept to get the nine level inverter output voltage using a four full bridge cascaded type inverter. The inverter is capable of producing nine levels of output-voltage levels from the dc supply voltage. The proposed inverter system is capable of producing nine level of output voltage levels dc supply voltage by using three full bridge cascaded topology type inverter. In this project has used to three H-bridge inverter with different dc sources. The multi-level inverters promising the high performance with reduced EMI and harmonics. The proposed project is nine-level inverter was designed and results were also shown in the thesis. This project is focused on minimizing the number of semiconductors devices for a given number of levels.

Keywords-Multi level inverter; SPWM; harmonic analysis; power electronics;

I. INTRODUCTION

Since past few year power consumers like industrial and commercial consumers face numerous power quality problems. Among them are harmonics and unbalances which are of great interest. Voltage quality get deteriorate with tremendous increase of nonlinear loads connected at distribution level. The primary target of grid-connected generation is to guarantee grid-connected current with the same frequency and phase with grid voltage with the minimal total harmonic distortion (THD)[1-2]. In recent years, the multilevel voltage inverter has received wide attention in research and high-power applications such as large induction motor drives, UPS systems and flexible AC transmission systems and single phase grid connected systems. As compared to traditional two-level inverters, the multilevel inverters have more advantages, such as lower semiconductor voltage stress, better harmonic performance, low electromagnetic interference and lower switching losses[2].

The common topology of this inverter is full-bridge three level. The need of multilevel inverter is to give a high output power from medium voltage source like batteries, super capacitors, solar panel. Multilevel inverters are promising; they have nearly sinusoidal output voltage waveform. It also reduces the harmonics of output current. As compared to conventional two-level inverter multilevel inverter has less switching losses, less stress on electronic components due to decrease in voltage, a smaller filter size, and lower electromagnetic interference(EMI), all of which make them cheaper, lighter and more compact[4-6]. The multi level inverter consists of several switches. In the multi level inverter the arrangement switches angles are very important. To synchronies the inverter frequency with grid frequency closed loop control action is carried out[8-1O]. This paper presents the cascaded H-bridge multilevel inverters for single phase grid connected system and their effects on grid current. Any carrier based PWM is applicable for cascaded H-bridge (CHB). The working of CHB with phase shifted modulation is explained in this paper. The paper is organized as follows. Section II explains Cascaded H-bridge seven-level inverter. Section III explains the control strategy and Section IV presents the simulation results with harmonic analysis. Section V summarizes the result.

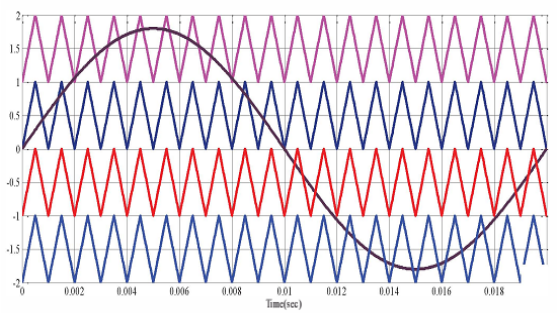
II. CASCADED H-BRIDGE MULTILEVEL INVERTER

Cascaded H-bridge (CHB) multilevel inverter is one of the popular topology for converter used in high power medium voltage drives. It contains multiple units of single phase H-bridge power cells. The H-bridge cells are normally connected in cascaded on its ac side to achieve low harmonic distortion and medium voltage operation. In practice, the number of power cells in a CHB inverter is mainly determines by its operating voltage and the cost required for manufacturing. The CHB multilevel inverter requires a number of isolated dc supplies each of which feeds an H-bridge power cell [3]. The number of voltage levels in a CHB inverter can be found from

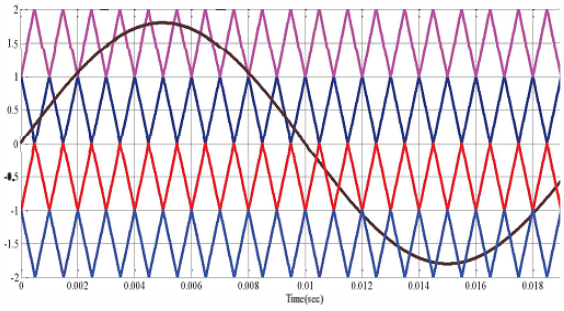
$$m = 2H + 1 \quad (1)$$

Where H is the number of cells per phase leg in H-bridge. For the CHB inverter, voltage level m is always an odd number while in other multilevel topologies like diode-clamped inverters it can have either an even or odd number of levels. Any carrier based PWM schemes can be used for CHB inverter. The carrier based modulation schemes for multilevel inverter can be classified in two categories as follows

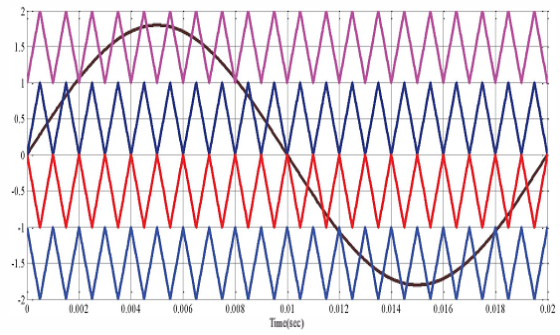
A. Level shifted multicarrier modulation The level shifted modulation scheme requires (m-I) triangular carriers for m level CHB inverter, all the carriers have the same frequency and the same amplitude. The (m-I) triangular carriers are vertically placed such that the bands forms by the carriers are contiguous. Following figure shows three schemes for the level shifted multicarrier modulation. (a) in-phase disposition (IPD), where all carriers are in phase; (b) alternative phase opposite disposition(APOD), where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition(POD), where all carriers above the zero reference are in phase but in opposition with those below the zero reference.



(a)IPD



(b)APOD



(c)POD

Fig. I. Level shifted PWM The frequency modulation index is given by

$$m_f = f_{cr} / f_m \quad (2)$$

Which remains the same as that for the phase shifted modulation scheme whereas the amplitude modulation index is defined as V,

$$m_a = \frac{V_m}{V_{cr}(m-1)} \quad (3)$$

Where Vm is peak amplitude of the modulating wave Vm and Vcr is the peak amplitude of each carrier wave.

B. Phase shifted multicarrier modulation In general, a multilevel inverter with m voltage levels requires (m-l) triangular carriers. In the phase shifted multicarrier modulation, all the triangular carriers have the same frequency and the same peak to peak amplitude, but there is a phase shift between any two adjacent carrier waves, given by

$$\phi_{cr} = 360^{\circ} /(m-1) \quad (4)$$

The modulating signal is usually a three phase sinusoidal wave with adjustable amplitude and frequency. The gate signals are generated by comparing the modulating wave with carrier waves.

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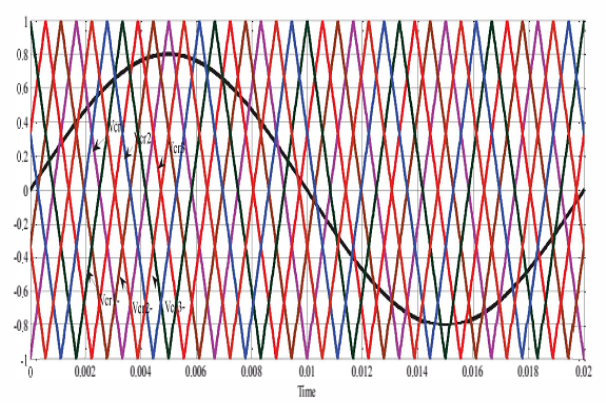

Fig. 2. Phase shift PWM for seven-level inverter

The principle of the phase-shifted modulation for a seven level CHB inverter is shown in fig. 2, where six triangular carriers are required with a 60° phase displacement (using equation (4)) between any two adjacent carriers. Modulating wave VMA is used. The carriers Veri, Vcr2, and Vcr3 are used to generate gatings for the upper switches QI, Qs, and Q9 in the left legs of power cells HI, H2 and H3 as shown in fig 3., respectively. The other three carriers, Vcrl-, Vcr2-, and Vcr3- , which are 1800 out of phase with Veri, Vcr2, and Vcr3, respectively, produce the gating for the upper switches Q2, Q6 and QIO in the right legs of the H-bridge cells. The gate signals for all the lower switches in the H-bridge legs are not shown since these switches operate in a complementary manner with respect to their corresponding switches [3]. The amplitude modulation index for phase shifted PWM as given in equation (5) is different than level shifted PWM. It does not depend on number of levels

$$m_a = \frac{V_m}{V_{cr}} \qquad (5)$$

TABLE I. SWITCHING TABLE

Output Voltage	Switching States		
	(Q1,Q2,Q3,Q4)	(Q5,Q6,Q7,Q8)	(Q9,Q10,Q11,Q12)
3E	(1,0,1,0)	(1,0,1,0)	(1,0,1,0)
2E	(1,0,1,0)	(1,0,1,0)	(1,1,0,0)
E	(1,0,1,0)	(1,1,0,0)	(1,1,0,0)
0	(1,1,0,0)	(1,1,0,0)	(1,1,0,0)
-E	(0,1,0,1)	(0,0,1,1)	(0,0,1,1)
-2E	(0,1,0,1)	(0,1,0,1)	(0,0,1,1)
-3E	(0,1,0,1)	(0,1,0,1)	(0,1,0,1)

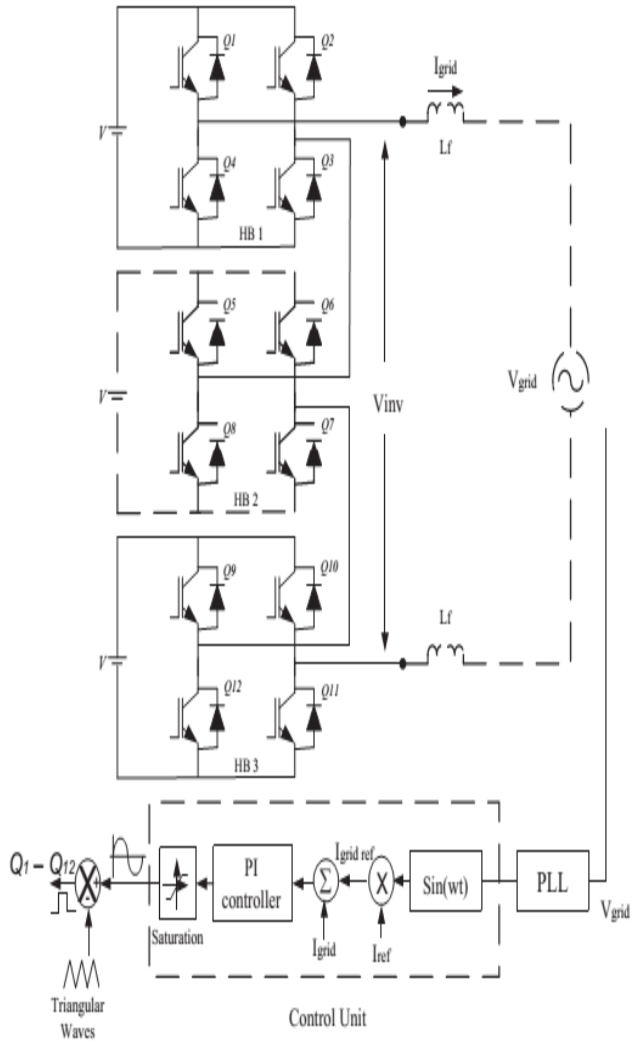

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Fig. 3. Circuit diagram of Cascaded Seven level Inverter for single phase Grid Connected System

In this Phase locked loop (PLL) is used to synchronies the grid frequency with the supply frequency which makes the grid voltage and grid current are in phase with each other as shown in simulation result section. The Lf is the current limiting filter to limit the grid current. The current limiting inductor Lf is given by

$$L_f = \frac{V_{DC}}{8 \times f_{sw} \times \Delta I_{L\max}} \quad (6)$$

Where VDC is the DC voltage of the inverter, Is", is switching frequency of the inductor and MLmax is ripple current of the inductor. The feedback current controller is used for this application. In this PI algorithm, Ire fis generated by comparing grid voltage with the reference voltage. Ire f is then multiplied by the output of PLL to generate 19ridre/- The current injected into the grid known as grid current Ignd, was sensed and fed back to a comparator that compared it with the reference current 19ridre/ The error from the comparison process of 19nd and Igridref was fed into the PI controller. The output of the PI controller, also known as Vref, being compared with the triangular wave to produce the switching signals for Q,-Q'2'.

IV MATLAB/SIMULINK RESULTS

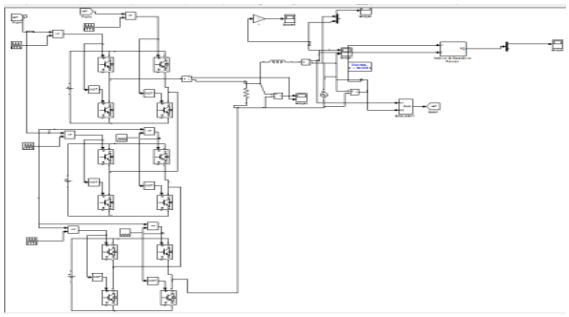
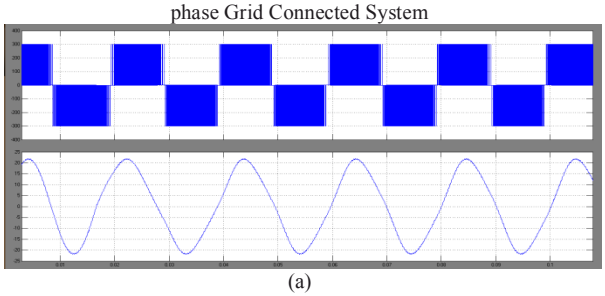


Fig 4 Circuit diagram of Cascaded Seven level Inverter for single phase Grid Connected System



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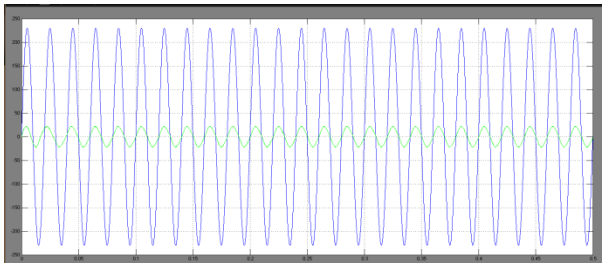

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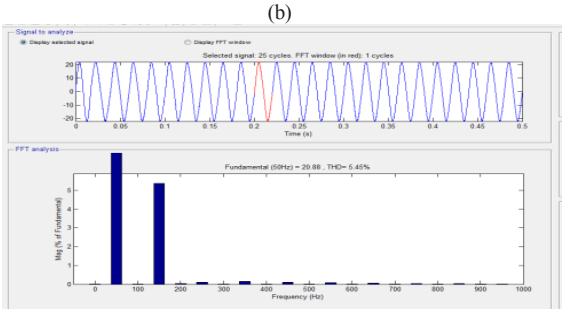
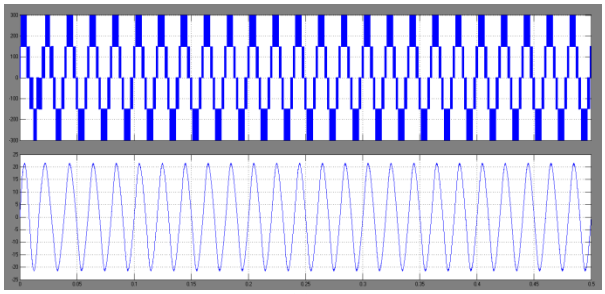
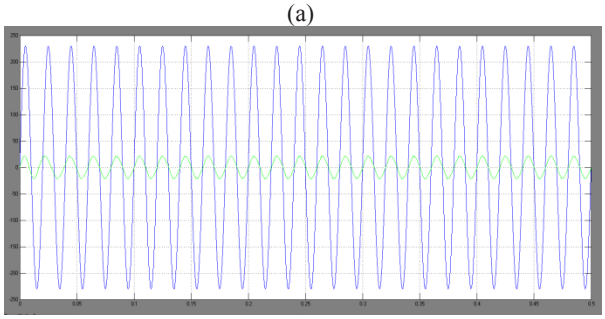


(c)

Fig, 5.(a) Three level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c)Harmonic Analysis of Grid Current



(a)



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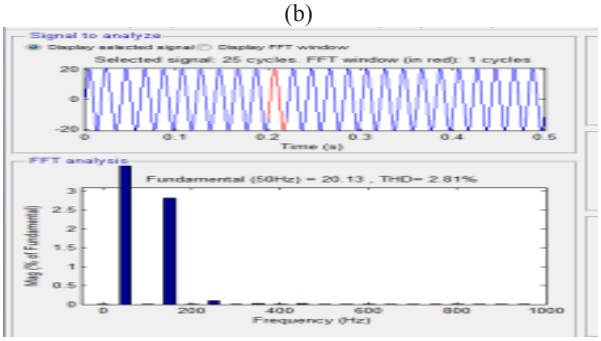

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p-ISSN: 2348-6848
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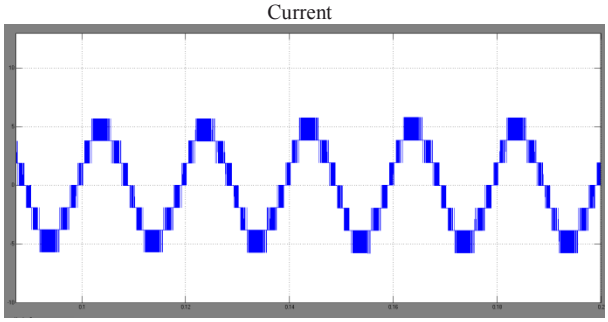
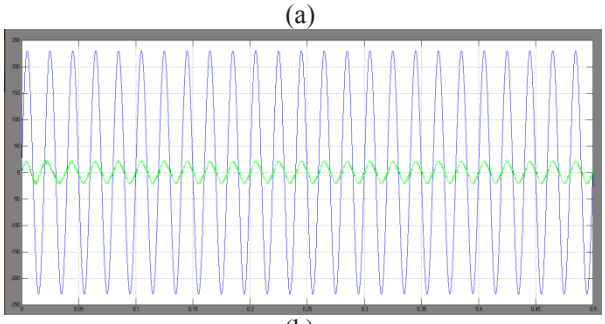
Fig. 6,(a) Five level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current



(a)



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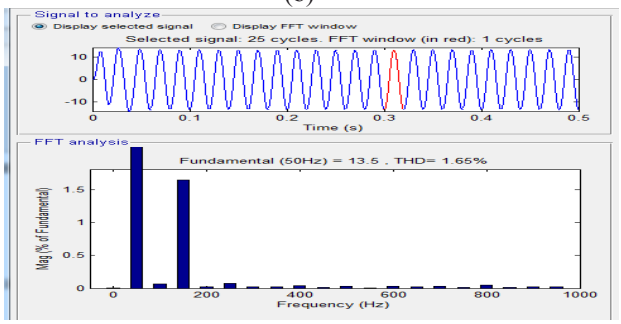


(c)

Fig 7(a) seven level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current

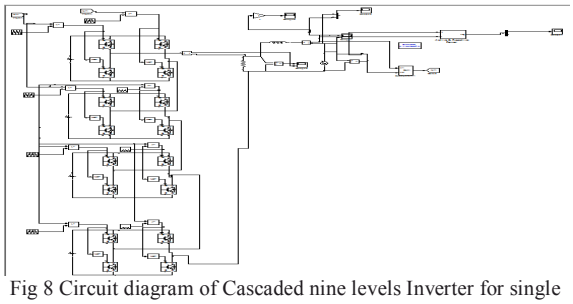
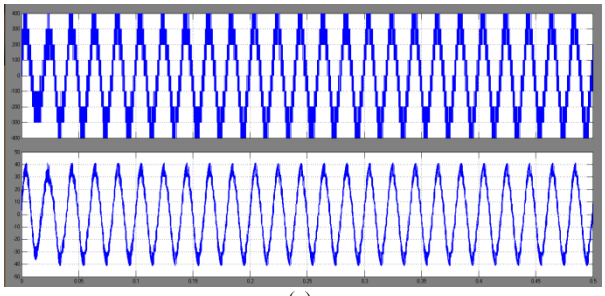
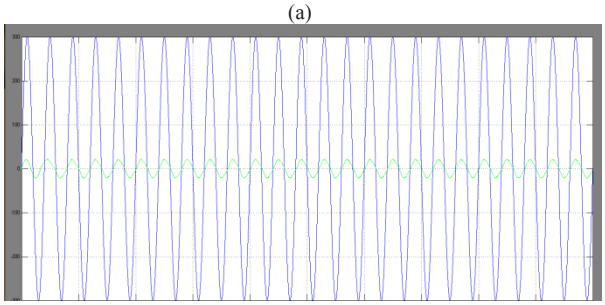


Fig 8 Circuit diagram of Cascaded nine levels Inverter for single phase Grid Connected System



(a)



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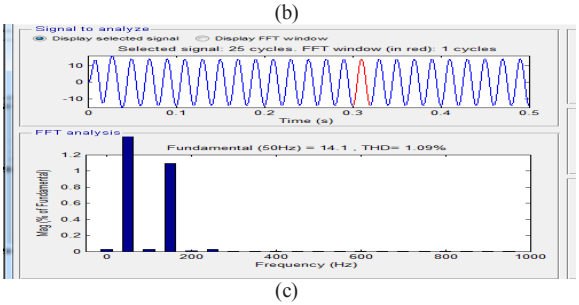

(c)

Fig 9 (a) nine level Output voltage of inverter (b) In phase waveform of grid voltage and grid current (c) Harmonic Analysis of Grid Current

V. CONCLUSION

This paper presents the design and simulation of cascaded H-bridge seven level inverter for single phase grid connected system. Control strategy is carried out to synchronies the grid frequency with the inverter frequency and to generate the modulating wave to fire the switches of the inverter. The harmonic analysis of grid current is carried out for different levels. From the analysis it is clear that as the number of levels increases the %THD decreases. So multilevel inverter is used for grid connected system to inject less harmonic current to the grid.

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