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ADCS real division: Linear improvement with Optimization of power and speed

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Abstract—A 500-MS/s 5-bit ADC for UWB applications has been fabricated in a 65-nm CMOS technology using no analog-specific processing options. The time-interleaved successive approximation register (SAR) architecture has been chosen due to its simplicity versus flash and its amenability to scaled technologies versus pipelined, which relies on operational amplifiers. Six time-interleaved channels are used, sharing a single clock operating at the composite sampling rate. Each channel has a split capacitor array that reduces switching energy, increases speed, and has similar INL and decreased DNL, as compared to a conventional binary-weighted array. A variable delay line adjusts the instant of latch strobing to reduce preamplifier currents. The ADC achieves Nyquist performance, with an SNDR of 27.8 and 26.1 dB for 3.3 and 239 MHz inputs, respectively. The total active area is 0.9 mm2, and the ADC consumes 6 mW from a 1.2-V supply.

Index Terms—ADC, analog-to-digital conversion, deep-submicron CMOS, successive approximation register, ultra-wideband radio

I.INTRODUCTION

Analog-to-digital converters (ADCs) are key design blocks in modern microelectronic digital communication systems since they act as bridges between the analog and digital worlds. It is a necessary component whenever data from the analog domain, through sensors or transducers, should be digitally processed. Figure 1 depicts a typical signal processing system [1]. The analog input signal is first filtered to remove high-frequency components in order to avoid aliasing. Then the signal is sampled at frequency fS, and the discrete sampled data is quantized in the analog-to-digital converter (ADC). The digital outputs from ADC are executed in the digital signal processor (DSP). Finally, they return to an analog signal by the conversion of digital-to-analog converter (DAC) and smoothing of the followed reconstruction filter.

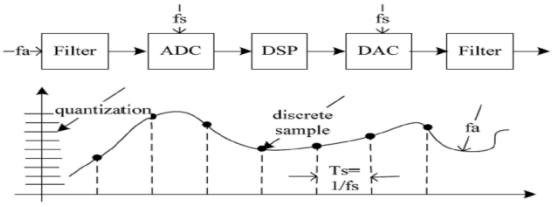

Figure 1 Basic signal processing system.

The first documented example of an ADC was a 5-bit, electro-optical and mechanical flash-type converter patented by Paul Rainey in 1921, used to transmit facsimile over telegraph lines with 5-bit pulse-coded modulation (PCM) [2]. The first all-electrical implementation came in 1937 by Alec Harvey Reeves, this also had a 5-bit resolution and the ADC was implemented by converting the input signal to a train of pulses which was counted to generate the binary output at a sample rate of 6 kS/s [2]. Following this, the successive approximation ADC was developed in 1948 by Black, Edson and Goodall to digitize voice to 5-bits at 8 kS/s [2]. Also in 1948, a 96 kS/s, 7-bit ADC was developed and it was implemented using an electron beam with a sensor placed on the other side of a mask. The mask had holes patterned according to the binary weights so that all bits were simultaneously detected, the pattern also employed Gray coding of the output in order to reduce the effect of errors in the most significant bit (MSB) transition [2], much as is done in modern high-speed flash ADCs [3]. Following the development of the transistor in 1947 and the integrated circuit in 1958, the ADC development continued in the 1960's with for example an 8-bit, 10 MS/s converter that was used in missile-defense programs in the United States [2]. During the same decade, all the currently used high-speed architectures were developed including pipeline ADCs with error-correction. In the recent years there has been a trend in ADC research to use low accuracy analog components which are compensated for through the use of digital error correction [3]. The

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motivation behind this is that analog design has not been able to benefit from process scaling in the same way as digital logic and therefore the relatively area-cheap digital logic is used to compensate for the shortcomings of expensive analog circuits.

Applications with Different Types of ADC Architectures

The four popular high-speed ADC architectures were described in the above sections. ADCs are selected according to specific application within the consideration of resolution, power, size, sampling frequency, performance and etc. Among the aforesaid four types of high-speed ADC, the time-interleaved ADC is a combination of several single channeled ADC, which is not suitable to be compared with the other three types of high-speed ADC architecture. So we just take the other three types of architectures, Flash, Pipeline and SAR as a comparison. For some applications, almost all the architectures may work well; for others, there may be a better choice to achieve the best performance. For example, a Flash ADC is most popular for applications requiring ultra-high speed when resolution and power consumption is not a primary concern; A SAR ADC is usually first considered to be implemented in the application of low power and small size with medium resolution[12-13]. Figure 2 shows the A/D converter application space according to different requirements of ADC sampling rate and resolution.

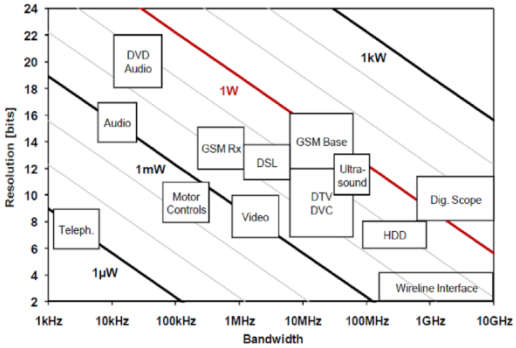

Figure 2 A/D Converter Application Space.

II. Design Considerations

Static errors are deviation of converter transfer characteristics from ideal one. The static performance of an ADC is defined by these metrics: offset error, gain error, and nonlinearities like DNL error and INL errors.

DNL[k] – The difference between the code bin width of code k and the average code bin width, divided by the average code bin width after correcting for gain and offset.

DNL – The maximum absolute value of DNL for all k. Simply, Figure 3 (a) suffers from large DNL but small INL. On the other hand, Figure 3 (b) suffers from large INL but relatively smaller DNL.

INL[k] – The difference between the ideal and actual code transition level k after correcting for gain and offset.

INL – The maximum absolute value of INL for all k.

As given in Figure 3 (a), these variations can be random with almost no correlation between successive steps. In this case the interpolating curve can be still very close the ideal one but the quantization error can vary significantly. In Figure 3 (b), the step size is small at the beginning but increases as the analog input becomes larger. Thus, there is a strong correlation between the successive steps and the interpolating curve moves away from the ideal one. However, the variation in the quantization error might be smaller [2]. To cover both of the cases presented in Figure 3, two different non-linearity specifications are used: 1) Differential Non-Linearity (DNL) and 2) Integral Non- Linearity (INL).

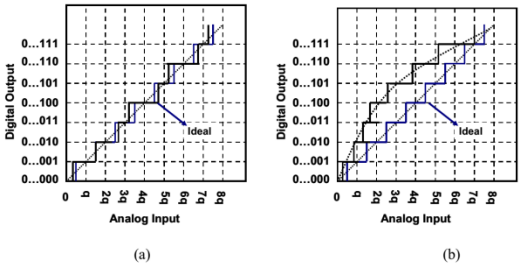

Figure .3 Two non-ideal transfer curves

Design considerations for SAR ADC with Binary-Weighted Capacitive DAC

A general SAR ADC is composed of an input sampling network (T&H), a comparator, a Digital-to-Analog Converter (DAC) and a digital controller (SAR Logic). The DAC has the same resolution as the ADC. The most critical block in a SAR ADC is the DAC. DAC can be implemented with many different well-known techniques. However, the most widely used DAC topology in SAR ADCs is the charge-redistribution based capacitive array 28 [4], as

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capacitive arrays do not dissipate static power and improve the power efficiency significantly. The most common capacitive DAC is the binary-weighted architecture which as been shown in Figure 4 with a 9-bit resolution. In this architecture, the input load capacitance and area of a binary-weighted capacitor DAC (CDAC) increase exponentially with the number of bits. For a 9-bit resolution as an example, the total input capacitance is equal to 512C and the total area is 512 times the unit capacitor area. This shows area un-efficiency by using this architecture.

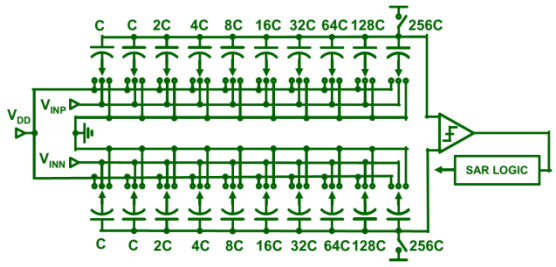

Fig4 Conventional binary-weighted CDAC based SAR ADC (9-bit).

Split CDAC is one of alternative to reduce both input capacitance and area, shown in Figure 5, a fractional value bridge capacitor is implemented so that the two capacitor arrays have the same scaling [5]. In the charge redistribution, the total weight of the left array is equal to the weight of the lowest bit in the right array.

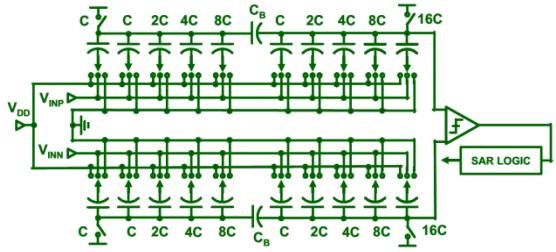

Figure 5 Differential split CDAC based SAR ADC (9-bit).

The performance of this type of SAR ADC is limited by:

A. The comparator, which must resolve small differences in VIN and VDAC within the specified time with accuracy;

B. Each of the capacitors associated with the data bits would be exactly twice the value of the next-smaller capacitor, and the settling time of the DAC, which must settle to within the resolution of the overall converter, for example, ½ LSB.

Therefore, the two critical components of this type of SAR ADC are the comparator and the DAC. The requirements of the comparator are speed and accuracy. Although comparator offset does not affect overall linearity as it appears as an offset in the overall transfer characteristic, the comparator needs to resolve voltages within the accuracy of the overall system. Therefore, offset-cancellation techniques are usually applied to reduce the comparator offset. It needs to be as accurate as the overall system. The comparator is usually designed to have input-referred noise less than 1 LSB.

III.PROPOSED METHOD

The -based switching method proposed in halves the array capacitance leading to around 90% energy saving when compared with the conventional one. The details the Vcm-based switching algorithm. In the global sampling phase _1, Vin is stored in the capacitor array. During the conversion phase _2, all the capacitors' bottom-plates are switched to the Vcm first, to give rise to the voltage −Vin at the output. The sign of Vout determines the MSB as the logic properly controls Sm,k−1. If −Vin < 0, Sm,k−1 goes to Gnd while the other switches Sm,k−2, …, Sl,0 remain connected to Vcm. If −Vin > 0, Sm,k−1 is switched to VDD. The cycle will be repeated for n − 2 times. The Vcm-based approach performs the MSB transition by connecting the differential arrays to Vcm.

The power dissipation is just derived from what is needed to drive the bottom-plate parasitic of the capacitive arrays, while in the conventional charge-redistribution where the necessary MSB "up" transition costs significant switching energy and settling time. Moreover, as the MSB capacitor is not required anymore, it can be removed from the n-bit DAC array. Therefore, the next n − 1 b estimation is done with an (n − 1) bit array instead of its n-bit counterpart, leading to half capacitance reduction with respect to the conventional method. Using supplies as reference voltages prevents static power dissipation from reference buffers.

The conversion becomes very sensitive to the supply ripple due to the switching effect. For 10-b accuracy the supply variation needs to be suppressed within ±0.049% of the full supply rail, or the supply ripple ±588 μV for a 1.2 V supply.. As the Vcm-based switching charges 75% less capacitance, simultaneously, when compared with the conventional switching, it can effectively reduce the under-shoot of the supply or reference buffer (when used). The inductive ringing effect can be well

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suppressed by minimizing the bonding inductance, e.g., multiple bonding, through the addition of a damping resistor and an on-chip decoupling capacitor Cdecp. On the other hand, to overcome this problem an effective approach might be the use of a SA searching algorithm like non binary conversion that relaxes the settling accuracy requirement during large switch transients.

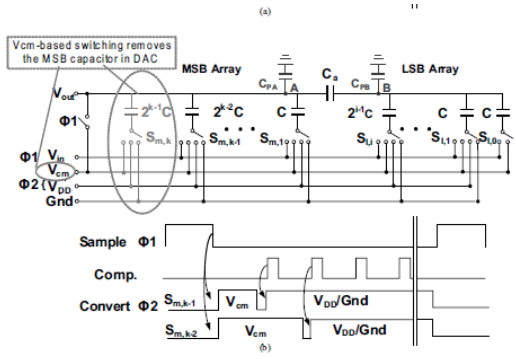

FIG6 Single-ended n-bit and (n − 1)-bit split capacitive DAC arrays

To calculate a given digital input X with its corresponding DAC output $V_{out}(X)$,

$$V_{\text{out}}(X) = \frac{\sum_{n=1}^{k}(2^{n-1}C+\delta_n)S_n + (C+\delta_0)S_0}{2^kC + \sum_{n=0}^{k}\delta_n}\cdot V_{\text{DD}} \quad (1)$$

$$\text{INL} = \frac{V_{\text{out}}(X)/A - V_{\text{idl}}(X)}{\text{LSB}}$$

$$\text{DNL} = \frac{[V_{\text{out}}(X) - V_{\text{out}}(X-1)]/A - \text{LSB}}{\text{LSB}}$$

$$A = \frac{\sum_{X=0}^{2^{n-1}} V_{\text{out}}(X)\cdot V_{\text{idl}}(X)}{\sum_{X=0}^{2^{n-1}} V_{\text{idl}}^2(X)} \quad (2)$$

$$V_{\text{out}}(X) = \frac{2^{k-1}C + \delta_k + C + \delta_1}{2^kC}\cdot V_{\text{DD}}$$

$$\text{INL}_{\text{con}} = \frac{\delta_k + \delta_1}{2^kC}\cdot\frac{V_{\text{DD}}}{\text{LSB}} = \frac{\delta_k+\delta_1}{C}$$

$$E[\delta^2_{\text{INLcon}}] = \frac{(2^{k-1}+1)\sigma^2}{C^2}. \quad (3)$$

$$V(X) - V(X-1) = \text{LSB} + \frac{1/2\sum_{n=0}^{k}\delta_n - \sum_{n=0}^{k-1}\delta_n}{C}\cdot\text{LSB}$$

$$\text{DNL}_{\text{CM}} = \frac{1/2\delta_k - 1/2\sum_{n=0}^{k-1}\delta_n}{C}$$

$$E[\delta^2_{\text{DNL}_{\text{CM}}}] = \frac{2^k\sigma^2}{4C^2}. \quad (4)$$

Show that the proposed method can achieve a DNL that is two times better in comparison to conventional switching. It can also be found that the error terms are decreased by half, which can be attributed to the cancellation of the terms. The capacitors contributing to two-bit transitions are correlated, which are switched from Vcm to VDD. In contrast, in the conventional method the capacitors connected to VDD in two-bit transitions are completely different, and the error terms are summed together instead of being cancelled.

VI.RESULTS ANALYSIS

(A)SPLIT SAR ADC: SAR ADC –

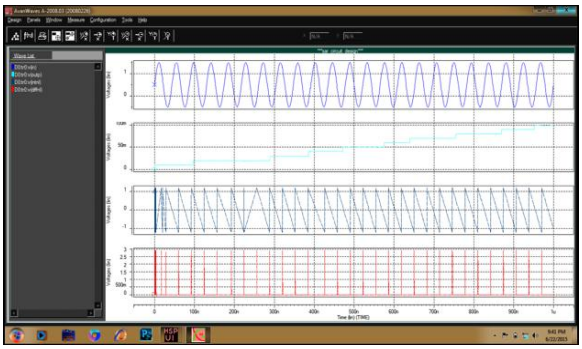

Figure 7: Analog input, digital output.INL &DNL errors for conventional SAR ADC

Proposed system:

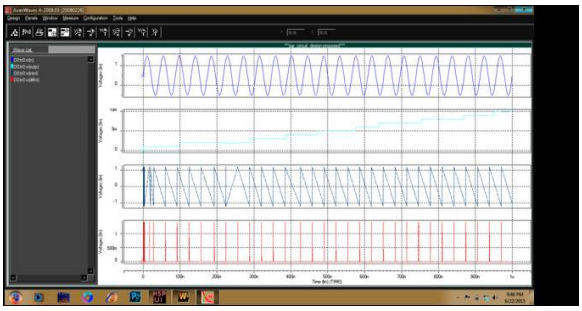

Figure 8: Analog input, digital output.INL &DNL errors for proposed Split SAR ADC

(B) Performance evolution:

Existing system:

Average value: 4.9648E-02
from 1.0000E-09 to 1.0000E-06
Maximum value: 1.0000E-02 at 9.5102E-07
from 1.0000E-09 to 1.0000E-06
Minimum value: 1.0000E-02 at 1.0000E-09
from 1.0000E-09 to 1.0000E-06
Peak to Peak value 9.0000E-02
from 1.0000E-09 to 1.0000E-06

Proposed system:

Average value: 4.9648E-02
from 1.0000E-09 to 1.0000E-06
Maximum value: 1.0000E-02 at 9.5102E-07
from 1.0000E-09 to 1.0000E-06
Minimum value 1.0000E-02 at 1.0000E-09
from 1.0000E-09 to 1.0000E-06
Peak to Peak value 9.0000E-02
from 1.0000E-09 to 1.0000E-06

(V)CONCLUSION

Two 1.2 V 10-b SAR ADCs operating at tens of MS/s with conventional and Vcm-based switching were presented. The linearity behaviors of the DACs switching and structure were analyzed and verified by both simulated and measured results. The Vcm-based switching technique provides superior conversion linearity when compared with the conventional method because of its array's capacitors correlation during each bit cycling. The proposed code-randomized calibration can eliminate the large DNL and INL errors in the conventional switching. Measured results demonstrated that both higher speed and lower power is achieved by using Vcm-based switching.

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