



Implementation of Averting Saturation from Series Transformers by using Dynamic Voltage Restorer Systems

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Abstract- *In this paper a method to prevent saturation in series transformer from DVR is presented. Power quality has been an issue that is becoming increasingly pivotal in modern industrial and commercial applications. Voltage disturbances especially the voltage sag and swell are the most common power quality problems due to increased use of a large numbers of sophisticated and sensitive electronic equipment in industrial systems. The method consists in correcting the voltage which is injected through the transformers into the power system to compensate voltage sags. To overcome this problem, custom power devices are used. One of the devices is the Dynamic Voltage Restorer (DVR), which is the most efficient and effective modern custom power device used in power distribution networks. It is a series connected power electronic based device that can quickly mitigate the voltage sags in the system and restore the load voltage to the pre-fault value. Moreover, the technique allows a certain level of sag compensation even when the estimated flux is expected to exceed the saturation limit. The voltage sag level and phase are computed through an adaptive Recursive Least Squares (RLS). In RLS Method we have to use 4-leg voltage source inverter and it can be slow process to compensate the voltage sag occur in the power system. The performance of the system can be evaluated by using MATLAB/SIMULINK software.*

Keywords: *Dynamic Voltage Restorer (DVR), Recursive Least Squares (RLS), Saturation, Series Transformers, Voltage Sag, 4-leg voltage source inverter.*

I. INTRODUCTION

Power quality is a very important issue due to its impact on electricity suppliers, equipment manufactures and customers. "Power quality is described as the variation of voltage, current and frequency in a power system. It refers to a wide variety of electromagnetic phenomena that characterize the voltage and current at a given time and at a given location in the power system" [1]. Both, electric utilities and end users of electrical power are becoming increasingly concerned about the quality of electric power. Sensitive loads such as computers, programmable logic controllers (PLC), variable speed drives (VSD)-etc. need high quality supplies [2]. Power quality is an umbrella concept for multitude of individual types of power system disturbances. Power distribution systems, should ideally

provide their customers with an uninterrupted flow of energy with a smooth sinusoidal voltage at the contracted magnitude level and frequency [3]. However, in practice, power systems, especially distribution systems, have numerous nonlinear loads, which significantly affect the quality of the power supply. As a result of these nonlinear loads, the purity of the supply waveform is lost in many places. This ends up producing many power quality problems [4-6]. An important percentage of all power quality problems are of the voltage -quality type where what matters is the deviation of the voltage waveform from its ideal form. The best known disturbances of the voltage waveform are voltage sags and swells, harmonics, interharmonics and voltage imbalances. Voltage Sag: A Voltage Sag is a momentary decrease in the root mean square (RMS) voltage between 0.1 to 0.9 per unit, with a duration ranging from half cycle up to 1 min. It is considered as the most serious problem of power quality. This study introduces various power quality problems and basic concept of dynamic voltage restorer [7]. This study deals with overview of a Dynamic Voltage Restorer (DVR) for mitigation of voltage sags.

A power electronic converter based series compensator that can protect critical loads from all supply side disturbances other than outages is called a dynamic voltage restorer. The restorer is capable of generating or absorbing independently controllable real and reactive power at its AC output terminal. This device employs solid-state power electronic switches in a pulse-width modulated (PWM) inverter structure. It injects a set of three phase AC output voltages in series and synchronously with the distribution feeder voltages [8]. The amplitude and phase angle of the injected voltages are variable thereby allowing control of the real and reactive power exchange between the device and the distribution system. The DVR functions by injecting three single phase AC voltages in series with the three phase incoming network voltages during a dip, compensating the difference between faulty and nominal voltages. All three phases of the injected voltages are of controllable amplitude and phase. Voltage source inverter fed from the DC link supply the required active and reactive power [9].

The scheme consists in correcting the voltages which are injected through the transformers into the power system to compensate voltage sags. It restricts the compensating voltages during the sag whenever it predicts that a maximum limit for the flux linkage is about to be exceeded. The prophecy is carried out at the beginning of a stabilized voltage sag. Furthermore the method allows a certain level of sag compensation even when the predictable flux is expected to exceed the saturation limit. The voltage sag level and phase are computed through an adaptive recursive least squares (RLS). The RLS evaluation incorporates a transient period before it attains a steady state whenever there is a sag occurrence [10].

During the transient period at the start of a voltage sag, a DVR injection transformer can experience a flux-linkage that is up to twice its nominal steady-state value. In order to prevent the transformers from saturating it is normal to choose a rating flux that is double that of the steady-state limit. An alternative method is to limit the flux-linkage during the transient switch-on period, thus preventing saturation. It is shown through both simulation and experimental results that an adaptive form factor can be applied to the DVR injected voltage, which minimizes the disturbance seen by a sensitive load, while at the same time preventing saturation. The proposed method removes the need for rating the series injection transformers for the DVR transient switch-on period, and therefore removes the redundancy normally associated with their steady state operation. In economic terms, this may reduce the total cost of a DVR system, thus making it a more attractive solution for voltage sag mitigation [11].

II. METHOD FOR CONTROLLING SATURATION

This section devises the method of controlling saturation proposed in this paper. The fundamental idea is to constrain the compensating voltage by multiplying it by a form factor. In order to accomplish such a goal, one must predict, at the moment of the sag detection, the value for the form factor to be applied up to the end of the next half cycle (or the next whole cycle) of the compensating voltage after the sag detection and keep the flux at its limit value. In general, V_c can be described as

$$v_c(t) = V \cos(\omega t + \alpha) \quad (1)$$

Where ω and α are, respectively, the fundamental frequency and the initial phase of the compensating voltage. By Faraday's law, the linked flux in the transformer's core at a given instant t can be expressed by

$$\lambda = \int_0^t V \cos(\omega \tau + \alpha) d\tau \quad (2)$$

Solving (2) and assuming that the transformer is demagnetized, that is, $\lambda_{\text{max}}=0$ at the $t=0$, the following expression for the flux is obtained:

$$\lambda = (V/\omega)[\sin(\omega t + \alpha) - \sin(\alpha)] \quad (3)$$

The first part of (3) represents the ac component of the flux, while the second one is its dc component. Whenever the injected voltage started at a zero cross, that is, the peak of the flux reaches its maximum value. For instance, if the expression for the flux is given by

$$\lambda = (V/\omega)[\cos(\omega t) + 1] \quad (4)$$

The technique proposed in this paper is inspired by the one described. Consider Fig. 2, where the injected voltage starts at angle α . It is possible to predict the maximum excursion for the flux linkage through the following integration:

$$\lambda' = \int_{\alpha/\omega}^{(\pi/2)/\omega} V \cos(\omega t) dt + \xi \int_{(\pi/2)/\omega}^{(3\pi/2)/\omega} V \cos(\omega t) dt \quad (5)$$

Where ξ is a form factor which is first set to unity. Note that between α and $\pi/2$, the injected voltage contributes positively to the flux. Between $\pi/2$ and $3\pi/2$, the voltage contributes negatively to the flux. Therefore, in the situation depicted in Fig. 2, at the angle α , the flux reaches its minimum value. If the module of the prediction provides a value higher than the allowed limit for the transformer, then the parameter must be adjusted to a value which restricts the amplitude to be equal to the lower limit.

$$\xi = \frac{-\lambda_{\text{max}} - V \int_{\alpha/\omega}^{(\pi/2)/\omega} \cos(\omega t) dt}{V \int_{(\pi/2)/\omega}^{(3\pi/2)/\omega} \cos(\omega t) dt} \quad (6)$$

Applying the factor, computed through (6), to the compensating voltage during its negative semi cycle, ensures that the flux will not surpass the minimum limit. When the injected voltage starts within a negative semicycle, at the point, is predicted through

$$\lambda' = \int_{\alpha/\omega}^{(3\pi/2)/\omega} V \cos(\omega t) dt + \xi \int_{(3\pi/2)/\omega}^{(5\pi/2)/\omega} V \cos(\omega t) dt \quad (7)$$

If, the injected voltage is required to be scaled by the form factor computed by

$$\xi = \frac{\lambda_{\max} - V \int_{\alpha/\omega}^{(3\pi/2)/\omega} \cos(\omega t) dt}{V \int_{(3\pi/2)/\omega}^{(5\pi/2)/\omega} \cos(\omega t) dt} \quad (8)$$

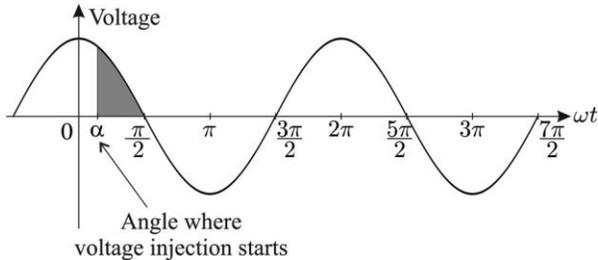


Fig. 2. Compensating voltage for one of the phases.

It must be noted that the procedure described before only shifts the flux curve so that, up to end of the semi cycle, subsequently after the start of the voltage injection, its value is not higher than the transformer's flux limit. It still remains a dc component which can cause the flux value to surpass the allowed limit within the subsequent opposite semi cycle. Therefore, in the proposed method, the condition

$$|\lambda_{\max}| \leq |V/\omega| \quad (9)$$

must be verified. Note that V is the peak value for the compensating voltage. If the condition (9) is not observed, the compensating voltage must be computed as

$$v_c(t) = \frac{V_{\max}}{2} \cos(\omega t + \alpha), \text{ for } \alpha \leq \omega t \leq \alpha + \pi/2 \quad (10)$$

Where $V_{\max} = \lambda_{\max}\omega$.

The method implementation is carried out in such a manner that, whenever the initial phase is detected within the interval from $3\pi/2$ up to 2π , it must be subtracted by 2π . This is necessary because the RLS algorithm computes α ranging from 0 up to 2π and leaves out the interval $-\pi/2$ up to 0.

In the proposed method, there is a need to compute the amplitude and phase of the compensating voltage. This task is carried out by a recursive least squares method which, for each instant, updates the amplitude and phase estimation. This is discussed in the next section. Furthermore, the DVR voltage correction only takes place in the moment where the estimation for the parameters is stabilized, that is, during the estimation transient when there is no compensating voltage injected into the grid. The proposed method is applied for each one of the three phases, accordingly to the flowchart depicted in Fig. 3.

III. COMPENSATING VOLTAGE CONSTRUCTION

The compensating voltage construction applied in this paper makes use of an RLS algorithm which computes the amplitude and the phase for each sample of the grid voltage. The RLS algorithm is applied for each one of the three grid phases. It is worth emphasizing that the DVR is not meant to compensate the voltage while the RLS estimation is in its transient period. Therefore, in this paper, a method is proposed for flagging whether the RLS estimation is stable. The next subsection is dedicated to explain the RLS algorithm used in this paper. The following one outlines the procedure in which the compensating voltage is only injected when the RLS estimation is constant.

A. RLS ESTIMATOR

The Recursive least squares (RLS) is an adaptive filter which recursively finds the coefficients that minimize a weighted linear least squares cost function relating to the input signals. This is in contrast to other algorithms such as the least mean squares (LMS) that aim to reduce the mean square error. In the derivation of the RLS, the input signals are considered deterministic, while for the LMS and similar algorithm they are considered stochastic. Compared to most of its competitors, the RLS exhibits extremely fast convergence. However, this benefit comes at the cost of high computational complexity.

To model voltages acquired from power systems, it is usual to describe them as a sum of sinusoids, with one being the fundamental, and the others being harmonics. If the voltage is corrupted by harmonics, this representation ensures that the dynamics of the harmonics do not contaminate the parameters estimation related to the fundamental sinusoid. Hence, denoting the data of voltages by V_g , the model \hat{v}_g is a sum of p sinusoids provided by

$$\hat{v}_g(n\Delta t) = \hat{v}_g[n] = \sum_{m=1}^p (V_{Gm} \cos(m\omega_0 n\Delta t + \alpha_m)) \quad (11)$$

Where V_{Gm} and α_m are, respectively, the amplitude and the phase of the sinusoid of $m\omega_0$ frequency, and n is the time index. The time interval Δt is the sampling period. Its selection does not interfere with the RLS performance once the Nyquist criterion is observed. The first of the p sinusoids is related to the fundamental phasor.

$$\hat{v}_g[n] = \sum_{m=1}^p [V_{Gm}^c \cos(m\omega_0 n\Delta t) - V_{Gm}^s \sin(m\omega_0 n\Delta t)] \quad (12)$$



or equal to a given limit L immediately after a sag detection, one can ensure that the RLS estimation for the parameters, that is, the amplitude and phase of the sag, has passed its transition time.

For each voltage sample, the RLS algorithm computes the phase α_1 and the amplitude V_{G1} which is provided to the constant level detector. This detector sets a flag signal to 1 whenever the parameters estimation is stable. On the instant that the parameters start changing, the RLS sets the flag signal to 0. Therefore, the flag signal can be used as an enable signal to the DVR action. The compensating voltage v_c is injected by the DVR as

$$v_c(n\Delta t) = \begin{cases} V \cos(\omega n\Delta t + \alpha_1), & \text{if flag} = 1, \\ 0, & \text{if flag} = 0 \end{cases} \quad (25)$$

Where V is the difference between a reference value V_{ref} and the estimated V_{Gm} .

The constant level detection procedure imposes the sampling rate to be fast enough so that a given constant level is detected with no critical delay in comparison with the fundamental cycle. In the simulations and experiments, the sampling frequency has been set in 10 kHz and the moving average M has been carried out with five samples.

IV. CONTROL OF 4-LEG VSI CONTROLLER

Four-leg voltage source inverters are more advantageous than 3-leg voltage source inverters in such a way by the greater utilization of DC link voltage, independency of the modulation factor of load current and avoidance of superposition of a DC component with the AC output voltage. Four-leg voltage source inverters require a balanced sinusoidal output voltage for supplying unbalanced and/or nonlinear loads. This requirement is satisfied with the help of Pole Placement Control technique via state feedback in this work. The proposed method is found to be effective in achieving an accurate adjustment of the transient performance of the 4-leg voltage source inverter and in tracking its reference input under steady state conditions. A settling time of 0.58ms is achieved. Also the performance of the proposed controller is compared with that of PI, PID, LQR and State Feedback with Integral Control.

Power quality is a term used to broadly encompass the entire scope of interaction among electrical suppliers, the environment, the system and the products. The widespread use of non-linear loads is leading to a variety of undesirable phenomena in the operation of power systems. The harmonic components in current and voltage waveforms are the most important among these. Conventionally passive filters have been used to eliminate line current harmonics. Current controlled voltage source inverters can be utilized with appropriate control strategy to perform active filter functionality. However, the extensive use of power electronics based equipment and non-linear loads at PCC generate harmonic currents, which may deteriorate the

quality power. Recently various control strategies for grid connected inverters incorporating PQ solution. In an inverter operates as active inductor at a frequency to absorb the harmonic current. A similar approach in which a shunt active filter acts as active conductance to damp out the harmonics in distribution network is proposed. But the exact calculation of network inductance in real-time is difficult and may deteriorate the control performance. Generally current controlled voltage source inverters are used because of their faster response compared to voltage controlled voltage source inverters as its power is controlled by switching instant. And also in current controlled voltage source inverters active and reactive power is controlled independently.

This suggests a new method that consists of four leg current controlled voltage source inverter that is capable of compensating problems like power factor, current unbalance and current harmonics. In three-phase three leg topology the zero sequence currents in the load cannot be compensated and hence the zero sequence currents flow in the neutral wire (Between the system and load). The zero sequence currents thus return to the ac distribution system. If the load is nonlinear and contain harmonics then these harmonics also enter ac system thus degrading the power quality. In three phase application with three leg inverter, if the load requires a neutral point connection a simple approach is to use two capacitor to split the dc link and tie the neutral point to the midpoint of two capacitors. In this case the unbalanced loads will cause the neutral currents that flow through the fourth wire distorting the output voltage. Another drawback is the need for excessively large dc link capacitors. In a control strategy based on p-q theory is proposed where load current and inverter current sensing are required to compensate load harmonics.

The widespread increase of non-linear loads nowadays, significant amounts of harmonic currents are being injected into power systems. Harmonic currents flow through the power system impedance, causing voltage distortion at the harmonic currents' frequencies. The distorted voltage waveform causes harmonic currents to be drawn by other loads connected at the point of common coupling (PCC). The existence of current and voltage harmonics in power systems increases losses in the lines, decreases the power factor and can cause timing errors in sensitive electronic equipment's. The harmonic currents and voltages produced by balanced 3-phase non-linear loads such as motor drivers, silicon controlled rectifiers (SCR), large uninterruptible power supplies (UPS) are positive-sequence harmonics (7th, 13th, etc.) and negative-sequence harmonics (5th, 11th, etc.). However, harmonic currents and voltages produced by single phase non-linear loads such as switch-mode power supplies in computer equip- *Corresponding author. Currents unlike positive and negative-sequence harmonic currents do not cancel but add up arithmetically at the neutral bus. This can result in neutral current that can

reach magnitudes as high as 1.73 times the phase current. In addition to the hazard of cables and transformers overheating the third harmonic can reduce energy efficiency. The traditional method of current harmonics reduction involves passive LC filters, which are its simplicity and low cost. However, passive filters have several drawbacks such as large size, tuning and risk of resonance problems. On the contrary, the 4-leg APF can solve problems of current harmonics, reactive power, load current balancing and excessive neutral currents simultaneously, and can be a much better solution than conventional approach.

V. SIMULATION RESULTS

The figure 4 shows simulation Diagram of the DVR system of the proposed methodology. Three different scenarios of voltage sags have been simulated.

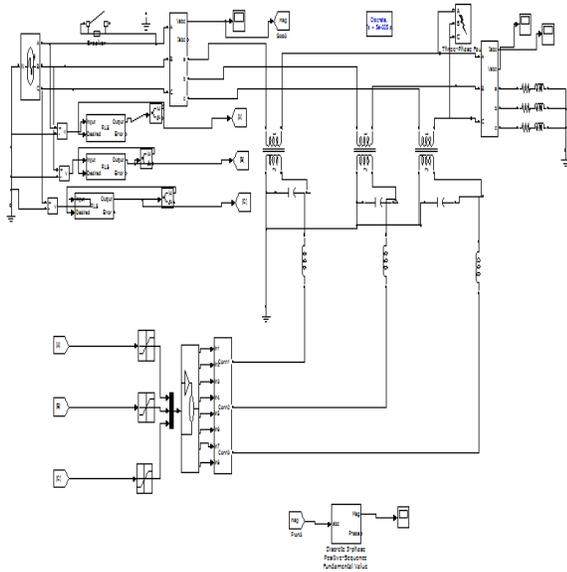


Fig 4 Simulation Diagram of the DVR system.

Case I:

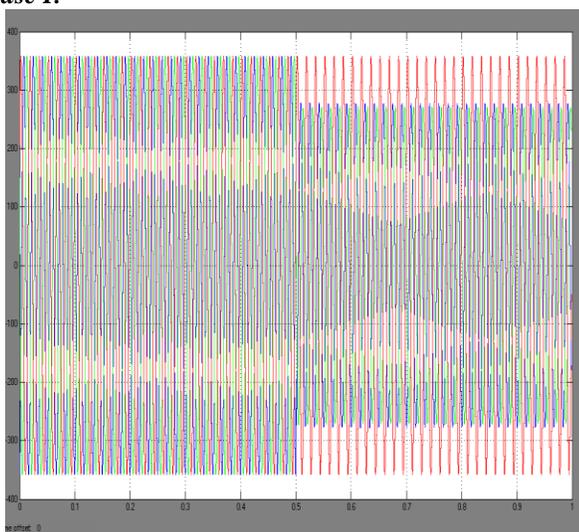


Fig. 5 Voltage sag on phase A

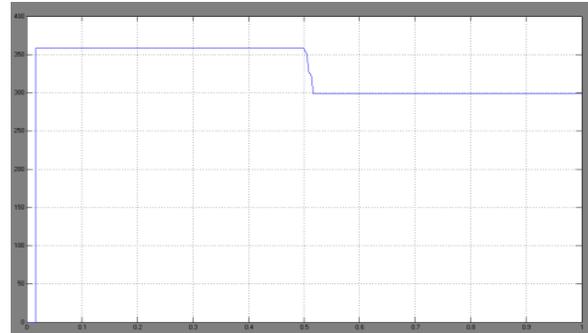


Fig. 6 Amplitude estimation of phase-A.

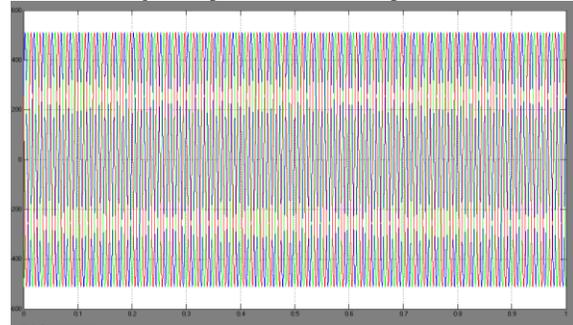


Fig. 7 Load voltage of DVR

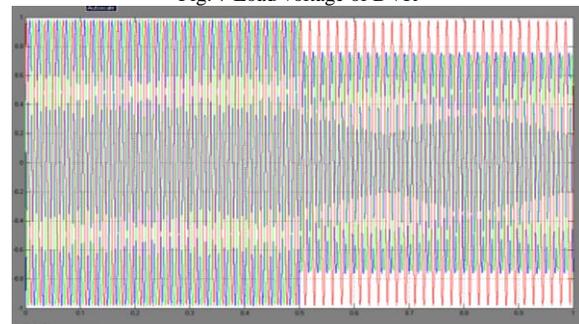


Fig. 8 Load current of DVR

Case I shows the simulation results of DVR, in this case consider that a three-phase grid is under a phase-to-phase sag during 58 ms, figure 5 shows the least-squares amplitude estimation for phase-A. In figure 6 We can highlight four instants. The first two are related to the beginning of the sag and the last two are associated with the end of the sag. Recall that the compensating voltage is not triggered while the amplitude and phase are varying. Fig. 7 shows The load voltage.

Case II:

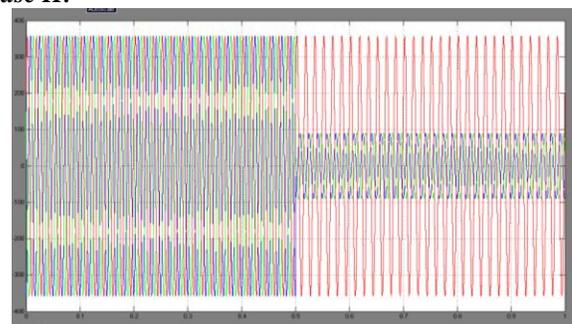


Fig. 9 Voltage sag on phase A

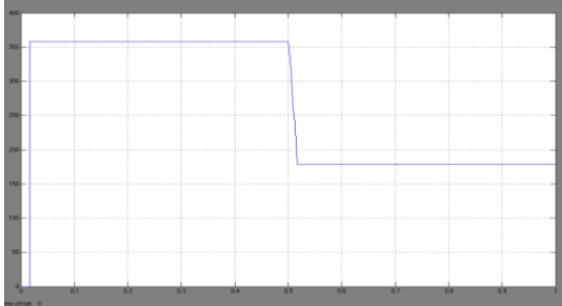


Fig. 10 Amplitude estimation of phase-A.

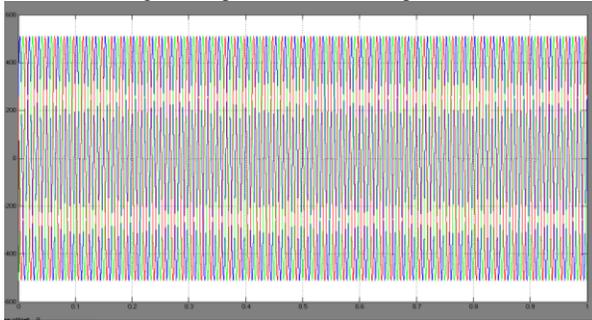


Fig.11 Load voltage of DVR

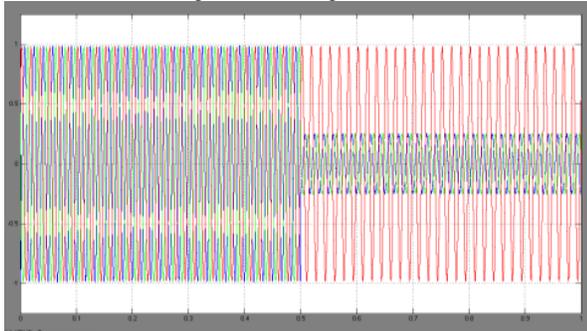


Fig.12 Load current of DVR

In Case II the voltage sag is depicted, Fig 9 shows a phase-to-phase fault for an angle α is different from the previous one. Fig 10 shows the amplitude estimation carried out by the least-squares algorithm for phase-A. Fig 11 shows the voltages applied to the load.

Case III:

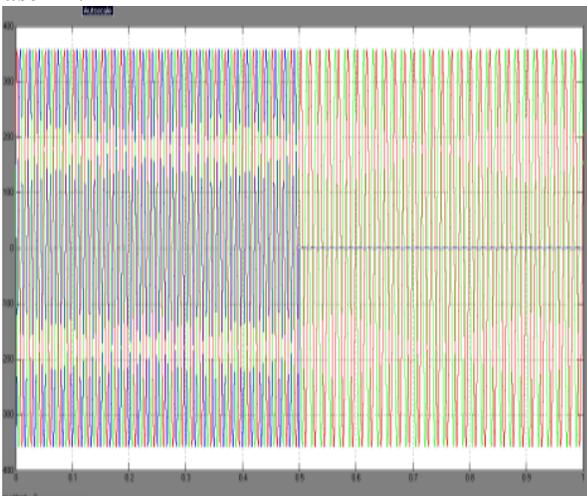


Fig.13 Voltage sag on phase A

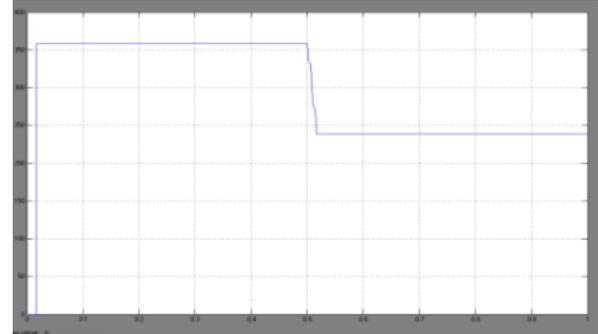


Fig.14 Amplitude estimation of phase-A.

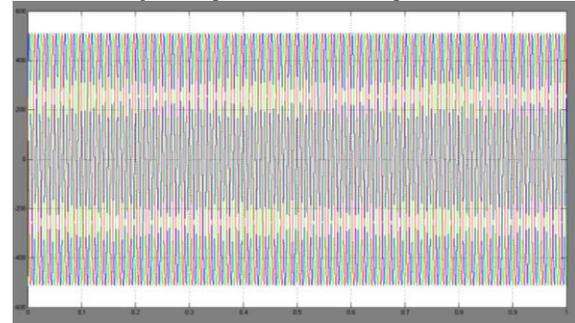


Fig.15 Load voltage of DVR

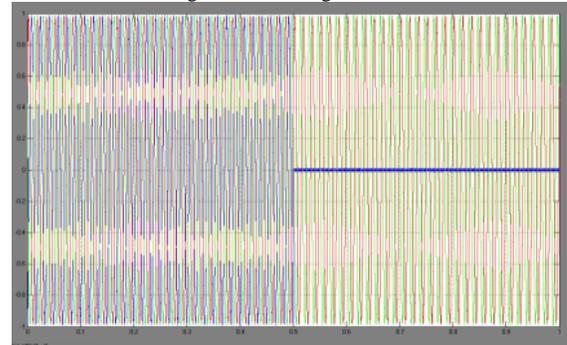


Fig.16 Load current of DVR

In Case III the third case simulates a sag for single phase, figure 13 shows voltage sag on phase-A. Figure 14 shows the RLS amplitude estimation for the sagged phase voltage, and figure 15 shows the voltages applied to the load.

VI. CONCLUSION

This paper has proposed a method to Prevent Saturation in Series Transformers from Dynamic Voltage Restorer (DVR) Systems. The DVR system makes use of an RLS algorithm to compute the compensating voltage. The method relies on the correct computation of the compensating voltage phasor which is constrained whenever it can provoke saturation. The compensation is never rendered while the RLS amplitude phasor estimation is varying. Hence, the RLS algorithm is combined with a technique for detecting whether the estimation for the amplitude reached a constant value. This ensures that the compensating voltage is always at a proper level. In some cases, this is performed at a cost of



not completely compensating the sag for a certain period of time. The technique allows a certain level of sag compensation even when the estimated flux is expected to exceed the saturation limit. The voltage sag level and phase are computed through an adaptive recursive least squares (RLS). The RLS estimation incorporates a transient period before it achieves a stable state whenever there is a sag event. The DVR is not supposed to operate in this period. Therefore, this paper also outlines a simple procedure for detecting the RLS estimation stable level.

REFERENCES

- [1] Shazly A. Mohammed, Aurelio G. Cerrada, Abdel-Moamen M. A. and B. Hasanin, "Dynamic Voltage Restorer (DVR) System for Compensation of Voltage Sags, State-of-the-Art Review" International Journal Of Computational Engineering Research (ijceronline.com) Vol. 3 Issue. 1.
- [2] Shailesh M. Deshmukh, Bharti Dewani, "Overview of Dynamic Voltage Restorer (DVR) for Power Quality Improvement" (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 6, November- December 2012, pp.1372-1377.
- [3] Fitzer, Chris; Arulampalam, Atputharajah; Barnes, Mike; Zurowski, Rainer, "Mitigation of saturation in dynamic voltage restorer connection transformers" IEEE Transactions on Power Electronics, Vol. 17, No. 6, 11.2002, p. 1058-1066.
- [4] Y.-H. Chen, C.-Y. Lin, J.-M. Chen, and P.-T. Cheng, "An inrush mitigation technique of load transformers for the series voltage sag compensator," IEEE Trans. Power Electron., vol. 25, no. 8, pp. 2211–2221, Aug. 2012.
- [5] R. H. G. Tan and V. K. Ramachandramurthy, "Voltage sag acceptability assessment using multiple magnitude-duration function," IEEE Trans. Power Del., vol. 27, no. 4, pp. 1984–1990, Oct. 2012.
- [6] M. A. Mora and J. V. Milanovic, "Monitor placement for reliable estimation of voltage sags in power networks," IEEE Trans. Power Del., vol. 27, no. 2, pp. 936–944, Apr. 2012.
- [7] J. Roldán-Peréz, A. García-Cerrada, J. L. Zamora-Macho, P. Roncero-Sánchez, and E. Acha, "Troubleshooting a digital repetitive controller for a versatile dynamic voltage restorer," Elect. Power Energy Syst., vol. 57, pp. 105–115, May 2014.
- [8] P. Kanjiya, B. Singh, A. Chandra, and K. A.-. Haddad, "SRF theory revisited to control self-supported dynamic voltage restorer (DVR) for unbalanced and nonlinear loads," IEEE Trans. Ind. Appl., vol. 49, no. 6, pp. 2330–2340, Dec. 2013.
- [9] S. R. Naidu and D. A. Fernandes, "Dynamic voltage restorer based on 4-leg voltage source converter," IET Gen. Transm. Distrib., vol. 3, no. 5, pp. 437–447, May 2009.
- [10] T. Jimichi, H. Fujita, and H. Akagi, "A dynamic voltage restorer equipped with a high-frequency isolated dc-dc converter," IEEE Trans. Ind. Appl., vol. 47, no. 1, pp. 169–175, Jan. 2011.
- [11] F. B. Ajaei, S. Farhangi, and R. Iravani, "Fault current interruption by the dynamic voltage restorer," IEEE Trans. Power Del., vol. 28, no. 2, pp. 903–910, Apr. 2013.