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Design of low Power and low latency hybrid scheme for network on chip Design

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Abstract: Network-on-chip (NoC) has emerged as a scalable and promising solution to global communications within large multi core systems. The NoC with virtual point-to-point connections (VIP)is the existing, the proposed hybrid scheme can reduce the latency along with the power. A path allocation algorithm is proposed in this paper to determine VCS connections and circuit-switched connections on a mesh connected NoC, such that both communication latency and power are optimized. A novel switching mechanism, called virtual circuit switching, is proposed to intermingle with circuit switching and packet switching. Flits travelling in virtual circuit switching can traverse the router with only one stage. In addition, multiple virtual circuit-switched (VCS) connections are allowed to share a common physical channel

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1. INTRODUCTION

A bus arbiter controls access to the shared resource by granting access to only one of the several requesting masters. There are several disadvantages associated with these kind of communication architectures. Both point-to-point as well as bus based communication schemes are not very scalable and cannot efficiently handle the communication requirements of modern SoC architectures. The performance of a bus degrades as the number of requestors connected to the bus increases. This can be attributed to the fact that the bandwidth of the communication channel is shared among all the bus requestors. This results in the serialization of the requests to the bus, thus increasing communication latencies. Also, the complexity and the delay of the arbiter increases as the number of requestors to the bus increases. Technology scaling has caused wire delay to become a dominant component of the overall clock cycle time [1]. Long wires in point-to-point links as well as buses result in increased delays and are susceptible to noise. Hence, on-chip communication using these schemes is becoming expensive in terms of both power as well as speed in the era of deep-submicron technologies (DSM).

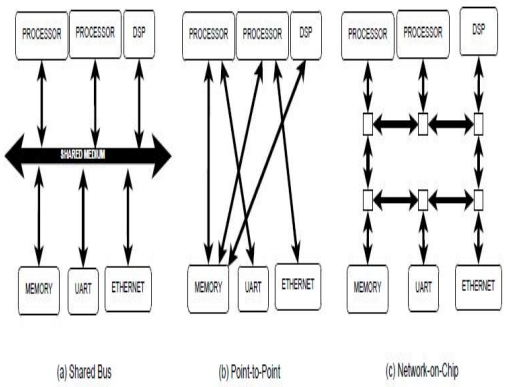


Fig: 1 bus, point to point, NoC communication

The NoC is a highly scalable packet based communication architecture that over- comes the disadvantages of the bus based communication systems. Table I compares the bus based and No based on-chip communication schemes and has been adapted from You et al. . NCOs help to accomplish the transfer of maximum amount of information between communicating nodes within the least possible time. NCOs consist of routing elements connected by small point-to-point links forming a data routing network on chip.

Unlike bus architectures, where the bus is occupied by one source node during the entire message transaction, the use of packet based communication in No allows for sharing of the links between various communicating nodes. This increases throughput and reduces communication latencies. No can be easily scale by connecting additional routing elements to the existing network. The aggregate bandwidth of the network scales with increasing network size. NCOs support design reuse as the same routing element can be used to scale the No to higher dimensions. This reduces the time-to-market and validation costs. Thus, NCOs offer a highly ancient communication infrastructure for modern day SoC and Multi core architectures. Figure 1 shows some examples of bus, point-to-point and No based communication architectures.

C. NoC Architecture and Components

A No consists of routing nodes spread across an entire chip connected together by communication links A brief description of the various components of the No is provided below. Processing Elements (PEs) are the computational elements of the chip. These can be general purpose processor cores, digital signal processing cores, arithmetic logic units, memory cores or any other specialized IP cores. They are the source and the sink for all the data in the on-chip communication network. Network Interfaces (NIs) connect the processing elements to the main on-chip communication network. They decouple the

Computational elements from the communication infrastructure. NIs convert the messages generated by the PEs into packets and insert additional routing information based on the architecture of the under

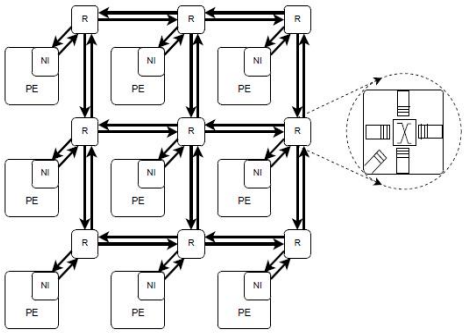


Figure:2 NoC Architecture

lying network. Packets are decomposed into smaller units called flow control units or its which are transmitted over the network. Flits are further classified as head, body and tail its. The head it carries the routing information required to route the packet to its destination. The head it allocates resources for the entire packet as it traverses from so urce to destination. The body and tail its carry only the packet payload with no routing information and follow the head it through the network. The tail it de-allocates the resources which have been allocate d to the packet by the
head it. Routing Nodes are the heart of the communication network.

They route the packets onto the appropriate link so that they can reach the intended destination. Routing protocols in conjunction with the routing information in the packet header are used to make routing decision at each routing node. Channels or Links connect the routing nodes in an Two links are present between any two routers in the network, one each for data transmission in each direction. Links provide the bandwidth required for data transmission. In addition to the data transmission links, additional links required for control may also be present.

Figure 2 depicts these component s for a 4x4 NoC where the routing nodes connected as a grid.
Network topology refers to the static arrangement of routing nodes and links in an interconnection network. Selection of a good topology is essential to minimize the communication latency an d maximize the bandwidth. The routing and the flow control schemes are heavily dependent on the type of the topology selected. Topologies can be classified into two categories: regular topologies and irregular topologies The most commonly used type of regular topology is the k array n-cube . This topology consists of N = k N nodes arranged as a regular n dimensional grid with k nodes in each dimension connected by a pair of communication links, one in each direction. Each of the nodes can act as an input or an output or a routing node. The most commonly used versions of the k-ary n-cube are the torus and mesh net-works. Torus networks possess edge symmetry.

II. PROPOSED HYBRID SCHEME BASED ON VIRTUAL CIRCUIT SWITCHIN

The basic principle of the proposed hybrid scheme is that VCs are exploited in virtual circuit switching to form a number of VCS connections and multiple VCS connections can share a common physical channel. In this hybrid scheme, VCS connections cooperate with PS

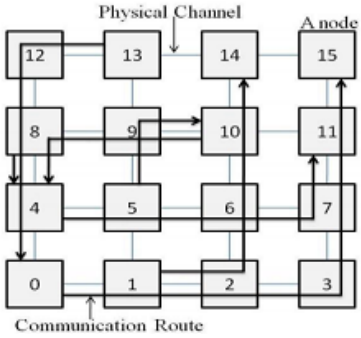


Fig.2 Simple traffic with communication routes in a 4 × 4 mesh.

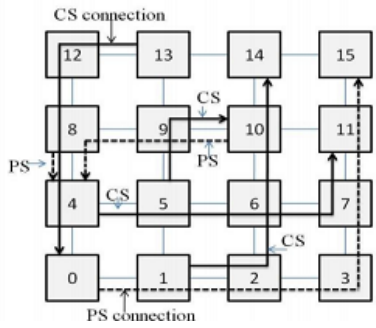


Fig.3. CS and PS connections of the conventional hybrid scheme

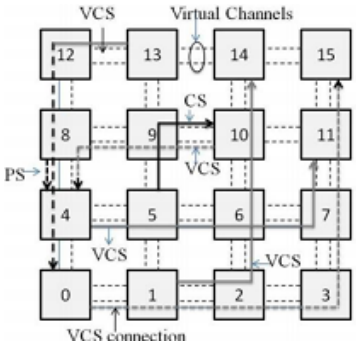


Fig.4. VCS, CS, and PS connections of the proposed hybrid scheme

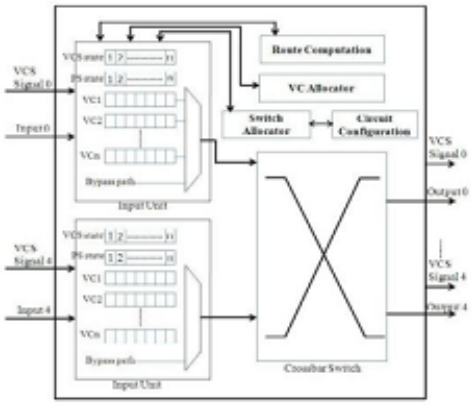


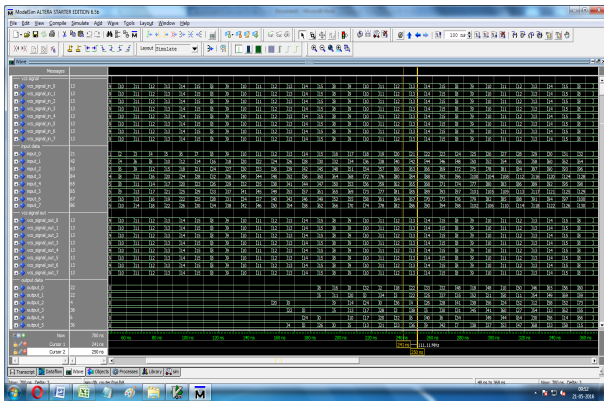
Fig. 5 Router Architecture

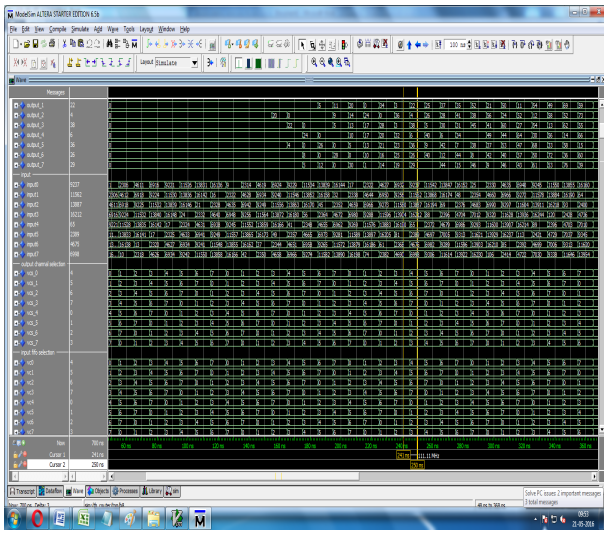
and CS connections at the same time, modified router architecture with five ports is proposed, as shown in Fig. 5. Compared with the baseline router [12], the additional hardware of the proposed router includes the bypass path, the circuitconfiguration, and the VCS state.

First, the bypass path is added in each input unit for allowing flits to go directly to the crossbar switch. Second, each input unit contains a PS state and a VCS state. The PS state corresponds to the VC state of the baseline PS router, and the VCS state is used to support VCS connections. Third, the circuit configuration unit is to store the interconnect information for CS connections. In this paper, both the PS and the VCS states have n fields corresponding to n VCs. First, the VCS signal is only issued when crossbar switches of the VCS connection wait to be preconfigured. Due to the low activity of VCS signal, the power overhead caused by VCS signal can be much less than the power saving by bypassing buffer writing, routing, and arbitration of routers. Second, in the network with two VCs, the width of VCS signal is 2 bits in Virtual Circuit Switching. The proposed hybrid scheme supports the interweaving of packet switching, circuit switching, and virtual circuit switching. Two extra bits are added to each flit to denote the switching type of the flit. When a flit enters the router, these extra bits are checked at first. Then, the corresponding router pipeline is executed according to the switching type of the flit. Operations of circuit switching in this paper are similar to [6]. This section mainly describes operations of virtual circuit switching. Note that VCS connections must be constructed in advance before the flit traveling in virtual circuit switching. Fig. 2 shows an example of traffic, in which physical channels (1, 2), (7, 11), and (8, 4) are shared by more than one communication, respectively. (x, y) denotes the physical channel from node x to node y. Fig. 3 shows CS connections and PS connections after using the conventional hybrid scheme. A CS connection is configured by recording in each router which input port should be connected to which output port. It is composed of physical channels and routers.

However, routers on a PS connection are configured during the (BW, RC, VA, and SA) stages when flits require passing through. A physical channel can be shared by one CS connection and multiple PS connections. Once flits on CS connections arrive at routers, crossbar switches are immediately configured so that the CS flits can bypass directly to the ST stage [4]–[6]. When there is no CS flit, the corresponding ports of crossbar switches are released to PS connections. Fig. 4 shows VCS, CS, and PS connections of the proposed hybrid scheme. A VCS connection comprises VCs and routers that have been configured by recording in each router which input VC should be connected to which downstream VC. Crossbar switches of routers are preconfigured during the SA stage before VCS flits require passing through. Because VCS connections are established over VCs, a physical channel can be shared by *n* VCS connections at most (*n* is equal to the VC number). Other communications competing for that physical channel must be executed in packet switching, such as the communication from node 8 to node 4 in Fig. 4.

OUTPUT WAVEFORMS





CONCLUSION

In this paper, we present a novel hybrid scheme based on virtual circuit switching to further reduce communication latency and power of NoCs. The basic principle of the pro-posed hybrid scheme is to

intermingle virtual circuit switching with circuit switching and packet switching. Intermediate router pipelines are bypassed by establishing VCS connections and CS connections. A path allocation algorithm is also presented to smartly allocate VCS connections and CS connections for a given traffic in mesh-connected NoCs, such that the average packet latency and energy consumption are both optimized.

Our future work will focus on extending the current work to support applications with unpredictable communication pat-terns. Other extensions include the fault tolerance, the quality-of-service (QoS) operation, the multicast delivery service, and the mapping, scheduling of applications based on virtual circuit switching

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