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High Speed Reliable Multiplier Design with Adaptive Hold Logic

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Abstract - Digital multipliers are many of the maximum critical mathematics functional units. The performance of these systems generally depends on the throughput of the multiplier. Whereas, effects in the negative bias temperature stability WDNHV SODFH ZKLOH D S026 WUDQVLVWRU LV XQGHUQHDWK WHUULEOH ELDV 9JV í9GG LQFUHDVLQJ WKH HGJH YROWDJH RI WKH S026 transistor, and decreasing multiplier speed. A comparable phenomenon, positive bias temperature instability occurs while an nMOS transistor is in positive bias. Each consequence degrades the transistor speed, and inside the long term, the device may additionally fail due to timing violations. Consequently, it is crucial to layout dependable high-performance multipliers. On this paper, we suggest an high-speed multiplier design with a AHL circuit. Due to the variable latency multiplier has higher throughput and the AHL circuit degrade overall performance . Moreover, CBM can be used in the proposed structure.

I. INTRODUCTION

The most essential arithmetic partial units of digital multipliers are applicable for fourier transforms, cosine transforms and digital circuits. The overall performance of the entire circuit depends on the throughput of the multipliers, and these multipliers are sluggish.

Negative bias temperature instability happens while a pMOS transistor is underQHDWK WHUULEOH ELDV 9JV í9GG In this case, the interplay between inversion band holes and hydrogen-passivated Si atoms breaks the Si–H layer generated throughout the oxidation manner, generating H or H2 molecules[8]. At the same time as these molecules broadcast away, interface traps are left. The accumulated interface traps between the gate oxide interface and silicon results in higher threshold voltage (Vth),by lowering the circuit switching speed. By the removal of biased voltage, the reverse response takes place, lowering the NBTI effect. However, the reverse reaction does now not put off all of the interface traps generated in the course of the pressure phase, and Vth is expanded in the long time.

By Comparing with the Negative bias temperature instability impact, the Positive bias temperature instability effect is a lot smaller on oxide/polygate transistors, and consequently is commonly not noted. But the Positive bias temperature instability effect can no longer be not noted, for high-ok/metallic-gate nMOS transistors with large charge trapping. In truth, it has been proven that the Positive bias temperature instability effect is more enormous than the Positive bias temperature instability effect on 32-nm high-ok/metallic-gate strategies[8].

Critical path delay is used in Traditional circuits as the general circuit clock cycle so that you can the delay path is shorter than critical path. For non-critical paths, the general cycle period will carry out correctly. However, the critical paths probabilities are activated low. In many of cases, bring about big timing waste by the the use of the critical path delay. Therefore, the variable-latency

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design became proposed to lowering the timing wastage of traditional circuits.

The circuit can be divided into two elements by using the variable latency into design, those elements are (1) shorter paths and (2) longer paths. Short path take single cycle for execution [8]. Two cycles are needed to execute longer paths. Comparing to conventional design, the average latency of variable latency design for shorter paths is high [8].

II.PRELIMINARIES

A. Column_ Bypassing Multiplier

A CB multiplier is an development at the regular array multiplier. The Array multiplier is a parallel multiplier and it acts as a fast multiplier as is shown in the following diagram. In carry save adder (CSA)[8], the multiplier DUUD\ FRQVLVWV RI Qí URZV LQ ZKLFK HDFK URZ FDUULHV Q í ıXOO DGGHU FHOOV (YHU\ IXOO DGGHU LQ WKH FDUU\ VDYH adder array has two outputs: 1) the sum bit goes to lower FA and 2) the carry bit is going to the lower left FA. The final row is a ripple adder for carry propagation[8].

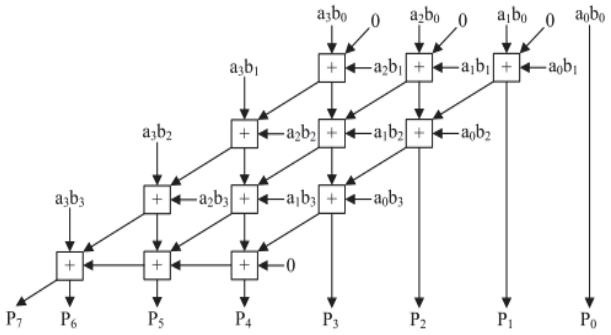

Figure 1. 4 X 4 normal AM.

The input states of the FAs within the AM are usually active regardless. Where in the full adder operations are disabled, a CB multiplier design with low-power is proposed when the corresponding bit in the multiplicand is 0. The following diagram shows the 4×4 CB multiplier. Supposing the inputs are 10102 * 11112, it is able to be visible that for the full adders in the first and third diagonals, two of the three input bits are zero: the carry bit from its upper right full adder and the partial product $a_i b_o$ is consequently, the output of the adders in each diagonals is zero, and the output sum bit is truly same to the third bit, that is the sum output of its upper FA.

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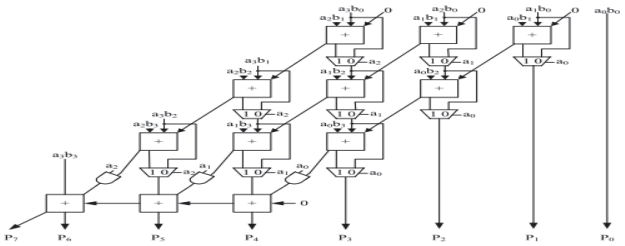

Figure 2. 4 X 4 column_bypassing multiplier

B. Row Bypassing Multiplier

The proposed architecture RB multiplier [6] is used to reduce the power of the Array multiplier. The operation is just like that of the low power CB multiplier, Where multiplicater is used as a selector to know multiplexers and the tri-state gates. The following diagram shows the 4x4 RB multiplier. The multiplier is connected to an FA through a tri-state gate.

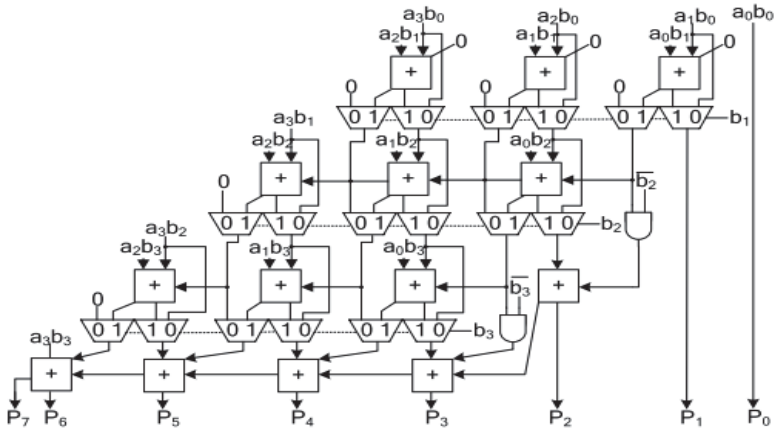

Figure 3. 4 x 4 row bypassing multiplier.

III. PROPOSED HIGH SPEED MULTIPLIER

A. Proposed Architecture

The following diagram shows the proposed structure of high speed multiplier design. Which includes the overall structure and the operation of each components. It includes two m_bit inputs, which are positive numbers and one 2m_bit output, 2m 1_bit Razor flip- flop [7], one CB (or) RB multiplier and an AHL circuit.

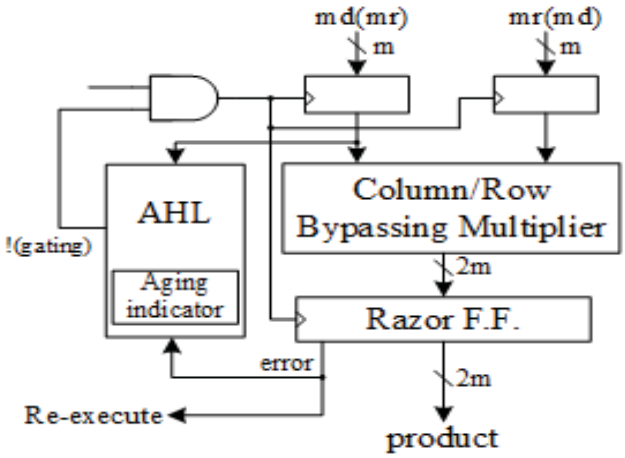

Figure 4. Proposed architecture.

The CB (or) RB multipliers in the proposed structure can be examined whether the number of zeros in either multiplicand or multiplicator to predict this operation and need two cycles or one cycle to complete this process. While the input patters are random, in the multiplicator and multiplicand has number of zeros and ones which follows a normal distribution.

By using the similar architecture two high speed multipliers can be implemented, and the difference between in the two input signals lies in the two bypassing multipliers of the AHL architecture. By considering the bypassing selection in the CB (or) RB multiplier, the input signal of the RB multiplier is the multiplicator, whereas for the CB (or) RB multiplier is the multiplicand .Here the timing violations is detected by using the razor flip-flop and, occur before the input of next pattern arrives.

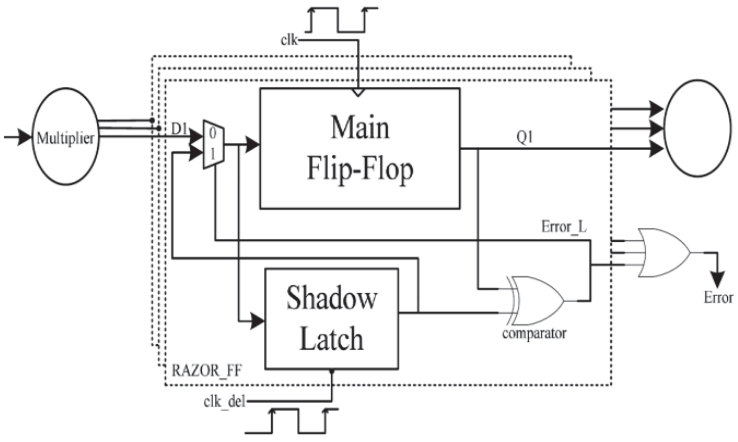

Figure 5. Razor flip-flop.

The above diagram shows the particulars about of razor flip-flop. The above diagram contains multiplexer, flip-flop, shadow latch and xor gate, which is used as a comparator. The execsution result of the combination circuit is given to the main flip-flop by using a normal clock signal, and the shadow latch is consider the delayed clock signal, ,which is slower than the clock signal. The shadow latch has latched bit which is different from the flip-flop, which means path delay of the present operation exceeds the cycle period, than the incorrect result is catched by the main

flip-flop. When error occurs the error signal to one (1) in the razor flip-flop then the system has notify to re-execute the process and the AHL circuit that an error occurred. Here we using to detect an operation require one cycle

pattern or may be two cycles to complete the operation. Whereas the re-execution is costly, but overall cost will low because of using low re-execution frequency. Find out more about razor flip-flop in [7].

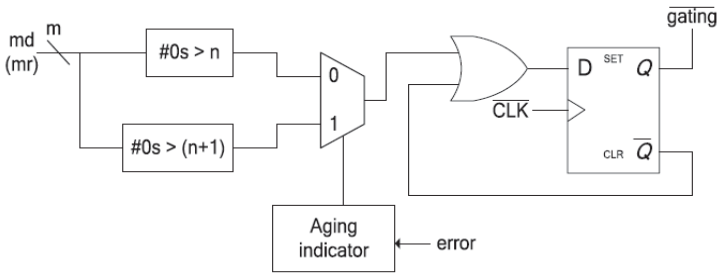

Figure 6. AHL block.

The above diagram shows AHL block which contains aging indicator with an input signal as error signal. AHL block is the key component of the proposed architecture. The above block contains one D-flip-flop, one mux, and with two judging blocks. Here we using aging indicator to count the number of errors by using a simple counter. when the input pattern is too short than the row or CB (or) RB multiplier operation need not complete successfully, occurs timing violations, these timing violations is caught by the razor flip-flop which produces the error signals. When the output signal 1; then the circuit is suffered with sufficient timing violations due to the aging effect. Whereas output is o than the aging effect is not sufficient and no need any actions.

The output of the first judging block in the adaptive hold logic circuit is 1 than the number of zeros in the multiplicand is longer than n, and the output of the second judging block is 1 than the number of zeros in multiplicand is longer than n+1. The input pattern of these two judging blocks are used to employed whether the operation requires two cycles or one cycle, only one will be chosen at a time.

The detail AHL circuit operation explains as shown in below: when an input pattern is given to the both judging blocks,and these judging blocks will decide whether the operation requires two or one cycles to complete both results to the multiplier. The multiplier selects any one of the output result based on aging indicator. In order to determine the input of D flip-flop, the OR operation is performed between the result of multiplexer. When the output of multiplexer is 1 than the pattern requires one cycle. The !(gating) signal is 1 and the input flip flops latches the new data in next cycle. On other side the output of multiplexer is 0, which means that input pattern requires two cycles to complete, the output of OR gate is 0 to the D flip-flop. Whereas the !(gating) signal is 0 to disable the clk signal of input flip flop in next cycle.

The overall explanation of proposed architecture is: when the input pattern is given to the row or CB (or) RB multiplier and to the adaptive hold logic circuit execute simultaneously. The AHL circuit will decide the number of input patterns requires two or one cycles based on number of zeros in multiplicand. When the adaptive hold logic will output 0 to disable clock signal of the flip-flop, then the input pattern requires two cycles to complete. For normal operations the hold logic output is 1. whenever the operation of a CB (or) RB multiplier is completed, the result is given to the razor flip-flop. The razor flip-flop checks that there is a path delay timing violation. When timing violation occur, it means the execution result of multiplier is incorrect than the cycle period is not enough for

the present operation. Thus the razor flip-flop output is error than it notifies that system has to re-executed using two cycles to ensure the operation is correct.

Finally, the one-cycle pattern to minimize performance degradations done using proposed architecture that adjusts percentage of the high speed effect. When the circuit is aged many errors will be occured, the AHL circuit uses the second judging block to decide the input is two cycles or one cycle.

IV. SIMULATION RESULT

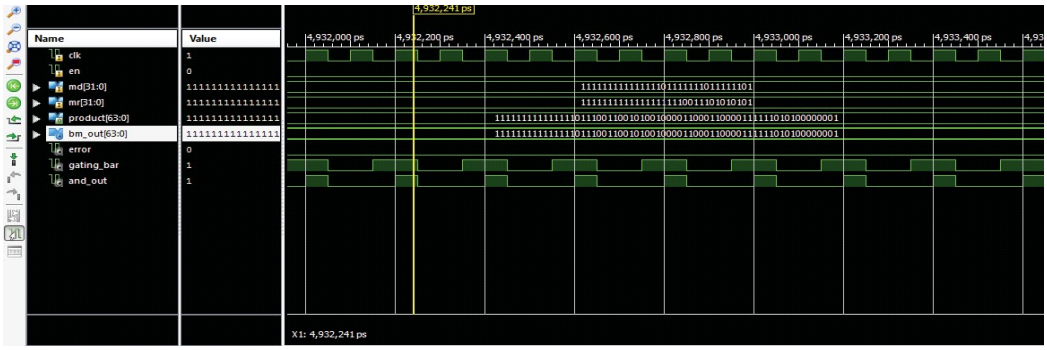

Figure 7.Simulation Results.

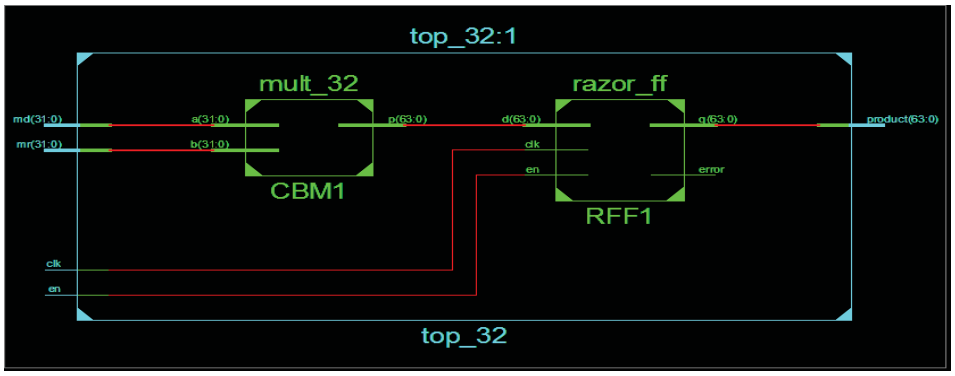

Figure 8.RTL schematic.

Table -1 Experiment Result

	32 X 32 column_bypassing multiplier	16x16 column-bypassing multiplier	8x8 column-bypassing multiplier
Delay	81.854ns	43.589ns	24.957ns
Number of slices	39%	9%	2%
Number of 4-input LUT's	34%	8%	2%
Number of Bonded IOB's	56%	27%	13%

V. CONCLUSION

This paper proposes a high speed variable latency multiplier with AHL. The adaptive hold logic circuit is able to adjust by using the multiplier to less performance degradation due to increase in delay. The practical results show that our proposed architecture with 32x32 multiplications with CB (or) RB multiplier, which results decreases in delay and improves the performance compared with previous designs.

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