Renewable Energy Source micro & smart grid to generate solar wind farm

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Abstract

This paper proposes multilevel topologies based on the concept of nested arrangement. Such topologies are called nested multilevel converters, since the central point of the legs are connected at the same point, with the external legs involving the internal ones. Nested configurations present advantages as compared to the equivalent NPC topologies in terms of reduced number of diodes and consequently higher efficiency. In addition to proposing a new family of power electronics converters, this paper presents an optimized pulse width modulation strategy that allows synthesizing voltage waveforms with higher quality, a losses comparison with the NPC topology, and a general comparison with other topologies proposed in the technical literature. Simulated and experimental results are presented to validate the theoretical expectations.

Keywords: Renewable Energy Source, micro grid, smart grid, solar energy, wind farm.

1. Introduction

MULTILEVEL converters were first conceived for highvoltageand high-power applications. The neutral-pointclamped(NPC) inverter was first proposed in [1]. Since then,many configurations have been proposed [2]–[4] to establishthe highly desirable characteristics for high-power applications,such as reduced waveform distortion and low blocking voltageby switching devices [5]. Besides the NPC, other principal configurationsare flying capacitor, cascade, and modular multilevelconverters [6]–[12].

More recently, the multilevel converters have found acceptancein low-power applications (e.g., in photovoltaic systems[13]–[15]), since it is possible to generate high-quality voltagewaveforms with power semiconductor switches operatingat a frequency near the fundamental [16]. Also, the number ofthe input dc-sources, in this application, is not longer restricted[17]. Even considering just one dc voltage source available, it ispossible to employ multilevel converters with different dc-linksources requirement, as done in [18].

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This paper investigates multilevel topologies based on theconcept of nested arrangement. Such topologies are callednested multilevel converters because the central point of the legsare connected at the same point, with the external leg involvingthe internal one, as observed in Fig. 1. Fig. 1(a)–(c) shows thenested multilevel converter for four-, five-, and six-level outputvoltage, respectively. An auxiliary resonant pole applied to thethree-level nested cell has been considered in [19] and [2].Although the authors in [19] and [2] employ the term nestedtopology, the circuits are different from the topologies presentedin Fig. 1. The five-level converter presented in Fig. 1(b) was proposedby [2]. The main contribution of this paper is to furnish aformal presentation of the nested multilevel configuration fromfour level to *n*-level. When compared to NPC topologies, thestudied configurations can be considered as an interesting optionfor applications that demand a number of levels higher than orequal to four, since as far as the number of levels increase higheris the reduction on the number of diodes employed. Simulatedand experimental results are presented to validate the theoreticalexpectations.

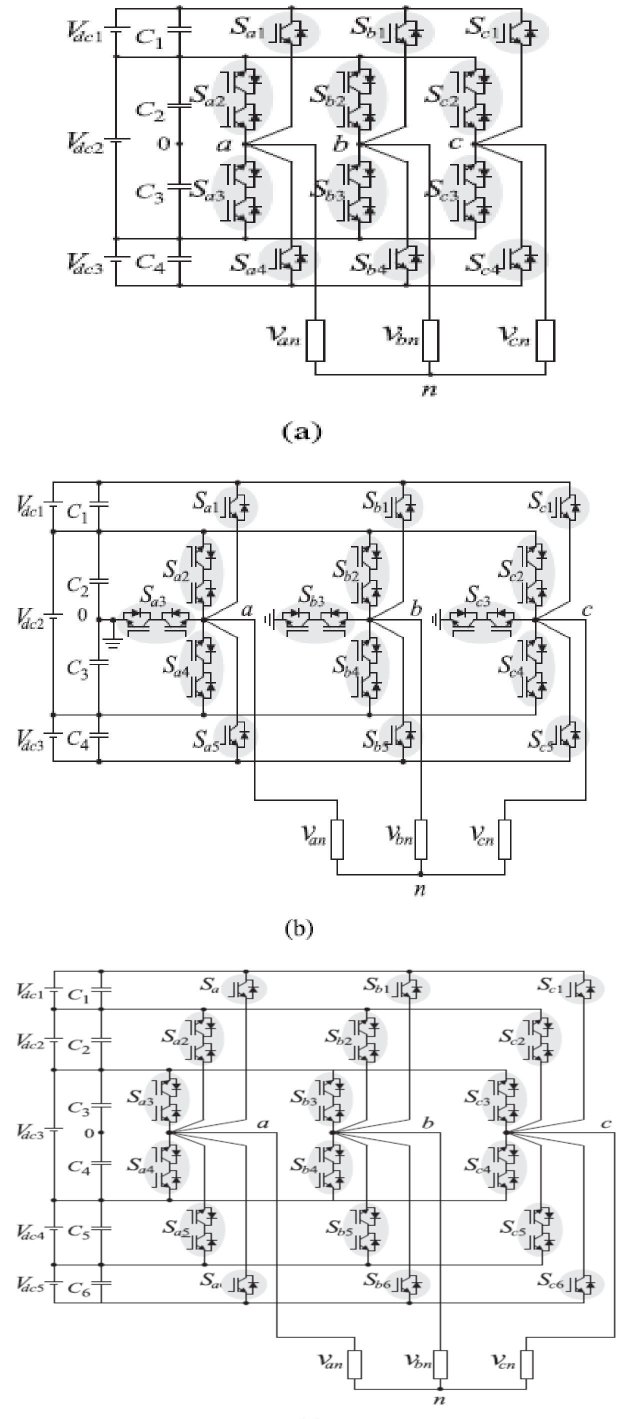

Fig. 1. Nested multilevel configurations with (a) four level, (b) five level, and(c) six level.

2. Related work

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An **inverter** is an electrical device that converts direct current (DC) to alternating current (AC); the converted AC can be at any required voltage and frequency with the use of appropriatetransformers, switching, and control circuits.Static inverters have no moving parts and are used in a wide range of applications, from small switching power supplies in computers, to large electric utilityhigh-voltage direct currentapplications that transport bulk power. Inverters are commonly used to supply AC power from DC sources such as solar panels or batteries.

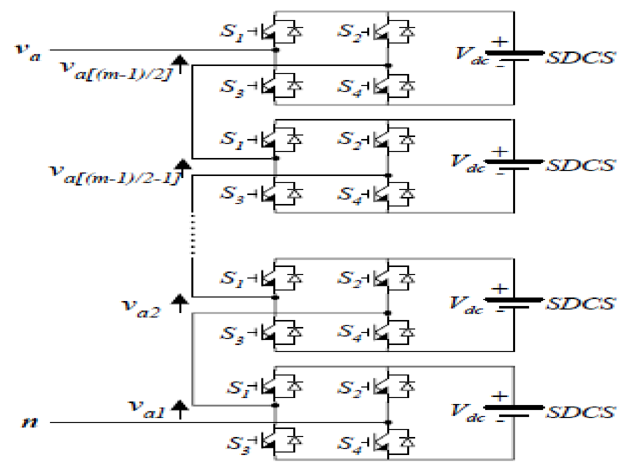
The electrical inverter is a high-power electronic oscillator. It is so named because early mechanical AC to DC converterswere made to work in reverse, and thus were "inverted", to convert DC to AC. The inverter performs the opposite function of a rectifier

2.1 Cascaded H-Bridges inverter

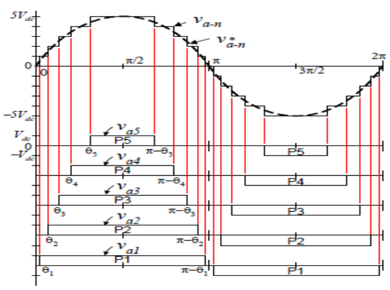
A single-phase structure of an m-level cascaded inverter is illustrated in Figure 31.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $–V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $–V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage $v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}$.

For a stepped waveform such as the one depicted in Figure 31.2 with s steps, the Fourier Transform for this waveform follows

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_n\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n}{n}$$



Single-phase structure of a multilevel cascaded H-bridges inverter



Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

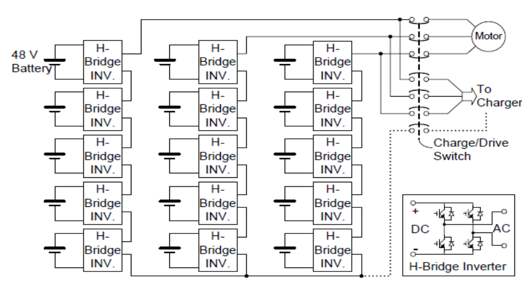
The magnitudes of the Fourier coefficients when normalized with respect to V_{dc} are as follows:

$$H(n) = \frac{4}{\pi n}\left[\cos(n\theta_1) + \cos(n\theta_2) + \ldots + \cos(n\theta_s)\right], \quad \text{where } n = 1, 3, 5, 7, \ldots$$

The conducting angles, θ_1, θ_2, ..., θ_s, can be chosen such that the voltage total harmonic distortion is a minimum. Generally, these angles are chosen so that predominant lower frequency harmonics, 5th, 7th, 11th, and 13th, harmonics are eliminated [5]. More detail on harmonic elimination techniques will be presented in the next section.

Multilevel cascaded inverters have been proposed for such applications as static var generation, an interface with renewable energy sources, and for battery-based applications. Three-phase cascaded inverters can be connected in wye, as shown in Figure 31.3, or in delta. Peng has demonstrated a prototype multilevel cascaded static var generator connected in parallel with the electrical system that could supply or draw reactive current from an electrical system [2-18]. The inverter could be controlled to either regulate the power factor of the current drawn from the source or the bus voltage of the electrical system where the inverter was connected. Peng [2] and Joos [4] have also shown that a cascade inverter can be directly connected in series with the electrical system for static var compensation. Cascaded inverters are ideal for connecting renewable energy sources with an ac grid, because of the need for separate dc sources, which is the case in applications such as photovoltaic's or fuel cells.

Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultracapacitors are well suited to serve as SDCSs [9, 6]. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Figure 31.3. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.



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Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

The main advantages and disadvantages of multilevel cascaded H-bridge converters are as follows

Advantages:

- The number of possible output voltage levels is more than twice the number of dc sources (m = 2s + 1).
- The series of H-bridges makes for modularized layout and packaging. This will enable the manufacturing process to be done more quickly and cheaply.

Disadvantages:

Separate dc sources are required for each of the H-bridges. This will limit its application to products that already have multiple SDCSs readily available.

3. Implementation

Flying-capacitor six-level inverter redundant voltage levels and corresponding switch states

Voltage V_{a0}	Switch State									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_{a0} = 5V_{dc}$ (no redundancies)										
$5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_{a0} = 4V_{dc}$ (4 redundancies)										
$5V_{dc} - V_{dc}$	1	1	1	1	0	0	0	0	0	1
$4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc}$	1	0	1	1	1	0	1	0	0	0
$5V_{dc} - 3V_{dc} + 2V_{dc}$	1	1	0	1	1	0	0	1	0	0
$5V_{dc} - 2V_{dc} + V_{dc}$	1	1	1	0	1	0	0	0	1	0
$V_{a0} = 3V_{dc}$ (5 redundancies)										
$5V_{dc} - 2V_{dc}$	1	1	1	0	0	0	0	0	1	1
$4V_{dc} - V_{dc}$	0	1	1	1	0	1	0	0	0	1
$3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$5V_{dc} - 4V_{dc} + 3V_{dc} - V_{dc}$	1	0	1	1	0	0	1	0	0	1
$5V_{dc} - 3V_{dc} + V_{dc}$	1	1	0	0	1	0	0	1	1	0
$4V_{dc} - 2V_{dc} + V_{dc}$	0	1	1	0	1	1	0	0	1	0
$V_{a0} = 2V_{dc}$ (6 redundancies)										
$5V_{dc} - 3V_{dc}$	1	1	0	0	0	0	0	1	1	1
$5V_{dc} - 4V_{dc} + V_{dc}$	1	0	0	0	1	0	1	1	1	0
$4V_{dc} - 2V_{dc}$	0	1	1	0	0	1	0	0	1	1
$4V_{dc} - 3V_{dc} + V_{dc}$	0	1	0	0	1	1	0	1	1	0
$3V_{dc} - V_{dc}$	0	0	1	1	0	1	1	0	0	1
$3V_{dc} - 2V_{dc} + V_{dc}$	0	0	1	0	1	1	1	0	1	0
$2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_{a0} = V_{dc}$ (4 redundancies)										
$5V_{dc} - 4V_{dc}$	1	0	0	0	0	0	1	1	1	1
$4V_{dc} - 3V_{dc}$	0	1	0	0	0	1	0	1	1	1
$3V_{dc} - 2V_{dc}$	0	0	1	0	0	1	1	0	1	1
$2V_{dc} - V_{dc}$	0	0	0	1	0	1	1	1	0	1
V_{dc}	0	0	0	0	1	1	1	1	1	0
$V_{a0} = 0$ (no redundancies)										
0	0	0	0	0	0	1	1	1	1	1

3.1 Other Multilevel Inverter Structures

Besides the three basic multilevel inverter topologies previously discussed, other multilevel converter topologies have been proposed; however, most of these are "hybrid" circuits that are combinations of two of the basic multilevel topologies or slight variations to them. Additionally, the combination of

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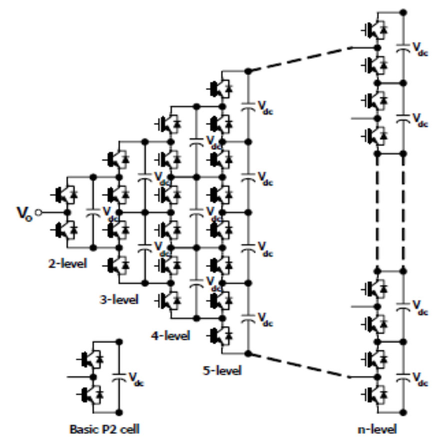
multilevel power converters can be designed to match with a specific application based on the basic topologies. In the interest of completeness, some of these will be identified and briefly described.

A. Generalized Multilevel Topology

Existing multilevel converters such as diode-clamped and capacitor-clamped multilevel converters can be derived from the generalized converter topology called P2 topology proposed by Peng [4] as illustrated in Figure 31.8. The generalized multilevel converter topology can balance each voltage level by itself regardless of load characteristics, active or reactive power conversion and without any assistance from other circuits at any number of levels automatically. Thus, the topology provides a complete multilevel topology that embraces the existing multilevel converters in principle.

Figure 31.8 shows the P2 multilevel converter structure per phase leg. Each switching device, diode, or capacitor's voltage is $1V_{dc}$, for instance, 1/ (m-1) of the DC-link voltage. Any converter with any number of levels, including the conventional bi-level converter can be obtained using this generalized topology [1, 4].



Generalized P2 multilevel converter topology for one phase leg.

B. Mixed-Level Hybrid Multilevel Converter

To reduce the number of separate DC sources for high-voltage, high-power applications with multilevel converters, diode-clamped or capacitor-clamped converters could be used to replace the full-bridge cell in a cascaded converter [5]. An example is shown in Figure 31.9. The nine-level cascade converter incorporates a three-level diode-clamped converter as the cell. The original cascaded H-bridge multilevel converter requires four separate DC sources for one phase leg and twelve for a three-phase converter. If a five-level converter replaces the full-bridge cell, the voltage level is effectively doubled for each cell. Thus, to achieve the same nine voltage levels for each phase, only two separate DC sources are needed for one phase leg and six for a three-

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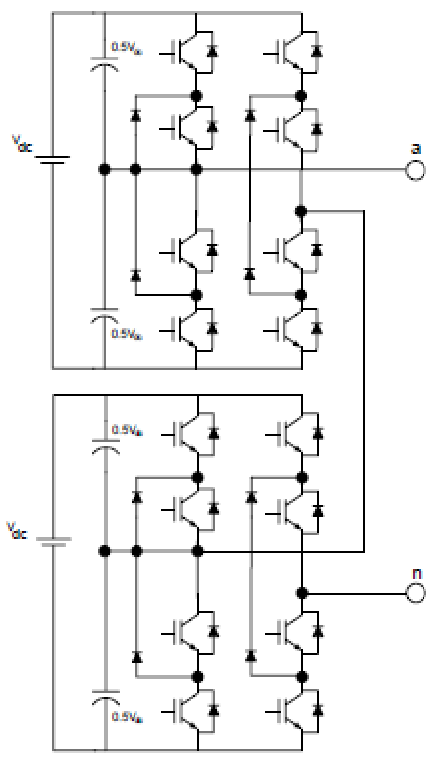
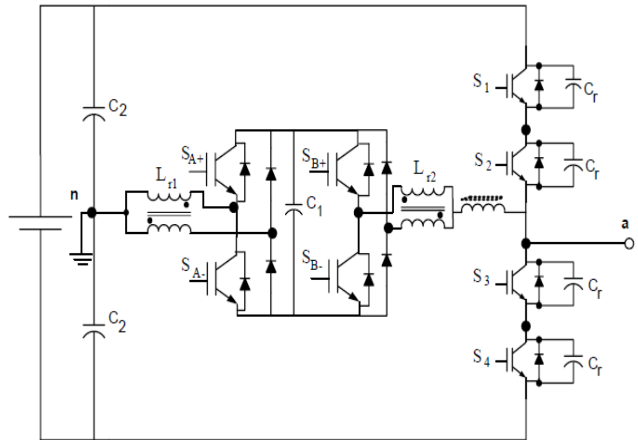
phase converter. The configuration has mixed-level hybrid multilevel units because it embeds multilevel cells as the building block of the cascade converter. The advantage of the topology is it needs less separate DC sources. The disadvantage for the topology is its control



will be complicated due to its hybrid structure.

Mixed-level hybrid unit configuration using the three-level diode-clamped converter as the cascaded converter cell to increase the voltage levels.



Zero-voltage switching capacitor-clamped inverter circuit.

C. Soft-Switched Multilevel Converter

Some soft-switching methods can be implemented for different multilevel converters to reduce the switching loss and to increase efficiency. For the cascaded converter, because each converter cell is a bi-level circuit, the implementation of soft switching is not at all different from that of conventional bi-level converters. For capacitor-clamped or diode-clamped converters, soft-switching circuits have been proposed with different circuit combinations. One of soft-switching circuits is a zero-voltage-switching type which includes auxiliary resonant commutated pole (ARCP), coupled inductor with zero-voltage transition (ZVT), and their combinations [1, 6] as shown in Figure 31.10.

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4. Experimental Work

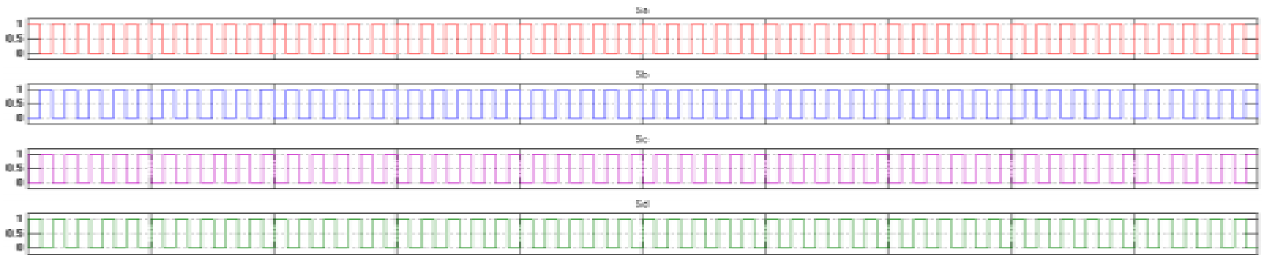

Fig. Switches S_a, S_b, S_c, S_d

Fig. Input Voltage V_{01}

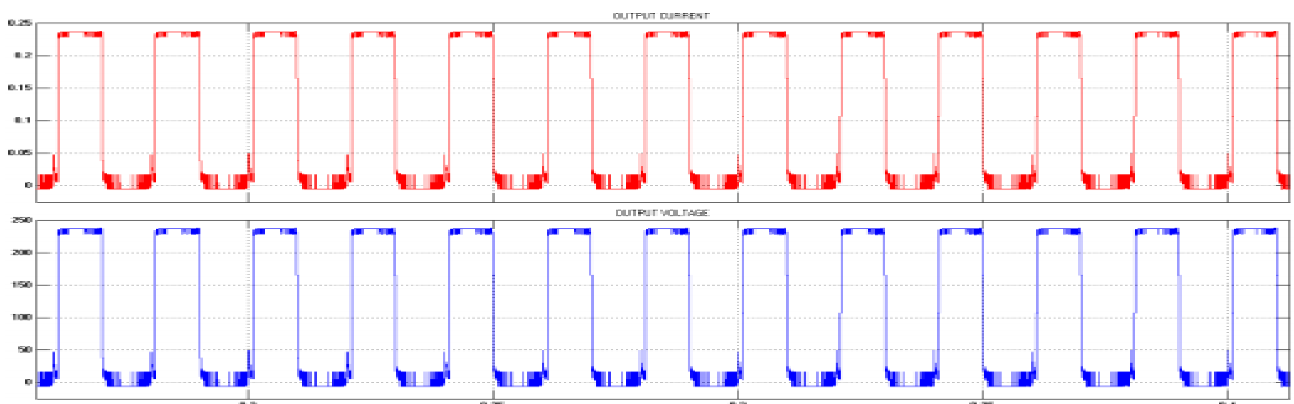

Fig. Output Voltage & Current

5. Conclusion

This paper has proposed a family of multilevel converters based on the concept of nested arrangement. The main advantage of the nested configurations compared to the equivalent NPC topologies are in terms of reduced number of diodes employed and higher efficiency. It has been demonstrated that the conduction losses of the proposed nested topologies are lower than the equivalent NPC converter. Also, the generalized hybrid PWM strategy allows voltages generation with high quality for the converters with number of levels equal or higher than four. Although dealing with irregular blocking voltage distribution among the semiconductor devices, the nested topologies favor the use of wide bandgap devices, such as SiC. In terms of the drivers employed for the nested topology, the four-level circuit requires three high-side drivers and one low-side driver, which is better than the other converters. A generalization of the nested circuit for an odd or even number of levels has been considered in this paper as well.

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