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PV Cell Fed DC-AC Buck and Buck-Boost Inverter

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Abstract- In this concept, two types of DC-DC converters with modified structures and different control methods for generating AC output voltage are proposed. In the modified cascaded dual buck inverter, absence of split capacitors leads to increased reliability of the inverter. Also, a new structure is proposed for integrated dual buck-boost inverter. The proposed inverters are capable of obtaining maximum power from solar cells by themselves. To evaluate operations of the proposed inverters, they have been modeled and simulated in PSCAD/EMTDC for different modulation indexes. Simulation results confirm validity and effectiveness of the proposed inverters.

AMONG various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-c1amped, flying capacitor and cascade H-bridge inverters. The cascaded inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components. They also feature a modular design concept which lessens the maintenance process and the cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaic systems, fuel cells, battery energy storage, and electric vehicle drives, where separate DC Sources naturally exist. However, since most of cascaded inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, they suffer from shoot-through problems, which is the most dominating failure (drawback) of VSIs. In addition, for the hard-switched cascaded inverters operating at higher DC bus voltages, cause them to lose the benefit of using power MOSFETs as the active switching devices for efficiency improvement and fast switching speed when they are available at certain voltage and power level.The proposed concept is implemented to PV cell fed using matlab/simulink software.

Keywords-cascaded dual buck inverter; integrated dual buck boost inverter; PV (photovoltaic) MPPT; split capacitors

I INTRODUCTION

Among various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-c1amped, flying capacitor and cascade H-bridge inverters [1-4]. The cascaded inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components. They also feature a modular design concept which lessens the maintenance process [5-7] and [20, 21]. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaic systems, fuel cells, battery energy storage, and electric vehicle drives, where separate DC sources naturally exist [8- 15] However, since most of cascaded inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, they suffer from shoot-through problems, which is the most dominating failure (drawback) of VSIs. In addition, for the hard-switched cascaded inverters operating at higher DC bus voltages, cause them to lose the benefit of using power MOSFETs as the active switching devices for efficiency improvement and fast switching speed when they are available at certain voltage and power level.

Sun et al. proposed a new cascaded dual buck inverter based on single dual buck inverter topology to address the issues mentioned above [16]. Although the dual buck type inverters are being categorized as VSIs, but they do not suffer from shoot-through problem which ultimately makes them more reliable [17- 19]. System reliability is another feature that also improves through applying the cascaded dual buck inverter because unlike traditional types of cascaded inverters, this type does not suffer from shoot-through concerns associated with each building block. Featuring almost no dead time is another great capability of the cascaded dual buck inverter which results in pushing the duty cycle to the theoretical limit and fully transferring the energy to load via total PWM. In addition, the cascaded dual buck inverter can be hard-switched while utilizing the benefits of power MOSFETs at certain power levels. But in this structure, there are two split capacitors. Voltage balancing of these capacitors is very important. If the voltages of these capacitors are not equal, even harmonics in output voltage will be produced leading to increased losses and decreased efficiency of the converter. In this paper, two DC-AC inverters, called modified cascaded dual buck and new integrated dual buck-boost, are proposed that can solve the aforementioned problem. The proposed dual buck inverter can solve the split capacitors problem, and the integrated dual buck-boost inverter can

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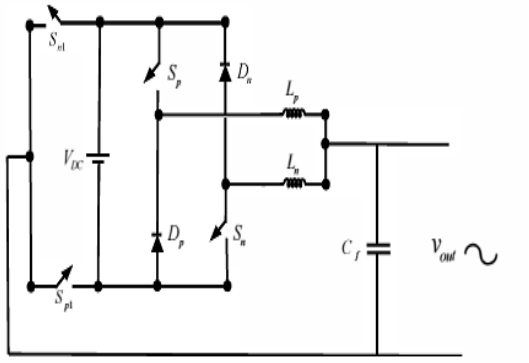
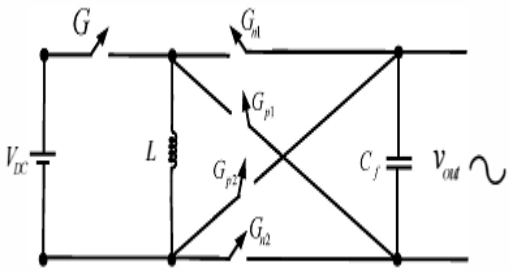
produce proper output AC voltage with minimum components. These inverters are still VSI and have all merits of them that mentioned earlier.

II PROPOSED TOPOLOGIES AND OPERATING PRINCIPALES

The proposed inverters are shown in Fig.3.1. As it can be seen from Fig 1 (a), the proposed Modified Cascaded Dual Buck (MCDB) inverter is comprised of two single buck inverters and two low frequency switches. Also, the proposed novel Integrated Dual Buck-Boost (IDBB) inverter is based on a single buck-boost DC-DC converter with four switches added to it (Fig 1 (b)). It is important to note that all the switches in both inverters are the unidirectional switches.



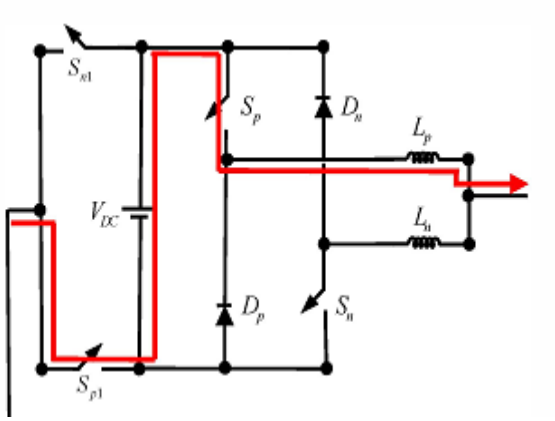
(a)



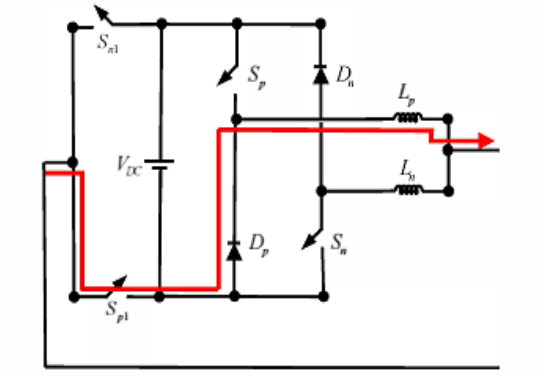
(b)

Fig 1 proposed (a) MCDB (b) IDBB, inverters

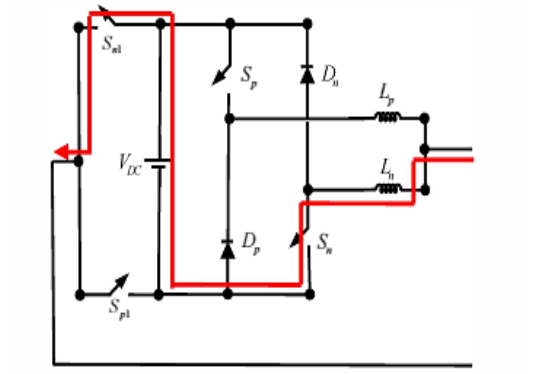
a) Proposed Modified Cascaded Dual Buck Inverter: In Fig 2, different operating modes that are achievable using the proposed MCDB inverter have been illustrated. For cases (a) and (b), the inverter produces positive half cycle of the AC output voltage and cases (c) and (d) contributes for negative half cycle. In Fig 2(a), first, the switches S_p and S_{pi} are on simultaneously, while the others are off. Therefore, the inverter can produce positive voltage which increases the current of positive inductance (L_p), linearly.



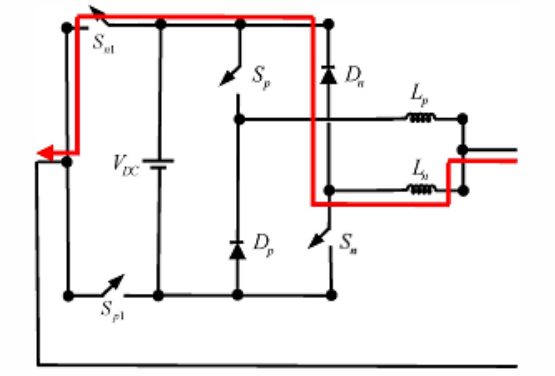
(a)



(b)



(c)



(d)

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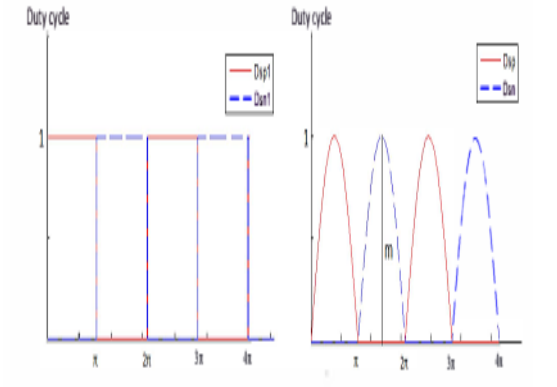
In Fig 2(b), only the switch S_{pi} is on and the others are off, therefore the inverter produces positive voltage in the output, while the current of positive inductance (L_p), decreases linearly. These two operation modes (positive half cycle of AC output voltage), are applied sequentially until positive half cycle of output voltage is finished. In other words, S_{pi} is on throughout positive half cycle of output voltage, but S_p can be on or off and its duty cycle can be increased from zero to one in sine wave type to produce proper positive half cycle of AC output voltage.

In negative half cycle, switching strategy is almost the same as positive section. Throughout negative cycle of AC output voltage, the S_{nl} should be on and S_n should be on or off to increase or decrease the current of negative inductance (L_n). The duty cycle of S_n should be increased from zero to one in sine wave type as similar for S_p.

The proposed MCDB inverter has two high frequency (Sp and Sn)' and two low frequency switches (S_{pi} and S_{nl})' S_{pi} and S_{nl} are on in the positive and negative half cycles of generated output AC voltage, respectively (Fig.3.3 (a)). Duty cycle of switches S_p and Sn are shown in Fig.3.3 (b). As it can be seen, the duty cycles are decided from comparison between fundamental frequency sine wave with peak value of m and sawtooth carrier signal. Therefore m is introduced as follow:



(a) (b)

Fig.3.3 switching signals of the switches of proposed MCDB inverter (a) switches S_{pl} and S_{nl} (b) switches S_p and S_n

$$m = \frac{V_{max}}{V_{dc}} \quad (1)$$

V_{max} is the peak value of desired AC output voltage, and V_{dc} denotes the input DC voltage. The parameter m can attain a value in the range of 0 to 1 in this inverter.

b) Proposed integrated Dual Buck-Boost Inverter:

As seen from Fig.3.4, the proposed IDBB inverter is comprised of a common buck-boost topology loop for charging of inductance (loop (1) in Fig 4), and four switches to change the output polarity (loop (2) in Fig 4).

Duty cycle of switch G is decided from comparison between fundamental frequency sine wave with peak value of m and saw tooth carrier signal. Value of m is calculated from (1). Also (G_{pl}, G_{p2}) and (G_{n1}, G_{n2}) pair switches are on simultaneously in the positive and negative half cycle of output voltage, respectively, in the complimentary state of G.

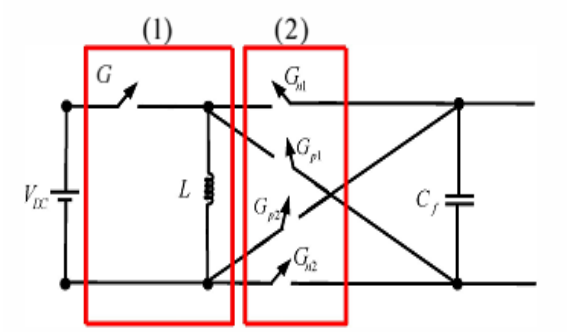
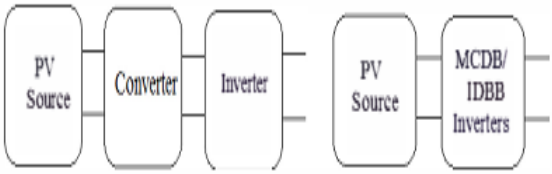


Fig 4 Structure of proposed IDBB inverter

III PV MPPT ANALYZEZ

For inverters with PV sources, two direct and indirect strategies are possible for MPP Tracking. Figure 5 (a), shows the indirect method, in which the PV sources are joined to the inverter by means of another converter tracking the MPP. In direct methodology, the MPPT is being done by the inverter itself which has been depicted in Fig 5(b).



(a) (b)

Fig 5 MPPT control methods (a) indirect method (b) direct method

In indirect method, MPP can be tracked by one of common techniques presented in published literature. According to Fig 5(b), if the direct connection is applied, the proposed inverters will be able to track the maximum power point of PV panels by themselves.

For instance, by considering v_m as the peak value of desired AC output voltage, (2) and (3) can be written for the MCDB and IDBB inverters, respectively.

$$D \times V_{PV} = V_m . sin(\omega t) \quad (2)$$

$$\frac{D}{1-D} \times V_{PV} = V_m . sin(\omega t) \quad (3)$$

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Where, D is the duty cycle of switches and V_{pv} is the PV output voltage. The parameter D should be appropriately chosen for satisfying the following equation.

$$V_{pv} = V_{mpp} \tag{4}$$

To track maximum power point of PV panels by inverter, the following equations are applied to choose suitable values for D_{sp} ,D_{sn} and DG.

$$D_{s_p} = \frac{V_m}{V_{pv}}.|sin(\omega t)| \quad ,0 < \omega t < \pi \tag{5}$$

$$D_{s_n} = \frac{V_m}{V_{pv}}.|sin(\omega t)| \quad ,\pi < \omega t < 2\pi \tag{6}$$

$$D_G = \frac{V_m.|sin(\omega t)|}{V_{pv}+V_m.|sin(\omega t)|} \quad ,0 < \omega t < 2\pi \tag{7}$$

IV COMPONENTS DETERMINATION

The relationship between voltage and current of inductor can be written as eq. (8).

$$v_L = L\frac{di_L}{dt} \tag{8}$$

In the MCDB inverter, while the S_p is on, (T_{on} = DT = $\frac{D}{f}$), (3.8) can be rewritten as follow:

$$V_{DC} - V_{out} = L\frac{\Delta i_L}{DT} = L\frac{f\Delta i_L}{D} \tag{9}$$

In (9), V_{DC} is the input DC source, V_{out} is the output voltage of buck converter, D is the duty cycle of switch S_p and f is the switching frequency. In the buck converter:

$$V_{out} = D \times V_{DC} \tag{10}$$

By replacing (10) in (9) and doing necessary simplifications, (11) is resulted:

$$L = \frac{D(1-D)V_{DC}}{f\Delta i_L} = \frac{(1-D)V_{out}}{f\Delta i_L} \tag{11}$$

Where Δi_L is the acceptable current ripple. If the proposed inverter be considered to operate in the Continuous Current Mode (CCM), from (11), the minimum value of L would be calculated as (13)

$$\Delta i_L = \frac{2V_{out}}{R_{out}} \tag{12}$$

$$L_{min} = \frac{(1-D)R_{out}}{2f} \tag{13}$$

The R_{out} is the load resistance. By considering the D to be zero:

$$L_{min} = \frac{R_{out}}{2f} \tag{14}$$

Also in the IDBB inverter, while G is off, (T_{off} = (1-D) T = $\frac{1-D}{f}$), (8) can be rewritten as follow:

$$V_{out} = L\frac{\Delta i_L}{(1-D)T} = L\frac{f\Delta i_L}{(1-D)} \tag{15}$$

The V_{out} is the output voltage of buck-boost converter, D is the duty cycle of switch G and f is the switching frequency. By considering that I_{out} is the average current of switch S_{pi} or S_{nl} current, (16) is resulted.

$$\Delta I_L = \frac{2I_{out}}{1-D} \tag{16}$$

From (15) and (16), (17) is resulted.

$$L = \frac{(1-D)^2 V_{out}}{2fi_{out}} = \frac{(1-D)^2 R_{out}}{2f} \tag{17}$$

R_{out} is the load resistance. The value of D can change from zero to one. For Continuous Current Mode (CCM) operation of the proposed inverter and proper value selection of L, the D is considered to be 0.9. According to (17), minimum value of L can be calculated as (18).

$$L_{min} = \frac{R_{out}}{200f} \tag{18}$$

A PHOTOVOLTAIC SYSTEM

A photovoltaic system, converts the light received from the sun into electric energy. In this system, semi conductive materials are used in the construction of solar cells, which transform the self contained energy of photons into electricity, when they are exposed to sun light. The cells are placed in an array that is either fixed or moving to keep tracking the sun in order to generate the maximum power [9]. These systems are environmental friendly without any kind of emission, easy to use, with simple designs and it does not require any other fuel than solar light. On the other hand, they need large spaces and the initial cost is high.

PV array are formed by combine no of solar cell in series and in parallel. A simple solar cell equivalent circuit model is shown in figure. To enhance the performance or rating no of cell are combine. Solar cell are connected in series to provide greater output voltage and combined in parallel to increase the current. Hence a particular PV array is the

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combination of several PV module connected in series and parallel. A module is the combination of no of solar cells connected in series and parallel.

The photovoltaic system converts sunlight directly to electricity without having any disastrous effect on our environment. The basic segment of PV array is PV cell, which is just a simple p-n junction device. The fig.1.4 manifests the equivalent circuit of PV cell. Equivalent circuit has a current source (photocurrent), a diode parallel to it, a resistor in series describing an internal resistance to the flow of current and a shunt resistance which expresses a leakage current. The current supplied to the load can be given as.

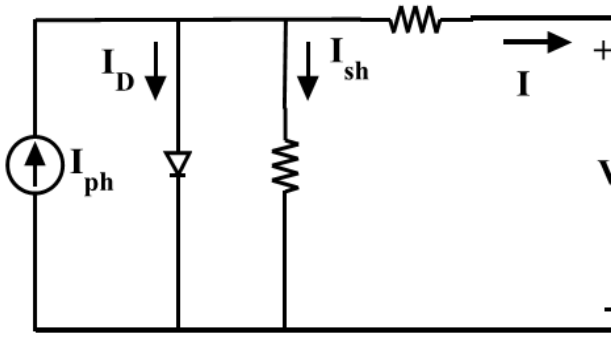
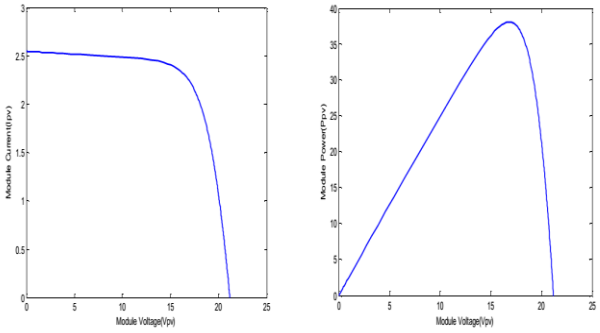


Fig 6 Equivalent circuit of Single diode modal of a solar cell

$$I = I_{PV} - I_O\left[\exp\left(\frac{V+IR_S}{aV_T}\right)-1\right]-\left(\frac{V+IR_S}{R_P}\right)$$

Where
IPV–Photocurrent current,
IO–diode's Reverse saturation current,
V–Voltage across the diode,
a– Ideality factor
VT –Thermal voltage
Rs – Series resistance Rp –Shunt resistance



IV MATLAB/SIMULATION RESULTS

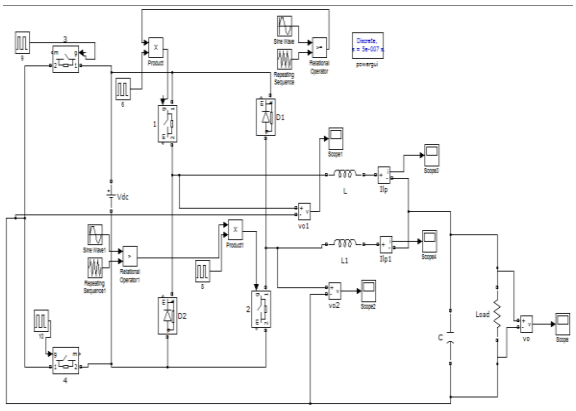


Fig 7 Matlab/simulation circuit of Modified Cascade Dual Buck converter

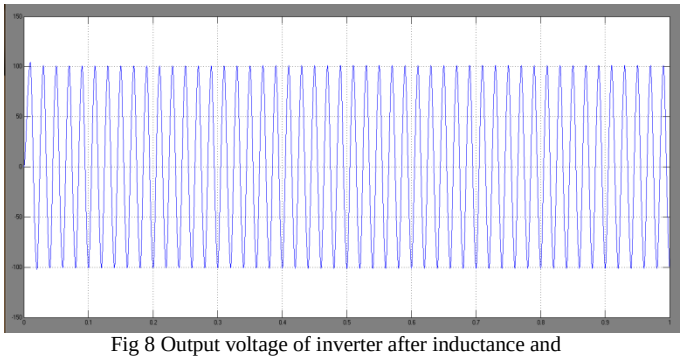


Fig 8 Output voltage of inverter after inductance and output voltage of inverter before inductance, when the inverter connected to the load, R =IOn , for the case of (a) m=O.3

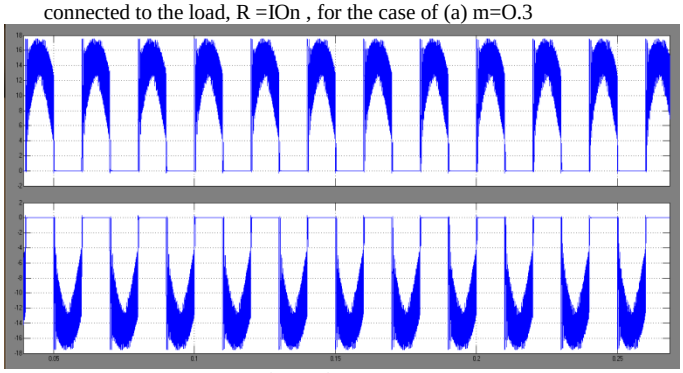


Fig 9 Current waveform of inductance Lp and L" when the inverter connected to the load of R = 1on , for the case of m =0.3

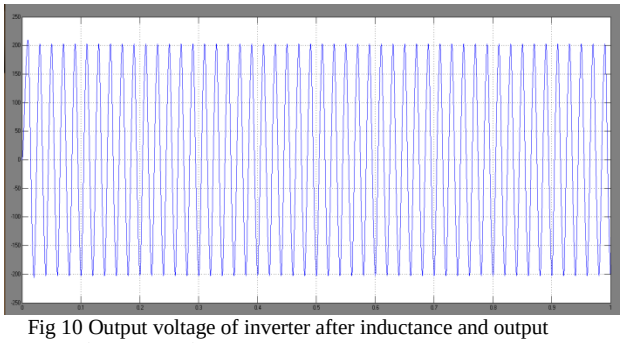


Fig 10 Output voltage of inverter after inductance and output voltage of inverter before inductance, when the inverter connected to the load, R =IOn , for the case of m=O.7

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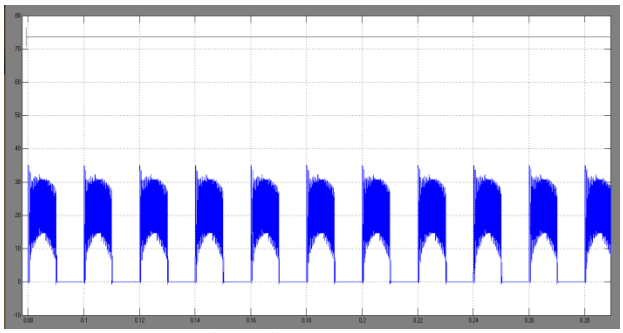

Fig 11 Current waveform of inductance Lp and L" when the inverter connected to the load of R = 1on , for the case of m =0.7

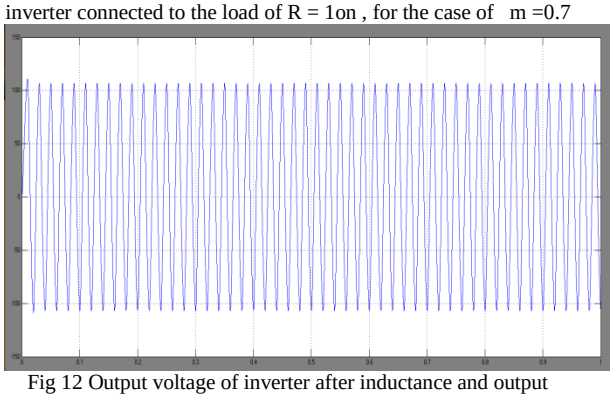

Fig 12 Output voltage of inverter after inductance and output voltage of inverter before inductance, when the inverter connected to the load of R=50n,L=50mH , for the case of (a) m=0.3

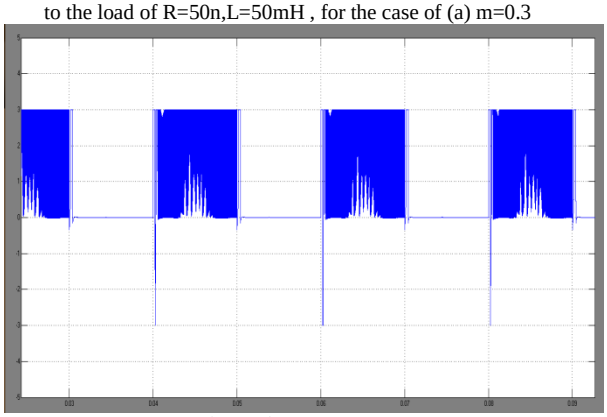

Fig 13 Current waveform of inductance Lp and L" when the inverter connected to the load of R =50n,L =50mH , for the case of (a) m = 0.3

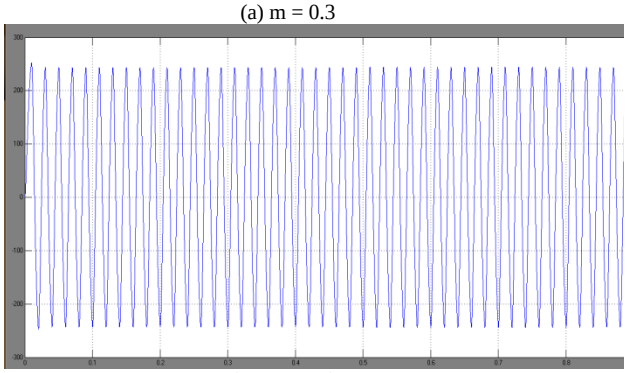

Fig 14 Output voltage of inverter after inductance and output voltage of inverter before inductance, when the inverter connected to the load of R=50n,L=50mH , for the case of (a) m=0.7

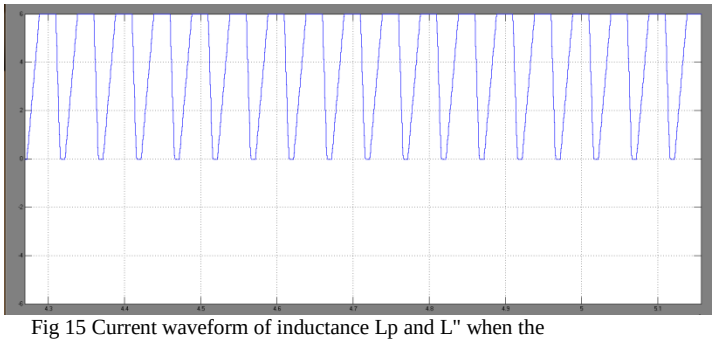

Fig 15 Current waveform of inductance Lp and L" when the inverter connected to the load of R =50n,L =50mH , for the case of (a) m = 0.7

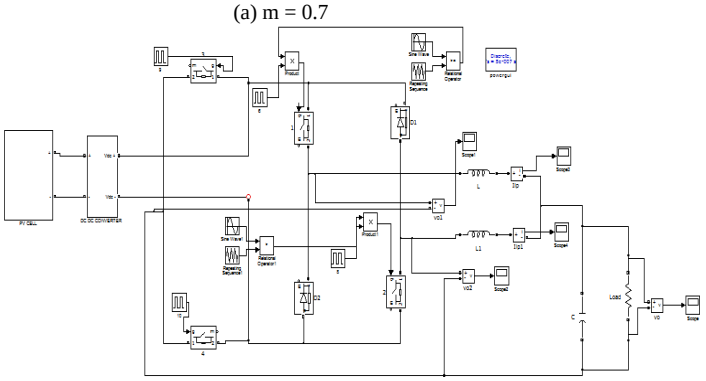

Fig 16 Matlab/simulation circuit of Modified Cascaded Dual Buck converter with PV

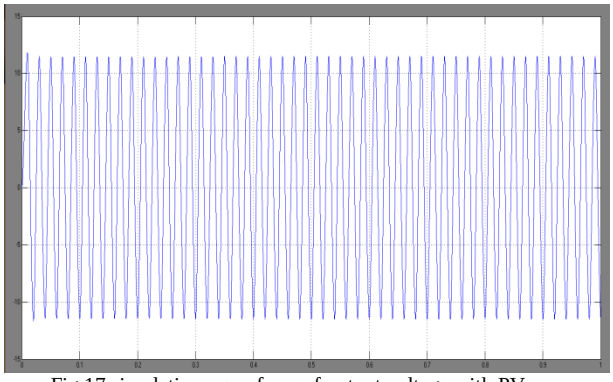

Fig 17 simulation wave form of output voltage with PV

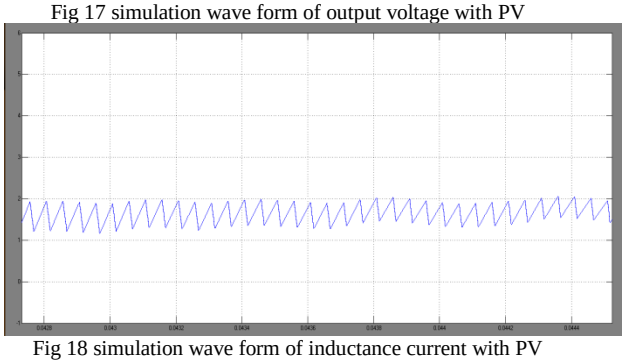

Fig 18 simulation wave form of inductance current with PV

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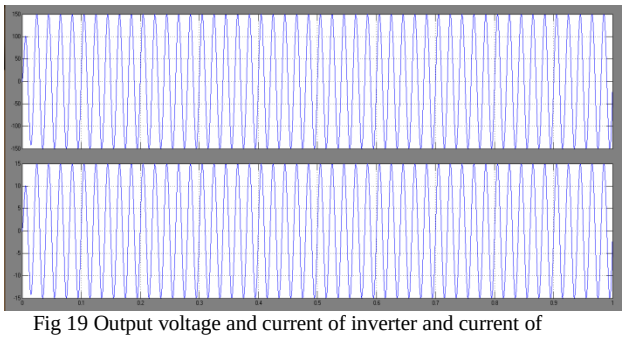

Fig 19 Output voltage and current of inverter and current of inductance, when the inverter connected to the load, R=lOn , for the case of (a) m =0.3

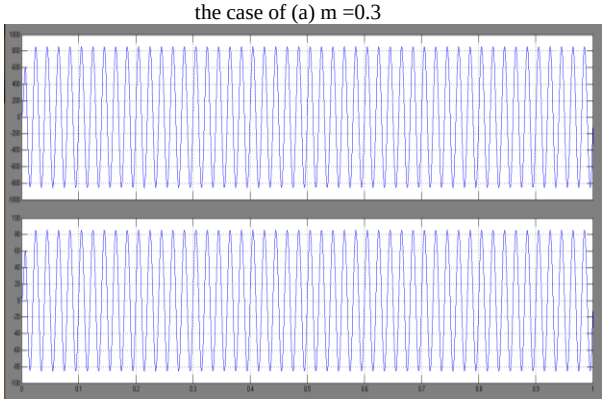

Fig 20 Output voltage and current of inverter and current of inductance, when the inverter connected to the load, R=lOn , for the case of (a) m =0.7

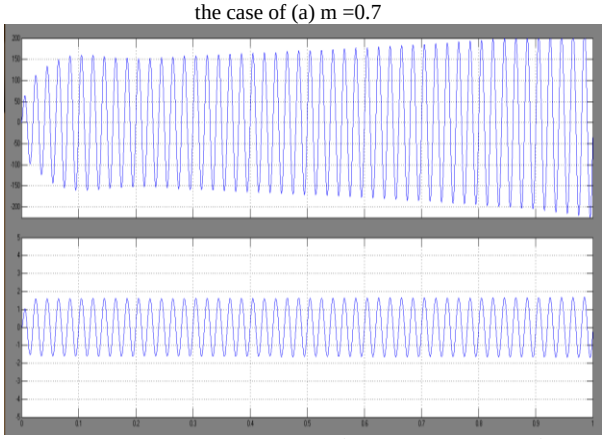

Fig 21 Output voltage and current of inverter and current of inductance, when the inverter connected to the load, R=50n,L=50mH , for the case of (a) m=O.3

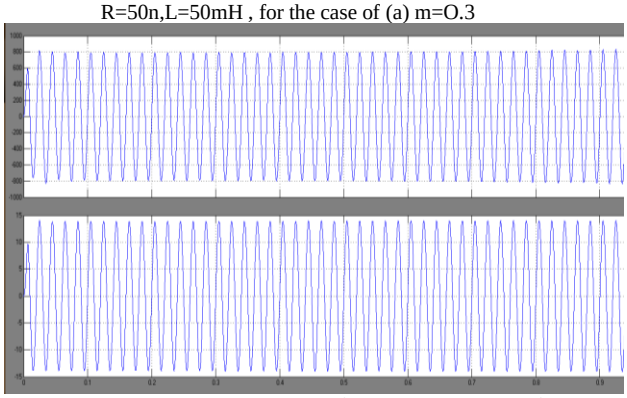

Fig 22 Output voltage and current of inverter and current of inductance, when the inverter connected to the load, R=50n,L=50mH , for the case of (b) m=O.7

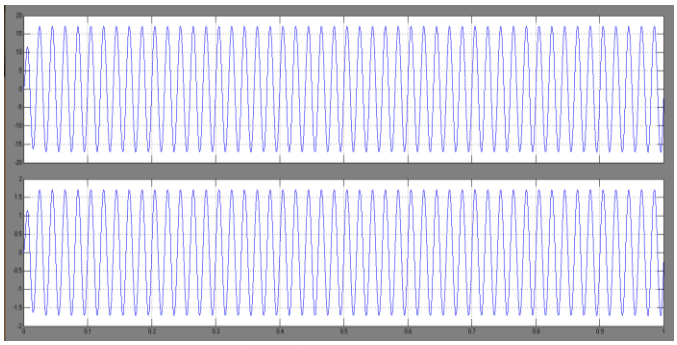

Fig 23 simulation wave form of Integrated Dual Buck-Boost (IDBB) voltage and current with PV

V CONCLUSION

This paper has proposed a modified cascaded dual buck inverter, absence of split capacitors leads to increased reliability of the inverter and also Integrated Dual Output Buck Boost converter. This converter having advantages of step up/step down dc-ac converter includes system reliability, reduction of size of components and there by acquiring less mass for the whole converter. The dual buck type inverters are still VSI, but with the unique topology and operation, they do not have the shoot-through worries, which lead to greatly enhanced reliability. With phase-shifted PWM fed to different cascade units, zero crossing distortion is eliminated. The phase-shift control increases the equivalent switching frequency by N times that of single-unit inverter, which leads to lower current ripple. Those converters are capable of obtaining maximum power from solar cells by themselves. This could be well verified from the simulation results. The converter gives an efficiency of 89.95%.To proposed with Renewable energy source are more economical .The converter behavior has been simulated in PSCAD/IEMTDC, the output voltage of inverter for both presence and absence of inductance, respectively showed.

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