International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

Reduced Switches Based Three-Phase Multi-Level Inverter for Induction Motor applications

Varikuppala Mahesh
M-tech Student Scholar
Department of Electrical & Electronics Engineering,
Global Institute of Engineering & Technology, Chilkur(V);
Moinabad(M) R.R (Dt); Telangana, India.
Email:varikuppalama@gmail.com

T.V.V Pavan Kumar M.Tech (Ph.D)
Project Supervisor & HOD
Department of Electrical & Electronics Engineering,
Global Institute of Engineering & Technology, Chilkur(V);
Moinabad(M) R.R (Dt); Telangana, India.
Email:pavankumart99@gmail.com

***Abstract*- In recent decades, the demand for high voltage, high power inverters that capable to transfer a high power, has increased due to the industrial and residential demands. However, the traditional converters rating power are limited to the rated power of the used semiconductor devices and the allowed switching frequencies. The idea of introducing multilevel inverters strongly has appeared to overcome the previous traditional inverters drawbacks. The general concept of multi-level inverter is to utilize isolated dc sources or a bank of series capacitors to produce ac waveforms with higher amplitude. The salient advantages of these inverters are small output voltage step, which results in high power quality, low harmonic components, better electromagnetic compatibility, and low switching losses. The proposed inverter operates with symmetrical DC power sources and low frequency modulation technique as well. The main contribution of the proposed topology is the total number of the active power switches used to generate the same number of levels compared to the previous topology is reduced by25 %. Therefore, it is expected that the proposed inverter has high efficiency and low control complexity due to the decreased number of the power switches. The operation of the proposed inverter hasbeen conducted by simulation results. Moreover, a comparison between the proposed inverter output is connected to Induction motor application**

***Keywords*—Three-phase multi-level inverter, low frequency modulation technique, symmetrical DC power sources, Induction motor.**

I. INTRODUCTION

Multilevel converters have received more and more attention because of their capability of high voltage operation, high efficiency, and low electromagnetic interference (EMI). The desired output of multilevel converter is synthesized by several sources of dc voltages. With an increasing number of DC voltage sources, the converter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. These results in low switching losses, and because of several DC sources, the switches experience a lower voltage stress. As a result, multilevel converter technology is promising for high power electric devices such as utility applications [1]. There are three major multilevel topologies: cascaded, diode clamped, and capacitor clamped. For the number of levels (M) greater than three or some applications such as reactive and harmonic compensation in power systems, these multilevel converters do not require a separate dc power source to maintain each voltage level. Instead, each voltage level can be supported by a capacitor with proper control. However, for M > 3 and applications involved inactive power transfer, such as motor drives, these multilevel converters all require either isolated dc power sources or a complicated voltage balancing circuit and control scheme to support and maintain each voltage level. In this aspect, the three existing multilevel converters are neither operable nor complete for real(active) power conversion because they all depend on outside circuits for voltage balancing [2]. Multilevel inverters produce a stepped output phase voltage with a refined harmonic profile when compared to a two level inverter-fed drive system. However, these configurations are also complex for higher number of levels. The three-level inverter is realized by connecting two 2-level inverters in cascade. This three-level inverter structure does not show the voltage fluctuations of the neutral point, as isolated power supplies are employed to power the individual inverters. [3-5].

For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources [4]. To reduce the number of DC sources and semiconductor switches required, when the multilevel converter is applied to a motor drive. This scheme provides the capability to produce higher voltages at higher speeds (where they are needed) with a low switching frequency, which has inherent low switching losses and high conversion efficiency. For electric/hybrid electric vehicle motor drive applications, one H-bridges and four switches for cascading the batteries for each phase is a good tradeoff between performance, cost and reliability.

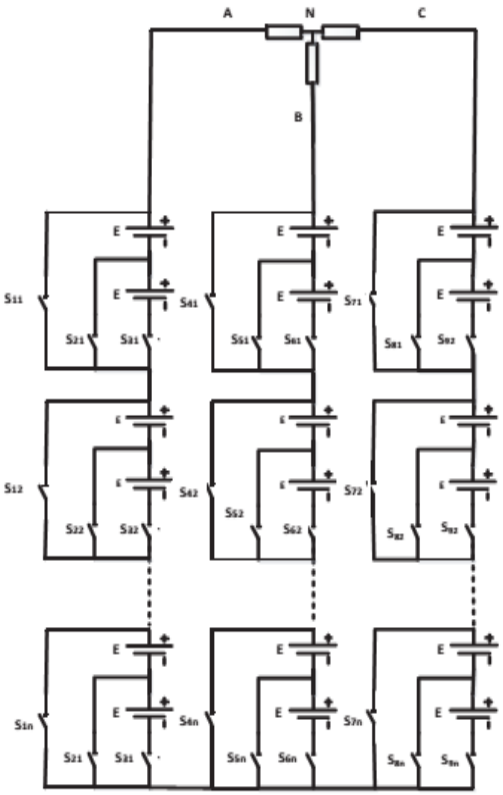
In this paper is organized as details the MLI fed induction motor drives. The performance investigation of the designed MLI fed induction motor drive is carried out; simulation results are presented and discussed. The performance of MLI and conventional inverters compared and results are presented and conclude the paper.

II. THE PROPOSED MLI TOPOLOGY

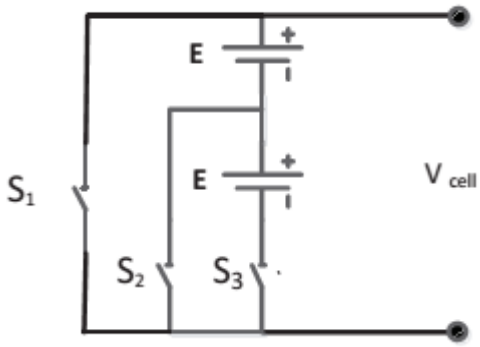
A new multi-level three-phase voltage source inverter with reduced components count is introduced in this paper. Figure 1 (a) shows the generalized power circuit of the proposed topology. It is formed through the arrangement of the primary basic cell in series configuration that is shown in Fig. 1 (b). Every basic cell consists of three switches S_1, S_2, $S_3$and two symmetrical

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

DC-power sources. This cell produces three voltage levels as explained in the following: when S_1in ON state a $0V_{dc}$is produced on the cell terminal, when S_2 in ON state an $EV_{dc}$is produced on the cell output, when S_3 in ON state $2EV_{dc}$is produced on the cell terminal ports. It should be noted that no switches could be operated in the ON at the same time in order to avoid a short circuit across the cell's DC power sources. Table1 summarizes the different switching states and the corresponding output voltage of the proposed MLI topology.



(a) Proposed topology.



(b) Basic cell.

Fig.1: The proposed MLI topology

TABLE 1: SWITCHING STATES FOR THE BASIC CELL

Switching state	Switch			Basic-unit Output voltage
	S_1	S_2	S_3	
1	ON	OFF	OFF	0
2	OFF	ON	OFF	E
3	OFF	OFF	ON	2E

The proposed topology can be extended to have multi-levels more than three levels per cell, by forming a series configuration of the basic cell. The number of the generated output line voltage levels (*M*), output phase voltage levels (M_{ph}), the number of the used basic cells (N_{Cells}), the number of switches ($N_{Switches}$) and DC power supply ($N_{Sources}$) all are given in (1) - (5) respectively

$$M = 4\,N_{Cells} + 1 \quad (1)$$

$$M_{ph} = 4\,N_{Cells} + 3 \quad (2)$$

$$N_{cells} = \frac{M-1}{4} \quad (3)$$

$$N_{Switches} = 3\,N_{Cells} \quad (4)$$

$$N_{Sources} = 2\,N_{Cells} \quad (5)$$

For example to obtain a nine voltage levels on the output line voltage (V_{ab}), according to the above equations, the investigated inverter produce five level per pole voltage (V_{ao}), eleven voltage levels per phase (V_{an}). Therefore, it is required for each arm to have two basic cells connected in series configuration, which is constructed from six switches and four symmetrical DC-power sources. The proposed multi-level inverter is recommended for the renewable energy resource especially the photovoltaic (PV) farms, at which there are enough DC energy sources to use.

In addition, the investigated topology is implemented as symmetrical MLI. However, it can be implemented as an asymmetry MLI, In this case, the voltage levels number increased dramatically. The relationship between the used DC-power sources voltages values will be: double ratio (D-Ratio) (E, 2E volt) or triple ratio (TR-ratio) (E, 3E volt). In this case, the equations controlled the number of the generated levels are matching the one presented in [13].

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

III. PROPOSED INVERTER SWITCHING SCHEME

Driving the inverter switches according to low frequency modulation, a square wave pulses have been generated according to Table 3. There are twelve modes of operation per one cycle (50 Hz). The driver signals for arm Band arm Care shifted by 120°, -120°, respectively. In order to produce three phase blanched output voltages, the MLI's switching scheme that is shown in Fig. 2 has to be accomplished.

The switching devices for each arm, fired by signals that are generated by Appling some logical operations on the six periods (P1to P6). The six periods produced from the intersection of rectified sine wave with amplitude equal to (Xvolt), and a constant DC value equal to (X/2 volt), as shown in Fig.2. As the sine wave amplitude voltage (X) value varies, the switching signal width for each switch will vary also. Therefore, as a result the THD and the output voltage root mean square (V_{rms}) will be varying. Equations (6) to (8) describe the logical operation applied on ($P_1$to P_6) to produce the required switching devices signals (S_1, S_2, S_3) for phase (A) as;

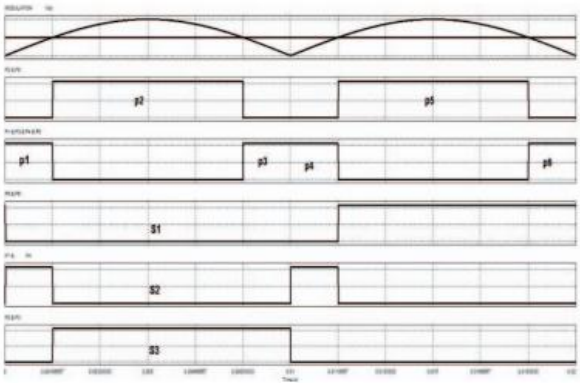


Fig.2: The six pulses generation.

$$S_1 = P_5 + P_6 \quad (6)$$

$$S_2 = P_1 + P_4 \quad (7)$$

$$S_3 = P_2 + P_3 \quad (8)$$

Where + stands for logic OR.

IV. COMPARISON OF THE PROPOSED TOPOLOGY WITH PREVIOUS MULTI-LEVEL INVERTERS

In order to ensure the feasibility of the proposed inverter, it is compared with the recent published topologies of multi-level inverter. They are introduced in[10], [12], [13], and [14]. The number of the voltage levels per pole is fixed for the comparison purpose. Also, the comparison is done based on symmetrical DC power supplies. For example, the presented topology in [13] is asymmetrical cascaded multi-level voltage source inverter and the proposed topology is symmetrical cascaded multi-level voltage source inverter, so the comparison is done for the topology in [13] by using symmetrical DC power sources only. This comparison of previous multilevel inverter and shows that the proposed topology has the smallest number of the active switches over other topologies.

The topology in [13], are the closest topologies to the proposed one, so a comparisons is carried out between them based on the required components and THD points of view. It is noticed that, the proposed topology in this paper requires reduced number of components to generate the same number of output pole voltage levels. It is about 25% reduction on the switches number. In terms of the output voltage quality aspects as total harming distortion THD, the proposed inverter circuit seems to have better THD factor compared to the topologies presented.

INDUCTION MOTOR (IM)

An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor. Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$n_s = \frac{120 f}{P}$$

Where f is the frequency of AC supply, n, is the speed of rotor; p is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.

A. Control Strategy of Induction Motor

Power electronics interface such as three-phase SPWM inverter using constant closed loop Volts l Hertz control scheme is used to control the motor. According to the desired output speed, the amplitude and frequency of the

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

reference (sinusoidal) signals will change. In order to maintain constant magnetic flux in the motor, the ratio of the voltage amplitude to voltage frequency will be kept constant. Hence a closed loop Proportional Integral (PI) controller is implemented to regulate the motor speed to the desired set point. The closed loop speed control is characterized by the measurement of the actual motor speed, which is compared to the reference speed while the error signal is generated. The magnitude and polarity of the error signal correspond to the difference between the actual and required speed. The PI controller generates the corrected motor stator frequency to compensate for the error, based on the speed error.

V. SIMULATION RESULTS

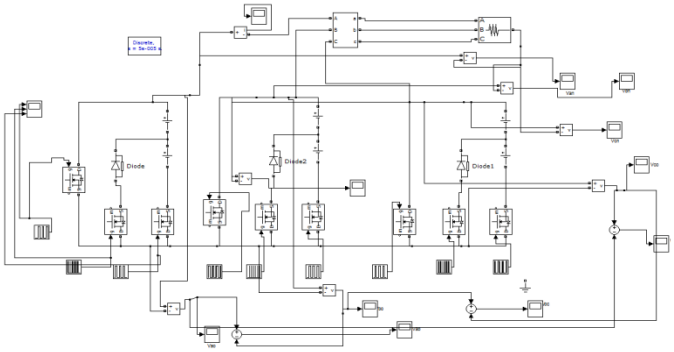


Fig.3.Simulation model of three seven level inverter with grid connected system.

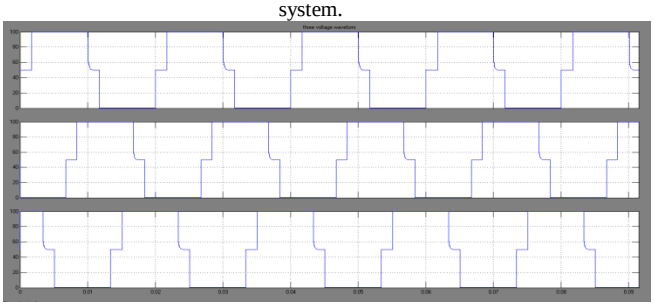


Fig. 4: simulation wave form Pole voltage (Vao,Vbo and Vco).

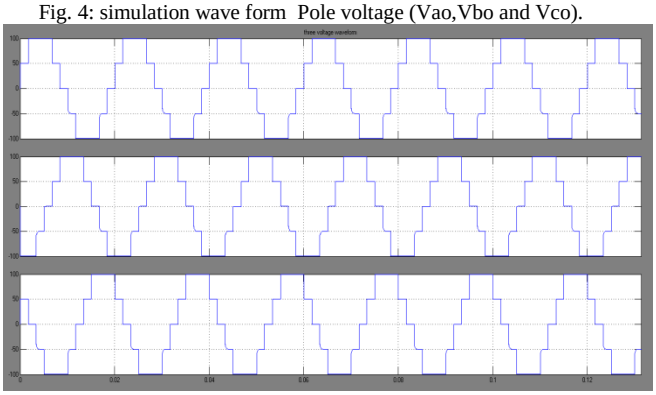


Fig. 5: The simulation waveforms for the line voltages waveforms (Vab, Vbcand Vca).

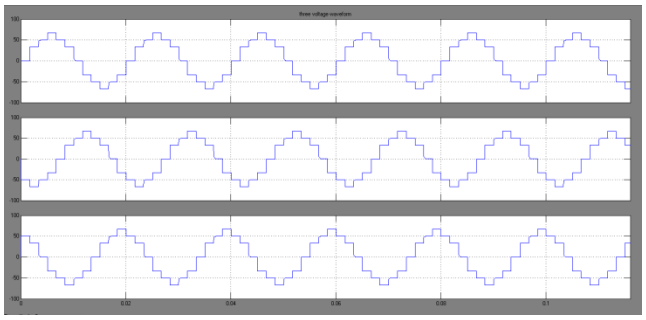


Fig. 6: The simulation results for the three phase voltages waveforms (Van, Vbn, Vcn).

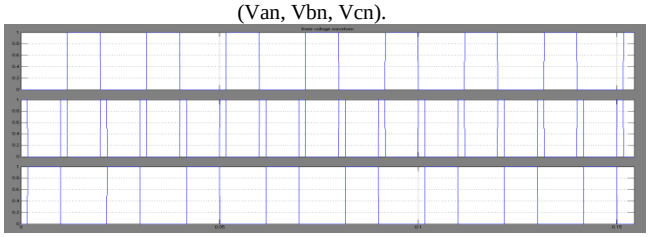


Fig.7: Simulation wave form of switching scheme for S1, S2 and S3.

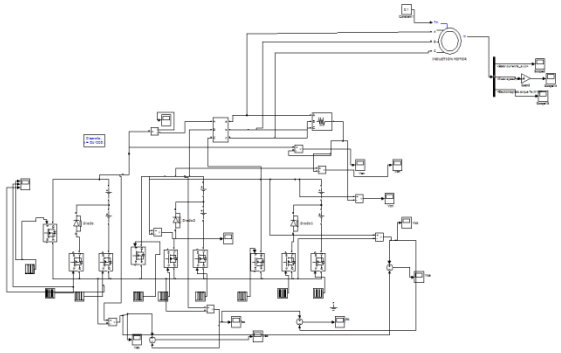


Fig 8 Simulation model of three seven level inverter with grid connected system with Induction motor drive

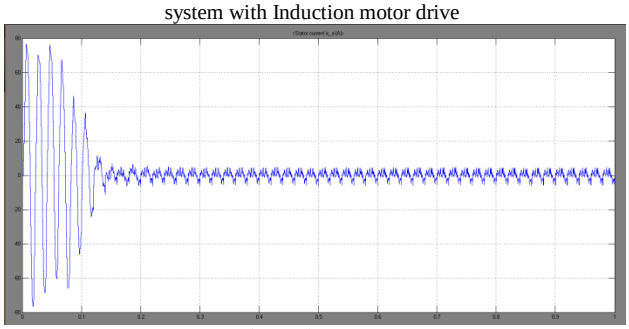


Fig 9 simulation wave form of induction motor stator current

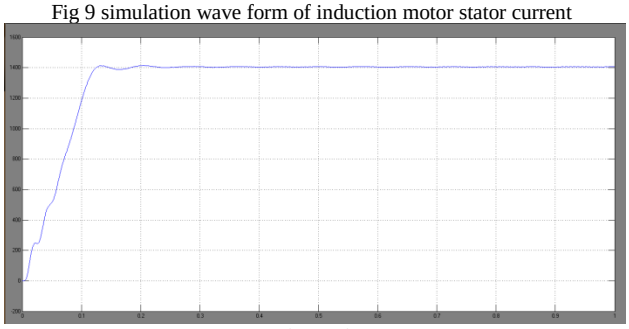


Fig 10 simulation wave form of induction motor speed

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 03 Issue 17
November 2016

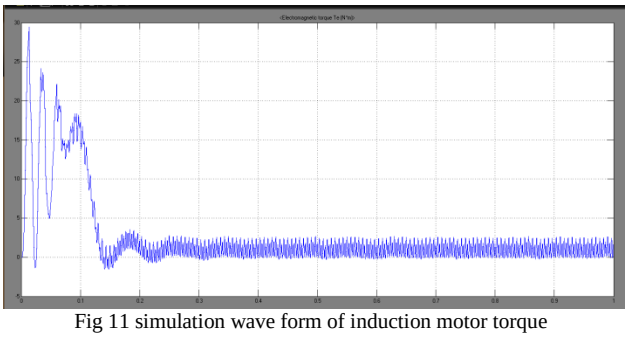


Fig 11 simulation wave form of induction motor torque

VI. CONCLUSION

In this paper, a new inverter topology for induction motor drive has been proposed which has superiorfeatures over conventional topologies in terms of the required power switches and isolated dc supplies, controlrequirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in power applications such as FACTS, HVDC, PV systems, UPS, etc. In the mentioned topology, the switching operation is separated into high- and low-frequency parts. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. The experimental results of the developed prototype for a conventional inverter and proposed inverter of the induction motor are demonstrated in this paper. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of switches. Moreover it effectively diminishes lower order harmonics. Therefore effective reduction of total harmonics distortion is achieved. And that output voltage is applied to the induction motor drive and study the characteristics of IM

REFERENCES

[1] Hammond, P.W, "A new approach toenhance power quality for medium voltage AC drives," IEEE Trans. Ind. Appl., 1997, 33, (1), pp. 202–208.

[2] S. J. Park, F. S. Kang, M. H. Lee, and C. U. Kim, "A new single-phase five level PWM inverter employing a deadbeat control scheme," IEEE Trans.Power Electron., vol. 18, no. 18, pp. 831–843, May 2003.

[3] Agelidis, V. G., Baker, D. M., Lawrance, W. B., and Nayar, C. V., "A multilevel PWM inverter topology for photovoltaic applications," Proceedings of the IEEE International symposium on Industrial Electronics, Vol. 2, pp. 589-594, July 1997, Portugal, Guimaraes.

[4] Gui-Jia Su, "Multilevel DC-Link Inverter", IEEE TRANS.IND. APPLICATIONS, vol. 41, no. 3, may/June 2005.

[5] M. Calais, L. J. Borle, and V. G. Agelidis, "Analysis of multicarrier PWM methods for a single-phase five-level inverter," in Proc. 32nd Annu. IEEE PESC, Jun. 17–21, 2001, vol. 3, pp. 1173–1178.

[6] Abdelaziz Fri, Rachid El Bachtiri, Abdelaziz El Ghzizal, "Basic topologies of a three-phase inverter (5l) for a photovoltaic system controlled by multi-carrier spwm,"Journal of Theoretical and Applied Information Technology, 10th September 2013. vol. 55 no.1

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter,"IEEE Trans. Ind. Appl., vol.1A-17, no. 5, pp. 518-523,

[8] M. F. Escalante, J. C. Vannier,and A. Arzande, "Flying capacitor multilevel inverters and DTC motor drive applications," IEEE Trans. Ind.Electron., vol. 49, no. 4, pp. 809–815, Aug. 2002.

[9] M. Malinowski, K. Gopakumar, J. Rodriguez, M. Pérez., "A Survey on Cascaded Multi-level Inverters,"IEEE Trans Ind. Electron., vol. 57, no.7, pp. 2197-2206, 2010.

[10] S. Nagaraja Rao, D.V. Ashok Kumar, Ch. Sai Babu, "New Multilevel Inverter Topology with reduced number of Switches using Advanced ModulationStrategies,"2013 International Conference on Power, Energy and Control (ICPEC).

[11] Nasrudin Abd. Rahim, Mohamad Fathi Mohamad Elias, and Wooi Ping Hew, "Transistor-Clamped H-Bridge Based Cascaded Multi-level Inverter With New Method of Capacitor Voltage Balancing,"IEEE transactions on industrial electronics, vol. 60, no. 8, august 2013.

[12] E.A. Mahrous, N.A. Rahim and W.P. Hew, "Three-phase three-level voltage source inverter with low switching frequency based on the two level inverter topology,"IET Electr. Power Appl., 2007, 1, (4), pp. 637 –641.

[13] Hamza Belkamel, Saad Mekhilef, Ammar Masaoud, Mohsen Abdel Naeim, "Novel three-phase asymmetrical cascaded multi-level voltage source inverter,"IET Power Electron., 2013, Vol. 6, Iss. 8, pp. 1696–1706.

[14] Ahmed Salem, Emad M. Ahmed, Mohamed Orabi, and Afef Ben Abdelghani, "Novel Three-Phase Multi-level Voltage Source Inverter with Reduced No. of Switches, "The Fifth International Renewable Energy Congress, 14-WEN-386-O, 2014.