Design and Analysis of Distributed Generation System for Quasi Z-source Inverter fed BLDC Drive

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Abstract–The major players in renewable energy generation are photovoltaic (PV), wind farms, fuel cell, and biomass. These distributed power generation sources are widely accepted for microgrid applications. However, the reliability of the microgrid relies upon the interfacing power converter.The quasi z-source concept can be applied to all dc-ac, ac-dc and dc-dc power conversion whether two-level. The input voltage and output voltage share the common ground, the size of the inverter is reduced, and it operates in a continuous current mode.BLDC motor is connected at the output side which acts as a load and efficiently utilizes the power obtained from solar using PI. The qZSI acts as the interface in between the PV dc source and the BLDC motor. PI promises the maximum power delivery to the load based on maximum power point tracking (MPPT). The proposed PI-based MPPT offers high efficiency and accuracy. The closed loop control regulates the speed of the BLDC motor for different load conditions and also maintains regulated voltage and current.

Index Terms—DC–AC converter, distributed generation (DG), quasi-Z-source inverter (q-ZSI), renewable energy source (RES).

I.INTRODUCTION

More Efforts are now being put into distributed power generation of renewable energy sources (RESs), such as photovoltaic (PV), wind power and fuel cells which are sustainable and environmental friendly. Practically, several distributed generations (DGs) consist of distributed power grid and further construct micro grid with local loads and managements. To ensure proper performance of the micro grid, DG is usually required to work in two modes: stand-alone or grid connected [1-2]. As an interface between RES and distributed power grid, the performance of power electronic converters becomes critical. Z-Source inverters are new single-stage electronic power converters with both voltage buck and boost capabilities that have been proposed for use in photovoltaic energy conversion systems and motor drives with a front-end diode rectifier [3]-[4]. Compared with traditional voltage-source (VS) and current-source (CS) inverters, the sole difference of a Z-source inverter is its X-shaped impedance network implemented using a split-inductor and capacitors, connected between the input power source and inverter circuit, for a VS type Z-source inverter [5]. This unique impedance network allows both switches within the same phase-leg to be turned ON simultaneously to introduce a shoot through (dc bus short-circuiting) state for boosting the inverter output voltage. Multiple shoot-through states can conveniently be introduced to traditional continuous and discontinuous pulse-width modulation (PWM) strategies for controlling a Z-source inverter with all steady-state performance merits of these PWM strategies retained [6-7].

Quasi-Z-source inverter (qZSI) topology has been introduced recently to overcome some of the shortcomings of the Z-source inverter. The qZSI offers several advantages over the Z-source inverter such as continuous input current, reduced components rating, higher reliability, and simple control strategy. This topology of the inverter is identified as one of the most suitable power conditioning interface between the PV generation system and the grid [8-9]. This paper presents an improved power circuit topology of qZSI where one capacitor of the quasi-Z-source network is replaced by storage batteries, thus flexible power conditioning functionalities can be achieved. In the proposed structure, the load can be isolated or it can be a micro grid or a full scale grid. Given the condition that the battery is within its valid charge or discharge status, MPPT can be accomplished by sending the captured extra power – to the battery, or the output power can be maintained for period of time by extracting absent power – from the battery [10]. It is much important for large-scale PV systems interfacing the power grid, where stable and sustainable energy supply is always demanded, while contrastively PV cell's output power varies accordingly with temperature and solar irradiation.

The Z-source inverter (ZSI) has been reported suitable for residential PV system because of the capability of voltage boost and inversion in a single stage. Recently, four new topologies, the quasi-Z-source inverters (q-ZSI), have been derived from the original ZSI [11]. This paper analyzes one voltage fed topology of these four in detail and applies it to PV power generation systems. By using the new quasi Z-source topology, the inverter draws a constant current from the PV array and is capable of handling a wide input voltage range [12]. It also features lower component ratings and reduced source stress compared to the traditional ZSI.
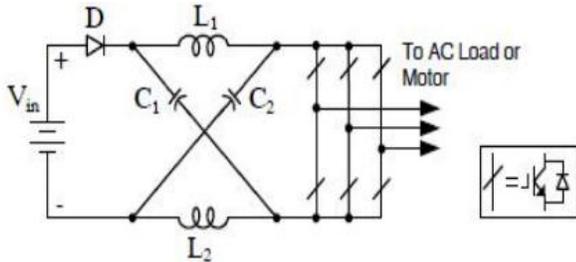
Fig.1. Voltage fed Z-source inverter
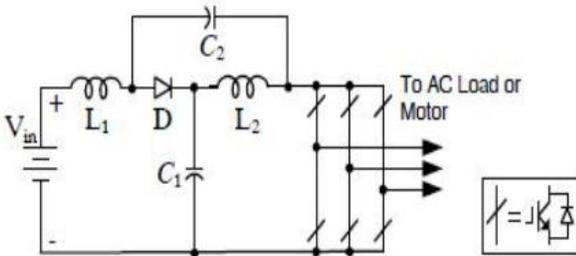
Fig.2. Voltage fed quasi-Z-source inverter

Figs. 1 and 2 shows the traditional voltage fed ZSI and the proposed voltage fed q-ZSI respectively. In the same manneras the traditional ZSI, the q-ZSI has two types of operational states at the dc side, the nonshoot-through states (i.e. thesix active states and two conventional zero states of the traditional VSI) and the shoot-through state (i.e. both switchesin at least one phase conduct simultaneously).Fig. 3 shows the proposed q-ZSI in the PV power generation system. It connects the PV arrays and outputs three phase 50 Hz, 330 V ac to resistive loads, which is the standard utility level. A three-phase LC Filter connected in right after the inverter bridge to get 50Hz sinusoidal ac outputs.
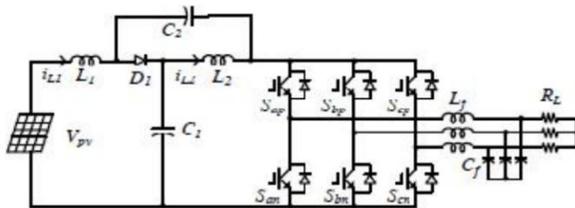
Fig.3. QZSI in the PV power generation system

II. DYNAMICMODELING OF THE QUASI-Z-SOURCENETWORK
A. Small-Signal Model of the Quasi-Z-Source Network

By applying a two-stage control strategy to be presented later on, the control of dc side and that of ac side are decoupled. With an intention to provide a comprehensive mathematical guide in terms of the q ZSI dc-side modeling, small-signal analysis is used for the studies, along with detailed derivations. For general analysis purposes, input voltage v_{in} is chosen as system input, to which input current I_{in} is related. This is because RES does not have as stiff output characteristics as an ideal

voltage source or current source. The relationship of V_{in} and I_{in} will be determined by specified energy source nature. For dc-side modeling, the three-phase inverter bridge and external ac load are represented by a single switch and a current source connected in parallel.Considering the asymmetric quasi-Z-source network, there are four state variables: the currents through two inductors$i_{L1}$and i_{L2} and the voltages across the capacitors v_{C1}andv_{C2}. Independent load current i_{load} serves as another input (disturbance) of the quasi-Z-source network. Choose v_{C1} and $i_{L1}(=i_{in})$as the output of the studied system. For simplification, assume that $C=C_1=C_2$,$L=L_1=L_2$, the stray resistances of inductors $r=r_1=r_2$, and the equivalent series resistances of capacitors $R=R_1=R_2$. Define shoot-through interval T_0, non-shoot through interval T_1, and switching period $T_s=T_0+T_1$; thus, the shoot-through duty ratio is$d0=T_0/T_s$. At the shoot-through state the capacitors transfer their electrostatic energy to magnetic energy stored in the inductors. The dynamic state equations of the quasi-Z-source network are given as

$$\frac{d\mathbf{x}}{dt} = \mathbf{A_1}\mathbf{x} + \mathbf{B_1}\mathbf{u}$$

(1)

Where

$$\mathbf{x} = [i_{L1}\ i_{L2}\ v_{C1}\ v_{C2}]'$$

$$\mathbf{A_1} = \begin{bmatrix} -((r+R)/L) & 0 & 0 & 1/L \\ 0 & -((r+R)/L) & 1/L & 0 \\ 0 & -(1/C) & 0 & 0 \\ -(1/C) & 0 & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_1} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1/L & 0 & 0 & 0 \end{bmatrix}'$$

$$\mathbf{u} = [i_{load}\ v_{in}]'.$$

At the non-shoot-through states the dc power source, as well as the inductors, charges the capacitors and powers the external ac load, boosting the dc voltage across the inverter bridge. The dynamic state equations are shown as

$$\frac{d\mathbf{x}}{dt} = \mathbf{A_2}\mathbf{x} + \mathbf{B_2}\mathbf{u}$$

(2)

$$\mathbf{A_2} = \begin{bmatrix} \frac{-(r+R)}{L} & 0 & -\frac{1}{L} & 0 \\ 0 & -\frac{(r+R)}{L} & 0 & -\frac{1}{L} \\ \frac{1}{C} & 0 & 0 & 0 \\ 0 & \frac{1}{C} & 0 & 0 \end{bmatrix}$$

$$\mathbf{B_2} = \begin{bmatrix} \frac{R}{L} & \frac{1}{L} \\ \frac{R}{L} & 0 \\ -1/C & 0 \\ -1/C & 0 \end{bmatrix}.$$

Using state-space averaging, the dc-side model of q-ZSI can be obtained as shown in

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$$\frac{d\mathbf{x}}{dt} = \mathbf{Ax} + \mathbf{Bu} \qquad \mathbf{y} = \mathbf{Cx} + \mathbf{Du} \tag{3}$$

$$A = d_0A_1 + (1-d_0)A_2, \quad B = d_0B_1 + (1-d_0)B_2,$$

$$y = \begin{bmatrix} v_{C1} \\ i_{L1} \end{bmatrix}, C = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix}, \text{ and } D = \begin{bmatrix} 0 \\ 0 \end{bmatrix}.$$

To obtain the small-signal model, perturbations $\hat{d}_0$, $\hat{v}_{in}$, and $\hat{i}_{load}$ are introduced with d_0, v_{in} , and i_{load} , respectively, which, in turn, cause variations $\hat{i}_{l1}$, $\hat{i}_{l2}$, $\hat{v}_{c1}$, and $\hat{v}_{c2}$ in the dynamic state variables of i_{L1}, i_{L2}, v_{C1}, and v_{C2}. Substituting $x=X+\hat{x}$ (where X and $\hat{x}$ are the dc terms and perturbations of the variables $x=d_0$, v_{in}, i_{load}, i_{L1}, i_{L2}, v_{C1}, and v_{C2}) into (3), considering the principles of inductor volt–second and capacitor charge balance in steady state and ignoring the second-order elements, the Laplace-transformed transfer functions of the multi-input multi output quasi-Z-source network can be derived.

$$G_{\hat{d}_0}^{\hat{v}_c}(s) = \frac{\hat{v}_C(s)}{\hat{d}_0(s)}\Bigg|_{\substack{\hat{i}_{load}(s)=0 \\ \hat{v}_{in}(s)=0}}$$

$$= \frac{(V_{C1}+V_{C2}-RI_{load})(1-2D_0)+(I_{load}-I_{L1}-I_{l2})(Ls+r+R)}{LCs^2+C(r+R)s+(1-2D_0)^2} \tag{4}$$
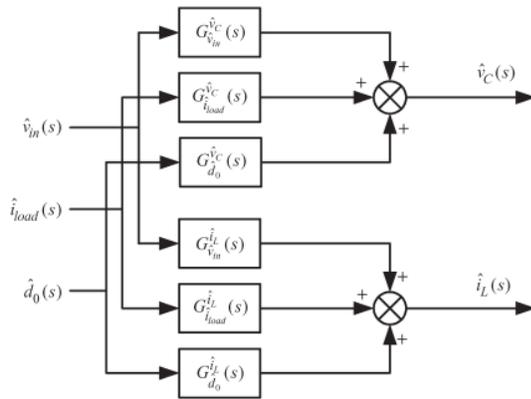
Fig.4. Small-signal model of the quasi-Z-source network.

The small-signal model of the quasi-Z-source network is shown in Fig.4. Assuming any two of the system inputs to be zero, one can get small-signal transfer functions from the remaining to the state variables.

B. Dynamic Characteristics of the Quasi-Z-Source Network

According to the small-signal model, the transfer functions from d_0 to capacitor voltages v_{C1} and v_{C2} are identical, denoted as $G_{d_0}^{\hat{v}_c}(s)$ in (4), shown at the bottom of the page. Other transfer functions are given in the Appendix. Based on these equations, the characteristic equation of the quasi-Z-source network can be obtained as

$$s^2 + \frac{r+R}{L}s + \frac{(1-2D_0)^2}{LC} = 0. \tag{5}$$

Equation (5) can be written as the following normalized form:

$$s^2 + 2\xi\omega_n s + \omega_n^2 = 0 \tag{6}$$

Where

$$\omega_n = \frac{1-2D_0}{\sqrt{LC}}$$

is the natural frequency a

$$\xi = \frac{r+R}{2(1-2D_0)}\sqrt{\frac{C}{L}}$$

is the damping ratio. Among these equations, D_0, I_{load}, V_{C1}, V_{C2}, I_{L1}, and I_{L2} represent a given equilibrium point nearby where the system can be linear zed. Equation (5) indicates that, aside from the parameters of the quasi-Z-source network (i.e., L, C, r, and R), D_0 is also one factor to determine the system dynamic characteristics. To make a clear map of the dynamic characteristics of the quasi-Z-source network, various root loci of the transfer function $G_{d_0}^{\hat{v}_c}(s)$ are studied by parameter sweep of L, C, and D_0. There is a right-half plane (RHP) zero in $G_{d_0}^{\hat{v}_c}(s)$ which is learned to imply high gain instability and impose control limitations. A feedback should be carefully designed with an adequate phase margin. It can be observed from Fig. 5(a) that, along with increasing L, zeros are pushed from the right half-plane toward the origin along the real axis, indicating an increasing degree of non minimum-phase undershoot (e.g., capacitor voltage dips before it rises in response to d_0 rising). Similar conclusion can be reached with an increase in D_0 from Fig. 5(c). However, the variation of C has very little influences on the RHP zeros seen from Fig. 5(b). Additionally, the conjugated pole pairs are observed to move toward the origin along with the increase in L, as shown in Fig. 5(a). The feedback control performance is predicted deteriorated with the increase in L. Moreover, increasing in L causes smaller damping ratio and decreasing natural frequency, which is consistent with (6). On the other side, the conjugated pole pairs can be seen shifting toward the real axis with the increase in D_0 or C, implying increasing system settling time and decreasing natural frequency, which is consistent with (6) too. The placement of poles and zeros gives an important guideline for passive component selection of q-ZSI design: Although large L and C are preferred for low steady-state current and voltage ripples, tradeoffs need to be made for proper transient responses.

Simple boost:

$$M \leq 1 - D_0 \tag{7}$$

Maximum constant boost:

$$M \leq \frac{2}{\sqrt{3}}(1-D_0) \tag{8}$$

Maximum boost:

$$M \leq \frac{2\pi}{3\sqrt{3}}(1 - D_0) \qquad (9)$$

Symbol D_0 is used to imply a steady state. As a result, changing either 0 or M will impose a limitation on the other parameter, which makes it become challenging to design the controller. On the other hand, to use a larged0but a small M for the same voltage gain is not cost effective, because this increases voltage stress across devices which results in high component rating. Notice that, in steady state, the peak phase voltage of the inverter can be written as

$$v_{p\_peak} = \frac{1}{2} \cdot \frac{V_{in}}{1 - 2D_0} \cdot M \qquad (10)$$

As described the relationship between the capacitor voltage and the input voltage can be expressed as

$$V_{C1} = \frac{1 - D_0}{1 - 2D_0} V_{in} \qquad (11)$$

Dividing (11) by (10) results in

$$\frac{V_{C1}}{v_{p\_peak}} = \frac{2(1 - D_0)}{M} \qquad (12)$$

Referring to (7)–(9), the capacitor voltage inequality can be derived assimple boost:

$$V_{C1} \geq 2v_{p\_peak} \qquad (13)$$

Maximum constant boost:

$$V_{C1} \geq \sqrt{3}v_{p\_peak} \\ \approx 1.73v_{p\_peak} \qquad (14)$$

 (13)–(15) imply that, to avoid overlap of d_0 and M, one can simply keep voltage on C_1 above twice the output peak voltage at the most. Since $v_{p\_peak}$is fixed in most DG applications, it is possible to control the capacitor voltage in a constant value with input variation. In a closed-loop control, one can keep a minimum capacitor voltage referring to (13)–(15); then, the minimum D0 and the maximum M can be inherently achieved, which lead to the lowest voltage stress across devices. For DG applications, the q-ZSI is expected to be able to work in both stand-alone and grid-connected modes. To operate in stand-alone mode, DGs in parallel usually construct the distributed power grid in a master–slave manner or all serve as virtual synchronous generators. Thus, the master q-ZSI or all q-ZSIs in parallel need to follow a voltage reference to maintain local power balance and valid system voltage and frequency. To operate in grid-connected mode or serve as the slave DG in stand-alone mode, since the output voltage is arbitrarily given by the utility or master DG, the q-ZSI should follow a current

reference to control the output active and reactive power. To an end, the controlled q-ZSI turns out two essentially different output characteristics: a voltage source or a current source. The next section will discuss the controller design for both types, respectively. Transition between the two operating modes for DG applications can be made on the micro grid level, where power rebalance and resynchronization are the most concerned aspects. With system reconfiguration by break actions and necessary protections, q-ZSIs can make transition between
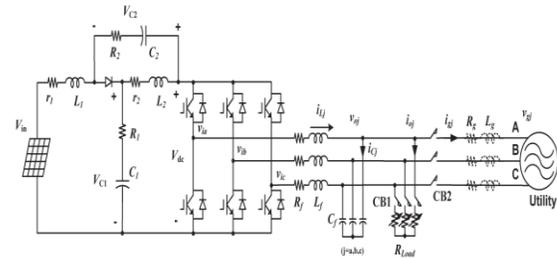
Fig.6. System Configuration of the Proposed Q-ZSI for DG Applications.

Voltage control and current control with precise output power management, relying on modern communication approaches, such as power line or wireless communication.

IV.TWO-STAGECONTROLMETHODOLOGY FOR QZSI-BASEDDG

Fig.6 shows the overall system configuration of the proposed q-ZSI, where L_f, R_f, and C_f are the inductance, capacitance, and stray resistance of the filter, respectively, and v_{oj},i_{Cj},v_{ij},i_{Lj},i_{oj}, and i_gj are the load voltage, capacitor current of the filter, output voltage of the inverter, inductor current of the filter, load current, and grid current, respectively, all in three phases(j=a, b, c). C_B stands for circuit breaker. C_{B1} is ON and C_{B2} is OFF when the q-ZSI works under voltage control mode and C_{B1} is OFF and C_{B2} is ON when the q-ZSI is under current control mode. It should be pointed out that, although one q-ZSI with variable resistive load is used to demonstrate the voltage control strategy, the controller design principle is still applicable to q-ZSIs that are connected in parallel.

A. Controller Design for Output Voltage Control

Through the decoupling capacitor, control of dc side and that of ac side are executed separately, as shown in Fig.7. Pulses generated by the dc-side controller (for voltage boost) and the ac-side controller (for dc–ac conversion) are combined together by logical OR to fire six insulated-gate bipolar transistors, assuming "1" is ON and "0" is OFF. The overlap of d0 and M can be avoided by setting thereference of the capacitor voltage v∗C_1 based on (13)–(15), depending on the different boost control methods involved. For the dc-side control, capacitor voltage v_{C1} is

measured and fed back. The dynamics of v_{C1} caused by d_0 can be obtained via transfer function $G_{d_0}^{\hat{v}_c}(s)$, as shown in (4). Linear approximation of the RES output characteristics can be accomplished by the small-signal modeling. Taking PV application as an example, a normal operation for voltage control generally starts from the open-circuit voltage of PV panels Voc and stays at operating points where VPV>VMPP, where VMPP is the voltage at the maximum power point (MPP). Based on the
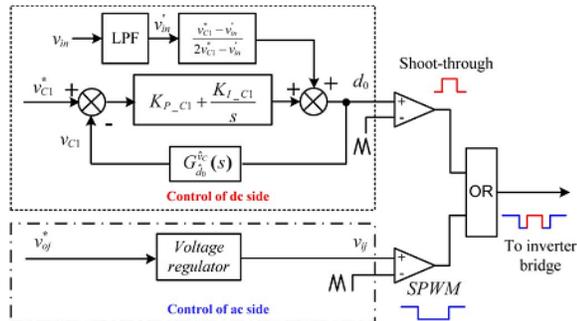
Fig.7. Two-stage control method of the q-ZSI for output voltage control.

Linear approximation, a proportional–integral (PI) controller assisted with a feed forward d_0 is used as the shoot-through compensator. The feed forward d_0 is determined according to the inherent relationship of v_{C1} and v'_{in} in steady state

$$d_0 = \frac{v_{C1}^* - v'_{in}}{2v_{C1}^* - v'_{in}}$$

(16)

Where v'_{in} is the input voltage v_{in} after a low-pass filter. Based on the small-signal modeling, PI parameters for the v_{C1} control loop can be decided. In order to prevent the clashes between the dynamics of ac and dc sides, the dc-side dynamics should be made considerably slower. This could be supported by having a relatively lower bandwidth in the dc-side voltage loop. In a three-phase system, fundamental frequency components are commonly transformed to dc components via d−q transformation, where a simple PI compensator can be applied with good performance. Another choice is to design the controller in stationary frame. Without d−q transformation, the designed controller is applicable to single-phase system too. This paper employs a typical multi loop controller in stationary frame as the voltage regulator,
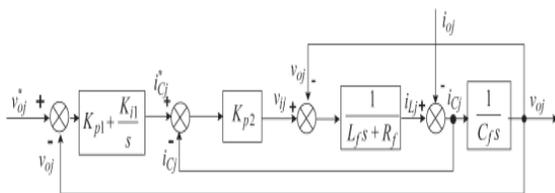
Fig8. Control block diagram of the voltage regulator for q-ZSI.
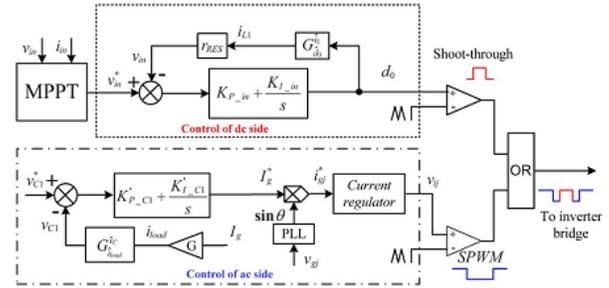
Fig. 9. Two-stage control method for grid-connected-q-ZSI-based PV powerconditioning system.

As shown in Fig.8. From Mason's gain rule, the closed-loop transfer functions can be obtained based on which the ac-side controller can be designed properly. In this implementation, K_{p2} was selected based on the principle of keeping the closed loop gain 0 dB from system output frequency (60 Hz) to half of the switching frequency (5 kHz in this implementation), where K_{p2}=30. Considering the time delay e−sT s caused by the digital implementation, K_{p2} would be less in practice to maintain a sufficient phase margin for stable performance. The outer voltage loop control parameters K_{p1} and K_{i1} are selected with the compromise that the crossover frequency is low enough to remove the switching harmonics but a sufficiently high bandwidth is retained to have fast response and perfect reference tracking. In this implementation, K_{p1} is 0.05 and K_{i1} is 300, where the crossover frequency is 200 Hz and the phase margin is 70∘.

B. Controller Design for Output Current Control

Fig.9 shows the overall diagram of the two-stage control method in grid-connected q-ZSI, where pulses from control of dc side and that of ac side are combined in the same manner as in the output voltage control mode. For the ac-side control, capacitor voltage v_{C1} is measured and fed back. The magnitude of the grid current reference I_g^* is generated through a PI compensator according to the error signal of v_{C1}. In the case that $v_{C1}^*-v_{C1}$ is positive, power injected into the grid should be reduced to maintain a constant v_{C1}, so negative PI parameters are used here. Along with the phase angle of the grid voltage given by phase-locked loop, the reference of ac current injected into the grid i_{gj}^* can be obtained. Since grid current magnitude is proportional to the equivalent load current i_{load} in small-signal mode, a coefficient G is used to transfer I_g to i_{load}, which relates to inverter operating condition (e.g., modulation index, shoot-through duty ratio, and the power factor). Consequently, the dynamics of v_{C1} caused by load change can be obtained via transfer function $G_{i_{load}}^{\hat{v}_c}(s)$,
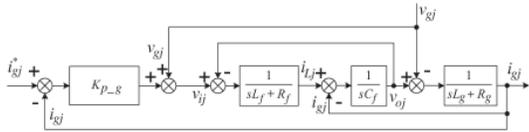
Fig 10 Control block diagram for output current of q-ZSI.

As shown in the Appendix. Similar to voltage control mode,V^*_{C1}should be selected according to (13)–(15), depending on the specific boost control method engaged. Various control methods for the grid-connected inverter can be applied as the current regulator. This project employs a conventional method in stationary frame, which is applicable to single-phase system too. It needs to be noticed that, for the proposed three-phase three-wire system, only two controllers are necessary since the third current is given by the Kirchhoff current law. Fig. 10 shows the block diagram of the current regulator, where a current feedback loop, along with grid voltage feed forward, is used. The grid voltage feed forward part guarantees a good disturbance rejection effect. Based on Mason's gain rule, transfer functions of control to output can be derived, according to which K_{p_g} can be decided. In this implementation, $K_{p\_g}$is set to 0.06, the crossover frequency is 1 kHz, and the phase margin is 89∘.As long as v_{C1} is kept constant by the ac-side controller, reference tracking of input voltage can be achieved at the dc side by adjusting d_0, referring to the steady-state derivation (11). The reference of the input voltage V^*_{in} of the q-ZSI is given by output power command, which, in most cases, could be the MPP tracking (MPPT). The PI controller is used to regulate the shoot-through duty ratio d_0. Through $G^{\hat{v}_c}_{d_0}(s)$, the variation of d0 gives a change on input current i_{L1}, which can be further transferred to input voltage by the impedance of the RES$_{rRES}$. Based on the small-signal modeling, PI parameters for the v_{in} control loop can be decided. In order to ensure valid operation, PI parameters of the dc side are selected with relatively slower response compared to the control loop for v_{C1}. This is becaused0is adjusted to track V_{in} in the output current control case, instead of regulating vC1for output voltage control. Therefore, MPPT algorithm that sets operating points backward and forward around the MPP can be applied effectively.

V. PRINCIPLE OF BLDC MOTOR

BLDC engine comprises of the perpetual magnet rotor and an injury stator. The brushless engines are controlled utilizing a three stage inverter. The engine obliges a rotor position sensor for beginning and for giving legitimate compensation arrangement to turn on the force gadgets in the inverter extension. In light of the rotor position, the force gadgets are commutated consecutively every 60 degrees. The electronic compensation takes out the issues connected with the brush and the commutator plan, in particular starting and destroying of the

commutator brush course of action, along these lines, making a BLDC engine more rough contrasted with a dc engine. Fig.11 demonstrates the stator of the BLDC engine and fig.12 shows rotor magnet plans.
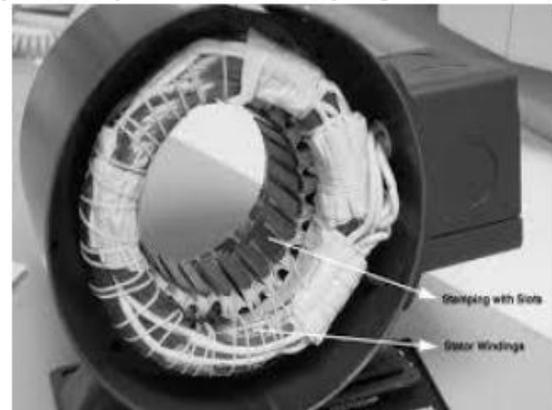
Fig.11. BLDC motor stator construction

Fig.12. BLDC motor Rotor construction.

The brush less dc engine comprise of four fundamental parts Power converter, changeless magnet brushless DC Motor (BLDCM), sensors and control calculation. The force converter changes power from the source to the BLDCM which thus changes over electrical vitality to mechanical vitality. One of the remarkable highlights of the brush less dc engine is the rotor position sensors, in view of the rotor position and order signals which may be a torque charge, voltage summon, rate order etc; the control calculation s focus the entryway sign to every semiconductor in the force electronic converter.

The structure of the control calculations decides the sort of the brush less dc engine of which there are two principle classes voltage source based drives and current source based drives. Both voltage source and current source based commute utilized for perpetual magnet brushless DC machine. The back emf waveform of the engine is demonstrated in the fig. 13. Be that as it may, machine with a non-sinusoidal back emf brings about diminishment in the inverter size and lessens misfortunes for the same influence level.
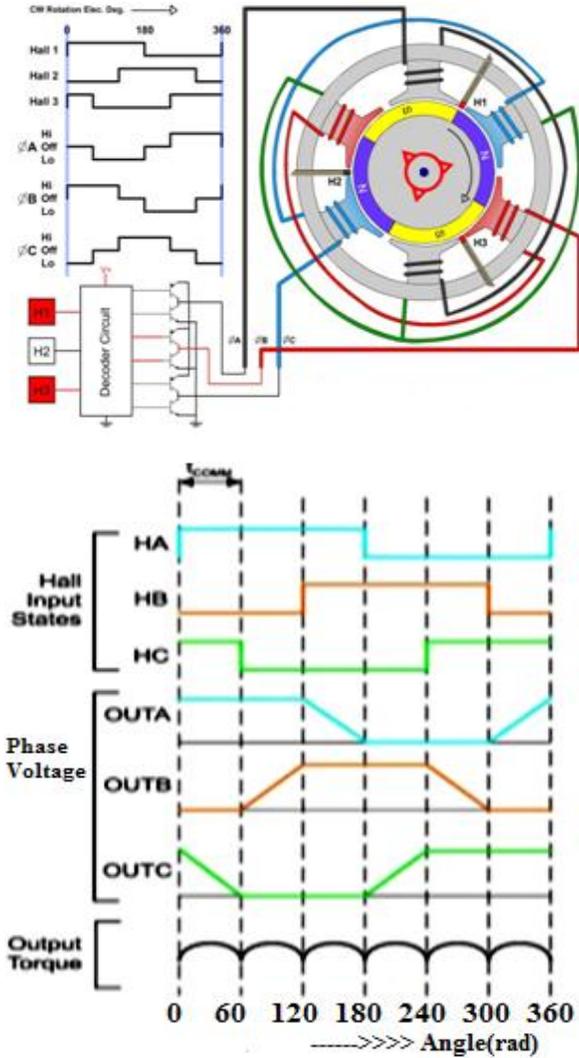
Fig.13.Four-Pole Brushless motor, Hall signals & Stator voltages Commutation, drive and winding timings

VI.MATLAB/SIMULINK RESULTS
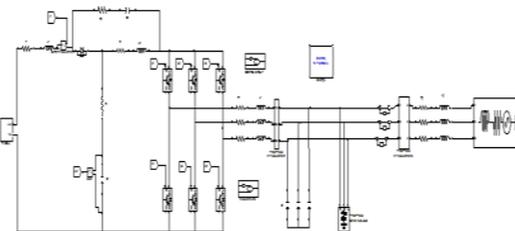
Fig.14 shows the Matlab/simulink model of CCM QZSI topology.
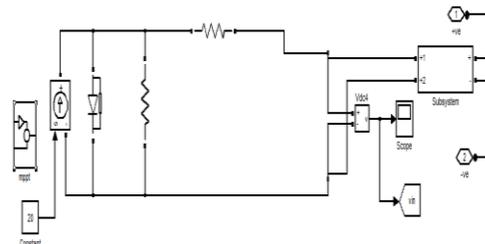
Fig.15. shows the Matlab/simulink model of PV system.

Fig.16. output voltage waveform of PV system.
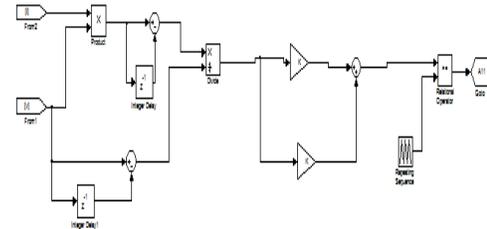
Fig.17.simulink model of MPPT.

Fig.18. Simulation waveforms of the process of MPPT in the grid-connected QZSI at current controlled mode
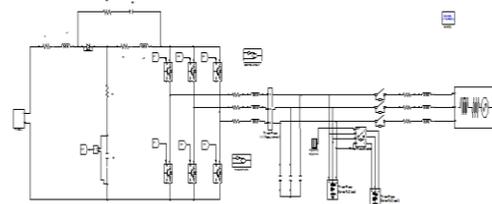
Fig.19. shows the Matlab/simulink model of VCM QZSI topology.
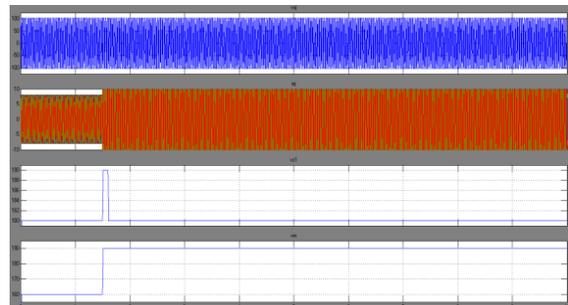
Fig.20. Simulation waveforms of the process of MPPT in the grid-connected QZSI at increasing voltage controlled mode
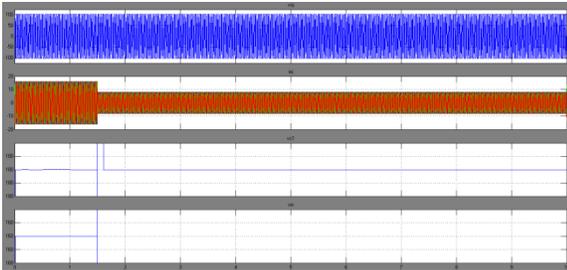
Fig.21. Simulation waveforms of the process of MPPT in the grid-connected QZSI at decreasing voltage controlled mode
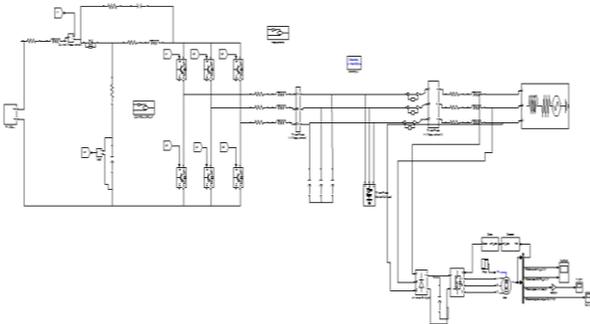
Fig.22. Matlab/simulink model of proposed converter with BLDC Drive.
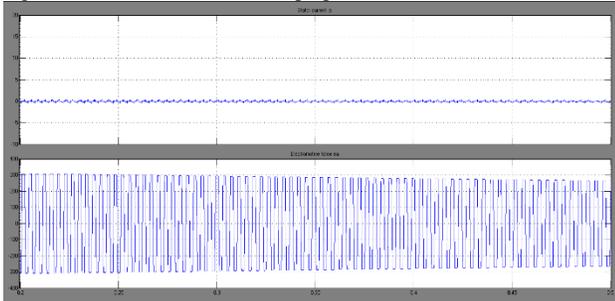
Fig.23.stator current and electromotive force of the BLDC motor.
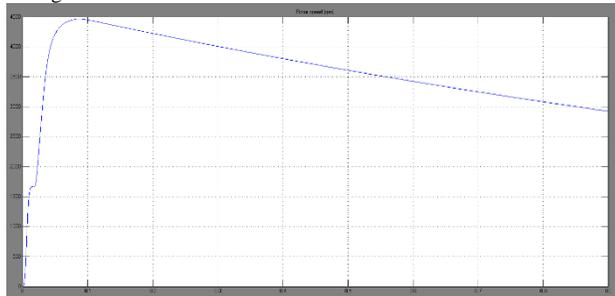
Fig.24.Speed of BLDC motor.

Fig.25.Electromagentic Torque.

VII.CONCLUSION
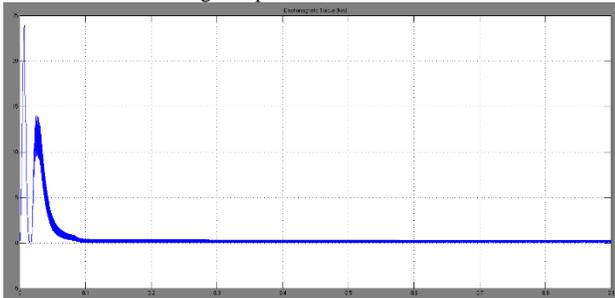
This paper presents detailed analysis on Z-source inverter control to study its transient behavior. For dc analysis, both small-signal and signal-flow-graph methods are used with an intention of developing a comprehensive guide on Z-source impedance modeling. A two-stage control method for the qZSI-based DG is implemented. The dynamic characteristics of the qZSI network have been investigated through small-signal analysis. The analysis is done using both shoot through mode and non-shoot through mode for Z-Source and Quasi Z-Source separately. Thus simultaneous control of shoot through duty ratio and the modulation index ensure the control objectives achieved. Simulation and experimental results are provided to verify the proposed control approach. This results confirm the effectiveness of the controller, exhibiting good reference-tracking and disturbance rejection characteristics.

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