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VLSI Architecture of Shared Multiplier Scheduling Scheme for Reconfigurable FFT/IFFT Processor

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Abstract: - ***This paper proposes VLSI Architecture of SMSS (Shared Multiplier Scheduling Scheme) for Reconfigurable FFT/IFFT processor. This architecture provides flexibility of selecting various FFT sizes (2, 4, 8, 16, 32, 64, 128 and 256) length, so that the hardware complexity of processor is reduced. The multipliers in SMSS based FFT processor are replaced with Vedic multiplier to improve speed of calculation. The proposed FFT/IFFT processors based on SMSS are designed using XILINX ISE Tool and modeled in Verilog HDL. The synthesis results shows that Area is reduced by 17% and speed is increased by 11%.In addition the proposed processor can be extended to any FFT sizes using additional stages.***

Keywords*: **FFT (Fast Fourier Transform), reconfigurable FFT, Vedic multiplier, MRMDC (mixed radix multipath delay Commutator), OFDM (Orthogonal Frequency Division Multiplexing).***

I. Introduction

FFT/IFFT processors play an important role in signal processing and image processing applications. Such a applications require high speed FFT/IFFT processors to meet continuing demands for higher data rates. For example, in OFDM systems the IFFT computation is required in transmitter, while FFT is performed in receiver. There is no need to implement IFFT processors separately because the IFFT processor is derived from FFT processor by taking complex conjugate of input and output data and then dividing the conjugate of the FFT output by FFT size. So the role of FFT processors in dealing with OFDM systems requires low power and high speed processors. For implementing such processors, several architectures are proposed for reducing hardware complexity. The FFT processors are divided mainly into Memory based, Reconfigurable, and Pipelined FFT processors .Memory based architectures [1], [2] are proposed to achieve small area. The Application specific instruction set processors [3], [4] have been proposed to meet flexibility for FFT computation. Reconfigurable FFT processors [5] are proposed to select various FFT sizes on processor so that hardware complexity is reduced. The pipelined processors [6] are used for achieving high throughput rate. Pipelined processors are classified into SDC (single-path delay commutator), SPF (single-path feedback), MDF (multipath delay feedback), and MDC (multipath delay commutator).From the above, MDC architectures provides high throughput rate and simple synchronizing control using multidata paths. In the MDC architectures [7], if the radix size is high then high throughput rate is achieved. For example to achieve higher data rate radix-8, radix-16 and above are used. But in OFDM systems the typical FFT sizes are 128,256 but radix-8 algorithm can't suitable for 128/256 FFT sizes because it is not power of 8. So mixed radix algorithm is used. So mixed radix FFT/IFFT processors are required to meet computational demands of OFDM systems. The MRMDC architecture [8] in pipelined processors employing eight parallel data paths operates at higher clock frequency to satisfy computation demands. SMSS based FFT/IFFT processors [9] in MRMDC architecture provides area efficiency and higher data rate. The SMSS based FFT processors reduces the number of complex multipliers by moving the moving the multipliers

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from second stage to first stage for 128/256 point FFT processor.

This paper proposes flexibility in selecting FFT sizes i.e. reconfigurable FFT/IFFT processor [5] based on SMSS algorithm [9], so that hardware complexity is further reduced .The multipliers in the existing processor are replaced with Vedic multiplier to improve the speed of computation. The remainder of this paper is organised as follows. Section II describes the MRMDC architecture [8] .Section III provides the details of the existing SMSS based FFT/IFFT processor. Section IV gives the information about the proposed Architecture of SMSS for reconfigurable FFT/IFFT processor (FFT size: 2, 4, 8, 16, 32, 64, 128 and 256). Section V presents the design and implementation of proposed FFT/IFFT processor with Vedic multiplier. Finally conclusion is presented in Section VI.

II. MRMDC Architecture

MRMDC (mixed radix multipath delay commutator) architecture [8] uses mixed radix algorithm and multipath data bits. The mixed radix algorithm with assumptions is described as follows. The N-point DFT (Discrete Fourier Transform) is defined as

$$X(k) = \sum_{n=0}^{N-1} x(n).W_N^{nk}, k=0,1,...,N-1 \quad (1)$$

Where x (n) =input sequence, X (k) =output sequence, N=transform length

W_N^{nk}= N^{th}primitive root of unity (twiddle factor)

$$W_N^{nk} = e^{-jnk(\frac{2\pi}{N})}$$

$$= \cos(2\pi nk/N) - j\sin(2\pi nk/N) \quad (2)$$

When the FFT size is not a power of radix r, then mixed radix algorithm should be used.

For example if

N=256

n = 64n1+n2, $0 \le n1 \le 4$, $0 \le n2 \le 64$

k = k1+4k2, $0 \le k1 \le 4$, $0 \le k2 \le 64$ (3)

Substituting (3) in (1)

X (k) = X (k1+4k2)

$$= \sum_{n2=0}^{63} \sum_{n1=0}^{3} x(64n1+2).W_{256}^{(64N1+N2)(K1+4K2)}$$

$$= \sum_{n2=0}^{63} \{BF4(n2,k1)\} W_{64}^{n2k2} \quad (4)$$

The 256 point mixed radix FFT algorithm can be derived from (4) by decomposing the remaining 64-point DFT into 8-point DFT twice.

The MRMDC architecture is explained using 128/256-point MRMDC FFT/IFFT processor [8] .The architecture consists of BU's, delay commutators, and twiddle factor multipliers. In the first stage, the radix-2/4 BU can perform one radix-4 or two radix-2 operations to compute the 128 and 256-point FFTs. There are three stages based on radix-2, radix-4, and radix-8 algorithms. The input sequence of single path is divided into eight data paths.

III.SMSS based FFT/IFFT processor

SMSS based FFT/IFFT processor with eight parallel MRMDC architecture gives high throughput and low hardware complexity. In the existing processor the first stage uses shared multipliers and second stage uses the modified radix-8 butterfly units. The architecture of existing SMSS based 128/256-point FFT/IFFT processor [9] is shown in below Fig .1.

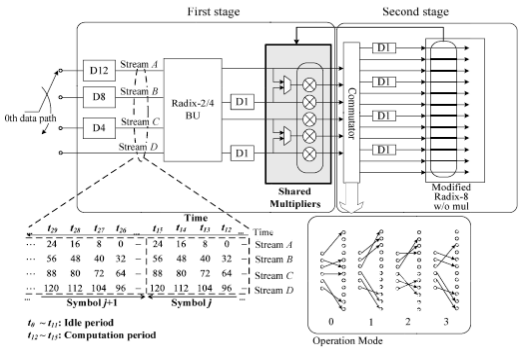

Fig.1. SMSS based 128/256 point FFT processor

In the first stage in fig.1, the radix-2/4 BU can perform two radix-2 butterfly computations. The structure performs complex multiplications for second stage before the delay commutator using shared multipliers. In the first stage, the input sequence of each data-path is

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divided into four data streams. Based on the SMSS based algorithm [9], the processor achieved area efficiency when compared with previous architectures. For a single FFT size processor it is suitable, but there is a case where variable size FFT processor is required. So we need a processor that supports reconfigurability feature in order to select multiple FFT sizes on single processor. Section IV presents architecture of reconfigurable FFT processor for the existing processor.

IV. VLSI Architecture of SMSS for Reconfigurable FFT/IFFT Processor

The existing SMSS based FFT/IFFT processor [9] can support 128/256 point FFT size at a time only. Variable size FFT processor is required to support multiple FFT sizes. Reconfigurable FFT/IFFT processor provides such a flexibility of selecting any FFT sizes on single processor design without going to each FFT size processor. The existing work can be extended to support various FFT sizes (2, 4, 8, 16, 32, 64, 128 and 256) lengths using reconfigurable FFT processor. The reconfigurable feature is added to the existing specific size FFT processor using multiplexer as shown in fig.2.

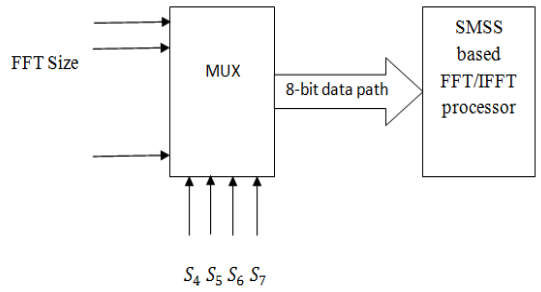

Fig.2. Block Diagram

The re-configurability for the SMSS based FFT/IFFT processor reduces the hardware complexity. The multipliers used in the SMSS based FFT/IFFT processors are replaced with Vedic multipliers, so as to improve performance .Vedic multipliers follows ancient set of rules, so that the multiplication operations are efficient in time. Vedic multipliers [10] are based on sixteen sutras. Of these URDHVA TRIYAKBHYAM (vertically and crosswise) is sutra that supports all types of multiplications. So that the speed of calculation is further improved using Vedic multipliers.The implementation and synthesis report gives the performance details of proposed processor in section -V.

V. Results and Comparison

The proposed SMSS based reconfigurable FFT/IFFT processor using Vedic multiplier is designed using Xilinx ISE13.2 Tool and modeled in Verilog HDL. The proposed FFT processors use Vedic multiplier [10] (URDHVA TRIYAKBHYAM sutra) to improve computation speed. The synthesis result shows the area efficiency of propose processor and computation speed improvement. The proposed processor is simulated using Modelsim10.1 simulator. The functional verification of design is done using MATLAB tool. The RTL schematic and simulation results are shown below as Fig.3, Fig.4.

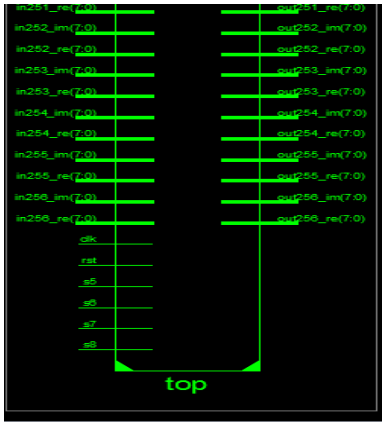

Fig.3. RTL schematic of proposed SMSS based reconfigurable FFT processor

The RTL schematic of proposed processor contains four selection lines ($S_5S_6S_7S_8$) and clock rate 126MHz with 256 complex inputs and complex outputs. The simulation results of proposed processor with selection lines $S_5S_6S_7S_8$ =0000 and inputs (in_re1, in_re2,in_re3,in_re4=1 others=0) as shown in fig.4.

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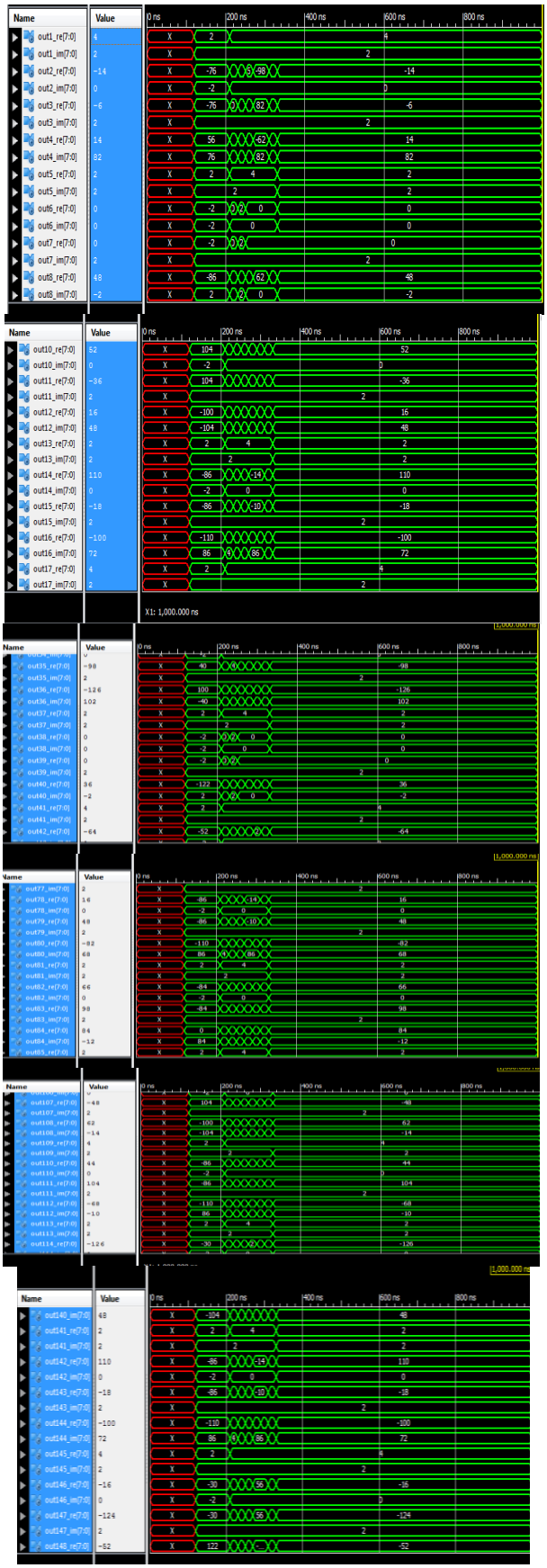

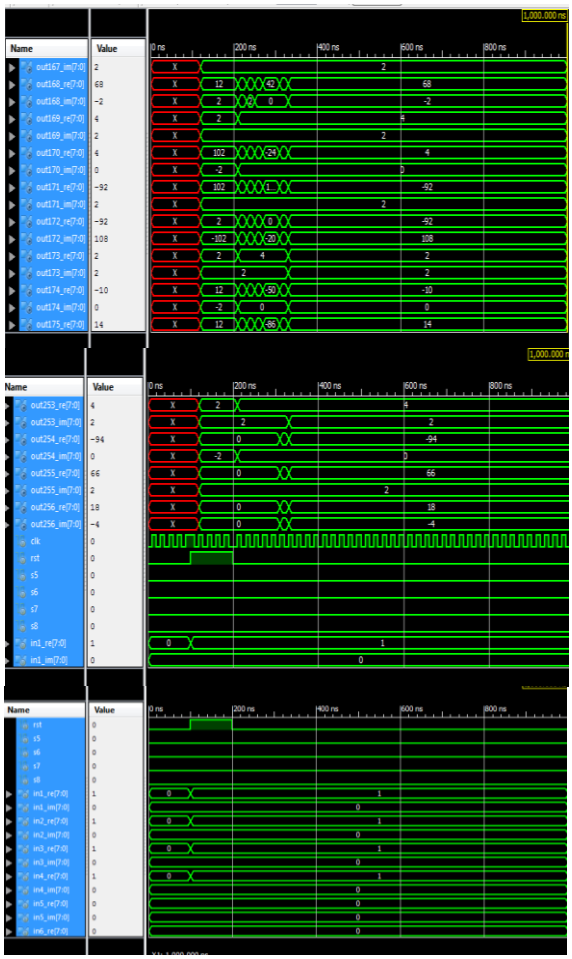

Fig.4. 256-point SMSS based reconfigurable FFT processor using Vedic multiplier.

Assuming that the processor have same throughput rate i.e. (64*clock rate) =8.036GS/s at 126 MHz clock rate. The hardware complexity and computation speed are compared in the performance table. The hardware complexity is compared with the existing SMSS based 256- point FFT processor in terms of ASIC design metric gate count. The equivalent gate count for the proposed processor is derived from the synthesis report of XILINX XST tool.

Table-I: Performance comparison

Technology	SMSS based Reconfigurable FFT(Vedic multiplier)	SMSS based FFT processor	Radix-4 Reconfigurable FFT
No. of Data path bits	8	8	8
Architecture	Pipelined	Pipelined	Pipelined
FFT Size	256	256	256
Clock Rate(MHz)	126	126	126
Delay(ns)	13.423	15.531	29.981
Gate Count	6,23,708	7,60,000	9,35,816

The gate count is calculated by selecting target device as Virtex-6 FPGA. The performance comparison is shown in above Table I.

VI. Conclusion

This paper proposed high speed and low hardware complexity SMSS based reconfigurable FFT/IFFT processor. The reconfigurable FFT processor can reduce the hardware complexity when compared with the existing 256-point SMSS based FFT processor. The proposed Vedic multiplier improves the computation speed. The performance results shows that the proposed reconfigurable FFT processor gives less hardware complexity i.e. area reduced by 17% and speed is increased by 11% with a throughput rate of 8.036GS/s. In addition the proposed architecture can apply any FFT size greater than 256 point using additional stages.

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