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Post Optimization of a Clock Tree for Vigor Give Noise Reduction

[1]RADHAKRISHNA VUNNAM , [2]S.ANIL KUMAR

[1]PG Scholar, Department of ECE, Rao and Naidu Engineering college, Ongole.

[2]Associate professor, Department of ECE, Rao and Naidu Engineering college, Ongole.

ABSTRACT—

The voltage drop incurred within the vigour supply in brand new VLSI chips to is a major hindrance referred to as vigor-provide noise. In sub one-volt give voltage, noise of very few enormous quantities millivolts factors circuit malfunction. The motive for energy provide noise is the quick and simultaneous transistor switching. At the same time the good judgment sign switching is unfold across the entire clock cycle, the switching of the clock tree and the sequential circuits are occurring at the same time, causing excessive local present peaks. The clock related transistor switching is the fundamental contributor to power give noise. This paper proposes to spread the switching of clock tree drivers in an try to decrease the peakcurrent, while preserving the clock sign pleasant and low skew at the some distance finish tree's leaves where the sequential circuits are related. A strategy of mobilephone switching characterization was oncdeveloped for fast computation of peak-current and other indicators parameters. This computation is embedded in a branch and certain tree traversal. We endorse a novel optimization algorithm centered on clock tree delay-invariant branch transformation, replacing low-threshold by means of excessive-threshold and smaller measurement drivers. The algorithm used to be applied in forty nanometers design. We completed a reduction of 50% of clock-tree peakcurrent..

I. INTRODUCTION

The voltage drop incurred in the vigour supply in modern-day VLSI chips to is a principal main issue often called vigour-deliver noise [1]. With the broaden of design complexity, moving from ASIC to approach on a Chip (SoC), and because of the sub one-volt provide voltage, noise of only a few hundreds of thousands millivolts causes circuit malfunction. The clock related voltage switching is the important contributor to vigor provide noise [2]. A wellstructuredclock-tee must deliver high excellent clock sign to the underlying sequential circuits connected at tree's leaves. The clock skew have got to keep within certain limits to ensure proper and robust sequencing of the logic. To make sure speedy switching of the logic, the slew of the signal at tree's leaves need to also be

small ample. The attempt to decrease the peakcurrentdrawn from the power deliver by means of clock-tree cure is hence a delicate task which must be treated carefully to make sure clock signal integrity. Normal logic and sequential circuits are designed to work in nominal power deliver voltage. Unluckily preserving consistent voltage for the duration of operation is comfortably unattainable. TheEnergy network is an RLC circuit and high current peaks will motive various voltage drops at various elements of the network. Once process variability and ambient stipulations come intoconsideration this phenomenon is significantly increasing [2]. All of it involves the simple Ohm low of multiplying peakcurrentvalue by means of the vigor network impedance. The noise can as a consequence be lowered by way of either decreasing the impedance, or averting excessive top-current. Constructing right energy provide network having low-resistance and inductance, and excessive capacitance has been dealt with in lots of research papers [3] and is beyond the scope of this paper.

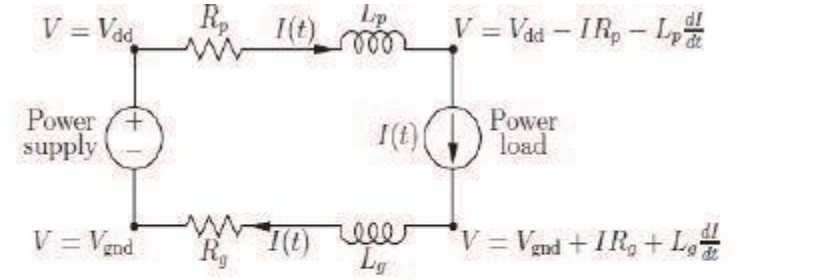


Figure 1. IR drop components based on RLC of Power Distribution Network (PDN) and transistors who are Power load of a SoC

Height-current discount achieves the following pursuits:

 it's lowering the IR drop on die, where the resistance is the principal impedance factor.

 it's reducing the L dI/dt

 term happening on the package deal degree, where inductance is a predominant impedance factor.

 Clock jitter is being lowered considering it's directly affected by IR drop.

 It explanations better utilization of the de-coupling capacitors for the reason that it's lowering the distance of the mighty capacitors used to mitigate the voltage drop. This distance is increasing with dI/dt discount.

II .REVIEW:

Clock signals. With the aid of its very structure, every sink (tree's leaf) has identical course to root, comprising equivalent drivers and interconnecting segments. This ensures (up to on-die versions) equal nominal supply-to-sink latency, and therefore clock-skew is stays very small (nominally). The elegancy of the H-tree structure can also be a supply of enormous power noise. Due to its symmetry, all of the drivers at a given stage of the tree will change at the same time. This result in a revolutionary sequence of present peaks, cumulating to a present pulse whose amplitude is increasing as we growth from supply (tree's root) right down to sinks (tree's leaves), as depicted Three. Pulling down of the cumulative current form will scale down each chip-level and package-stage noise. The former as a result of IR voltage drop discount, whilst the latter which is ruled via LdI /dt can be decreased due to the smoothing of the present pulse profile. It's principal to note that the quantity of present over time (charge) is unchanged, namely, the consumed energy and vigour are unchanged. To make sure mighty signal with low slew, the clock-tree is most often utilising low or nominal threshold voltage transistors, called in VLSI jargon LVT and NVT, respectively. Although suffering of high leakage, their quick transition time ensures low slew of the clock sign at the sinks. Moreover, the uniformity of clock-tree constitution, where every degree of the tree includes equal drivers ensures that sign uniformly propagates to sink. This explanations that the skew at each and every tree's stage being small sufficient such that small skew is guaranteed at tree's sinks, where FFs are linked. The robustness of the clock sign at tree's internal nodes does now not stand for itself; it is serving the integrity necessities at sinks. So an essential query is whether or not this uniformity can accept up, furnished that the integrity at leaves is executed. Here lies the concept of our proposal which breaks this paradigm.

 substitute as many as viable of the LVT and NVT drivers by using LVT ones.

 combo various forms within the same degree of the tree to introduce some "randomness" into tree.

 Use mix of driver sizes on the same degree of the tree, delivering a different measure of "randomness".

 preserve perfect clock sign slew and skew at sinks.

III. CHARACTERIZATION OF CLOCK DRIVERS

The combinatorial algorithm minimizing the peak current is traversing the clock-tree T in a branch-and-bound manner, where every visited node is evaluating its height present, signal extend and its slew. These values are used to make a decision whether backtracking should take place. Evaluating these parameters by a simulation at each and every node is unacceptable as a result of the impractical whole computation time. Rather, we might earlier signify every clock driver after which use composition of traits which is far computational efficient than simulation. It's going to be sown that most effective little accuracy is sacrificed in comparison with simulation. The build of the clock-pressure characterization library takes position offline. We first define the repertoire of library drivers. Each and every driver is then characterized via running large spice transient simulations whose outcome are tabulated for further use within the branch-and-certain algorithm. We display the algorithm on forty nanometers approach science design. For the sake of demonstration the diver library is characterised in a PVT corner the place P normal (procedure is ordinary), Vdd 1.1V and T 25 C . An identical characterization can take location in other corners as good. Characterization is making use of two inputs:

1. A vector of input slew values called Slopein , given in picoseconds

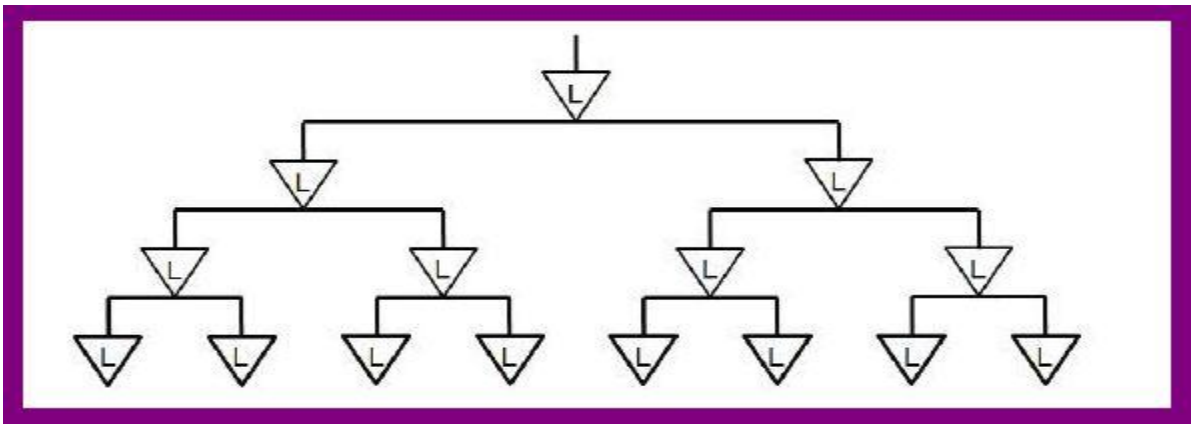
2. A vector of capacitive load values calledCL , given in femtofarads, Every pair of slew-load

Three peak current related parameters incurring at switching are unique

THE ALTERNATIVE OF LVT VIA HVT DRIVERS

Clock-tree top present discount is performed with the aid of deteriorating tree uniformity in an attempt to unfold the switching time at a stage, accordingly averting aligned switching. The optimization algorithm is replacing LVT by way of HVT drivers. This has two benefits. To begin with, because of its longerTpd , the coherency of the switching time at a stage shall be disrupted. Secondly, a byproduct is the reduction of leakage present. Though it does no longer affect the vigour noise, it has the advantage of whole vigour and energy reduction. A hazardous difficulty is instantly bobbing up. Isn’t that such replacements outcomes in a diverse of propagation delays alongside root-to-leaf paths, which finally may just take clock skew out of prescribed value? As easy drivertransformation which avoids this problem is thereforedescribed.Don't forget a clock-tree at the beginning designed as

shown in Fig. Three, comprising LVT drivers, which is the long-established design



practice. Fig. Four indicates the result of a SPICE simulation of a step input response received for the illustrated drivers.The golf green curve is the response of an HVT driver and the red curve is the response of two cascaded LVT drivers of 1/2 dimension of the fashioned LVT. We denote the latter by using LVT/2. Expectedly, upward push time of the latter is turbo. Nevertheless the 50% to 50% extend difference between the two configurations is three.6 picoseconds, which is not up to zero.5% of 1GHz clock frequency. Equal habits was once determined in simulations for the whole driver telephone library in forty manometers technology. The simulation below suggests the impact on peak present resulted by HVT and LVT/2 driver replacements. Fig. is the present waveform happened by means of traditional (default) 2 LVT drivers. The green waveform in Fig. is obtained for HVT even as the purple one results from cascaded LVT/2. Their superposition is proven in Fig . Comparing Fig. with Fig , the present height was decreased by means of 43%.

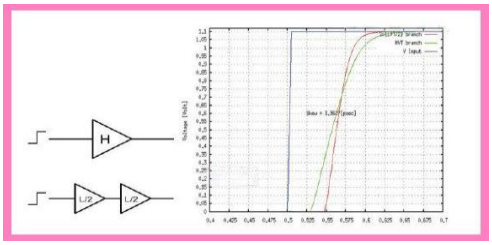


Fig: Step response for two driver configurations

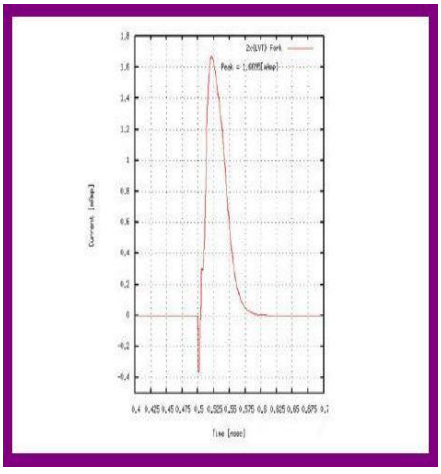


Fig: The peak current behavior of two LVT buffers

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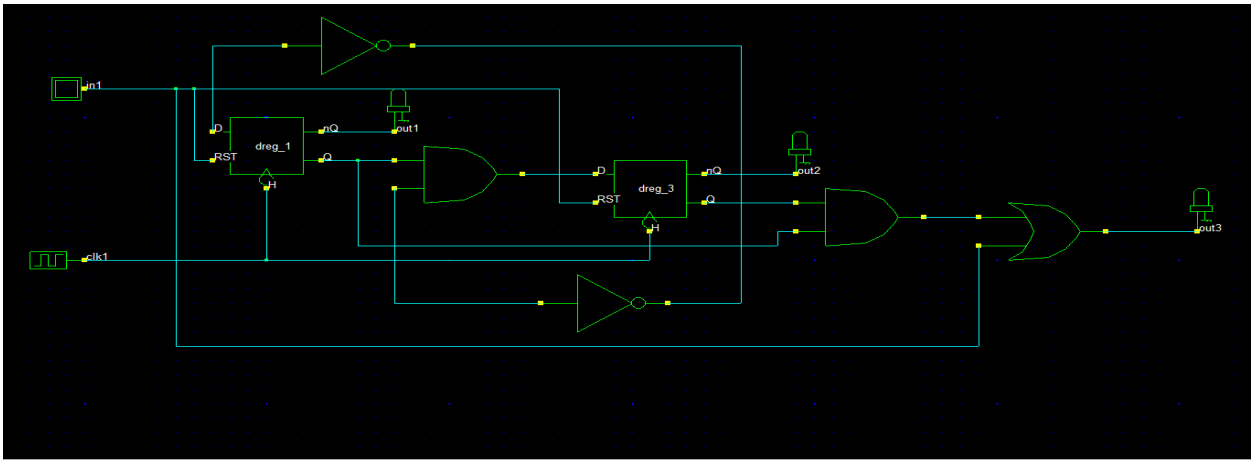
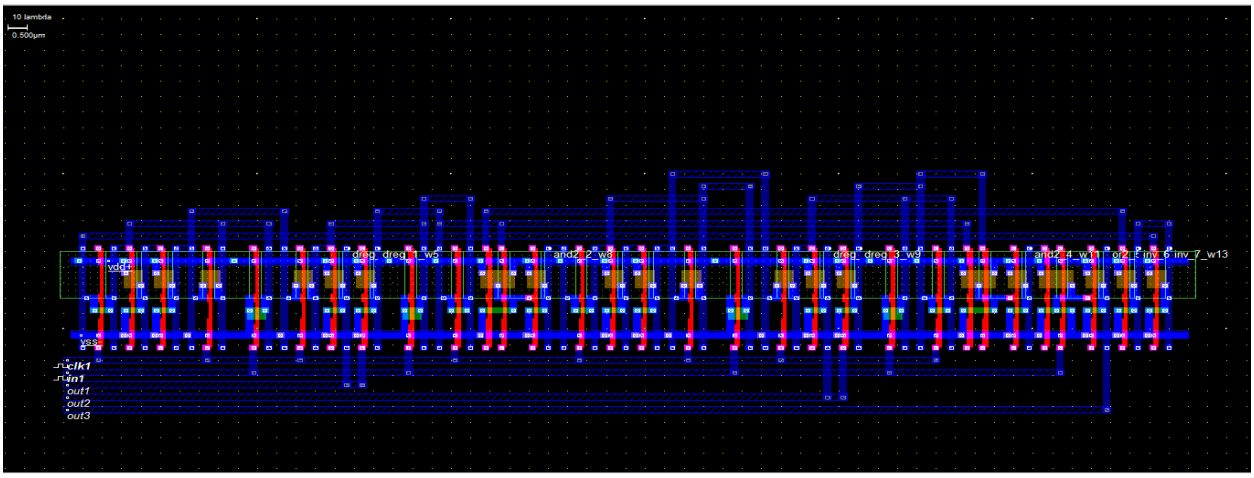
SIMULATION RESULT

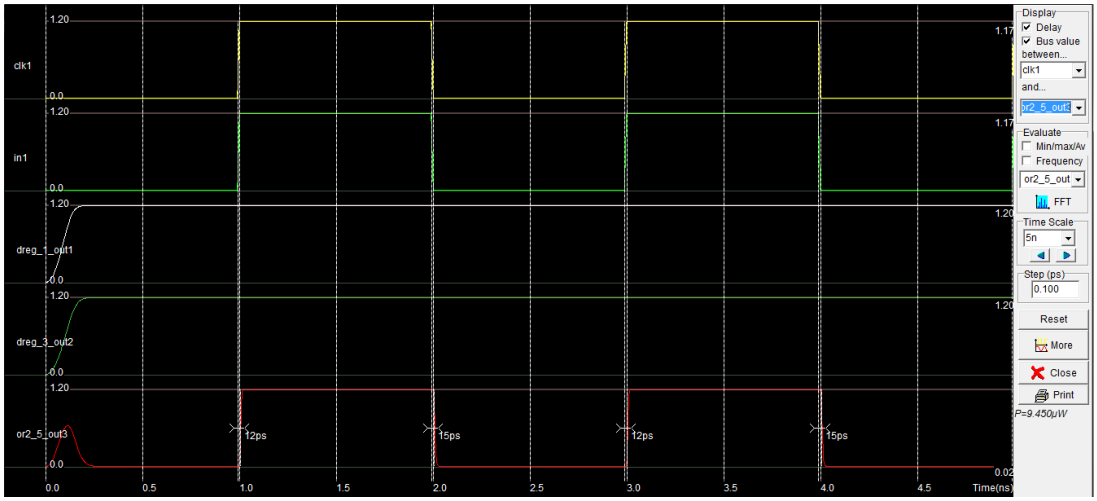
CIRCUIT DESIGNING:



LAY OUT:



SIMULATION RESULT:



CONCLUSION:

As it was noticed before clock tree is one of the major contributors of peak current in a SoC, that circumstance cannot be neglected and should be treated. Here we introduced one of the possible solutions. In that paper we didn't consider the impact of the process variation and differentiation of temperature among the SoC.All these effects will harm and affect negatively on jitter and skew of the optimized clock tree

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