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Modelling of Symmetrical three Phase Multilevel Inverter with Reduced Number of Switches

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ABSTRACT

In his paper a three phase multilevel inverter with a less number of switching devices is proposed. Large electrical drives and utility application require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power rating but also improves the performance of the whole system in terms of harmonics. In this paper the proposed inverter can output more numbers of voltage levels with reduced number of switches as compared to cascade H-bridge inverter, which results in reduction of installation cost and have simplicity of control system. Finally, the simulation results validate the concept of this new topology

Keywords: Multilevel Inverter, SPWM

I.INTRODUCTION

Recently, multi-level inverters great attention as a single stage inverter. Although, they have obtained need high number of components, but due to their advantages such as generating output voltage with extremely low distortion factor , low dv/dt, small output filter size, low electromagnetic interface , and low total harmonic distortion , still have great attention. Practically, all of these advantages appear strongly as the number of dc-power sources increased as in the case of renewable energy systems.

The general concept of is to utilize isolated dc sources or a bank of series capacitors to produce ac voltage waveforms with higher amplitude and near sinusoidal waveform. There are three conventional types of named as neutral point diode clamped, flying capacitor, and cascaded H-Bridge. Almost all of them are suffering from increased components number per level, and complex control architecture. Among the different topologies for, they can be classified into two main categories: 1) single dc-source inverter such as, and inverters; 2) multi-dc sources inverters such as inverter. While, multi-dc sources inverter is divided into symmetrical and no symmetrical topologies. principally, no symmetrical topologies produce more voltage levels compared to symmetrical topologies. Almost all of these topologies can be extended for more voltage levels by increasing the number of the primary configuration (basic cell).

Many topologies were presented in the last decade focusing on minimizing the basic multilevel topologies drawbacks. The author in presented a topology named multilevel dc link. It consists of a group of basic cells connected in series configuration. Each cell produces or 0 voltage across the connected cells, there is an H-bridge to change the polarity of the synthesized voltage. The required number of active switches for output voltage levels is for the inverters. However, this topology requires increased number of components compared to the conventional topologies, and high voltage stresses. However, in the authors presented a topology named transistor-clamped H-bridge . The primary cell can produce five-levels per pole in the output voltage. However, it suffers also from the increased components counts, requirements of electrolytic capacitors, complex control methodology

II.PROPOSED MODULAR MLI

A new modular three-phase with reduced components count is proposed and studied in this paper. The suggested three phase symmetrical inverter is shown in Fig. 2(a) . Each arm consists of series connection of basic cells with a series connected switch, for example arm A is consists of one cell connected in series with switch. Adding the common dc voltage source in to each arm forms the pole, creating the pole voltages. In order to obtain the zero state pole voltage another switch is added to the pole, similarly and for pole and. Fig. 1(b) shows the primary basic cell, where each cell consists of two switches and single dc voltage source. The two switches operate in a complementary fashion. Therefore, each cell can

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produce two voltage levels : when in ON-STATE, zero voltage is produced across the cell terminals, and when in ON-STATE, volt is applied across the cell terminals. Furthermore, using only one cell per each pole and applying suitable control signals to the, and, three voltage levels per pole (i.e., ,) are produced. The output pole voltage for cells connected in series configuration is shown in Fig. 1(c).

. The proposed topology is a modular type therefore it can be extended to any levels. Equations (1)–(4) provide the relations of the proposed topology as

$$N\_Pole = N\_Cell + 2 \quad (1)$$

$$M_{Level} = 2N_{Cell} + 3 \quad (2)$$

$$N_{SW} == 3(2N_{Cell} + 2) \quad (3)$$

$$N_{PS} + 1 = 3N_{Cell} \quad (4)$$

Then for the example of, [based on (2)] which is the pole voltage levels and [based on (3)] which is the output line-to-line voltage levels. Note that the number of output phase voltage levels will be derived to be seven levels in low frequency modulation and nine levels for high frequency modulation.

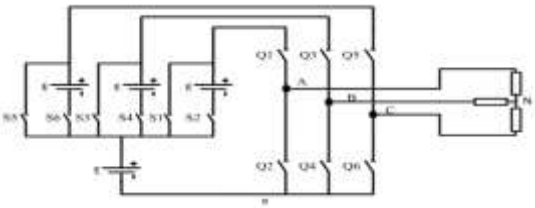

Fig 1(a). Proposed three-phase MLI topology.

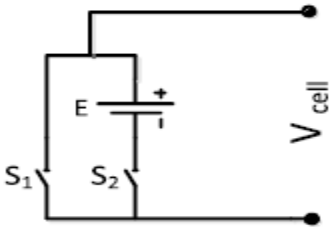

Fig 1(b) Basic cell.

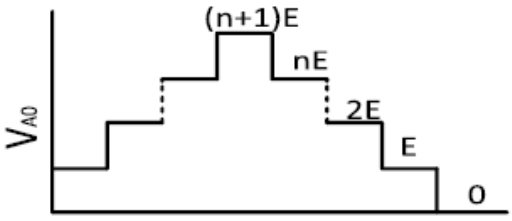

Fig 1(c)Pole voltage waveform for n-cell

I11.MODULATION TECHNIQUES FOR THE PROPOSED MLI

A. Low Frequency Modulation Technique

The low frequency modulation is considered as the basic modulation technique due to its lower switching frequency than the other modulation methods. It causes the switching loses reduced dramatically [33]. In order to investigate the performance of the proposed, three levels per pole by using single basic cell in each pole is used as shown in Fig. 2. It is simulated via PSIM and MATLAB/SIMULINK software packages. In order to generate the required switching signals for the proposed , a rectified sine waveform has a frequency equals to the output voltage frequency (50 Hz) is compared with a dc voltage signal has an amplitude equal to half of the sine wave amplitude as shown in Fig. 3. The intersection points between them identify six periods (to). Four switching signals are constructed from these periods combination in order to generate a sinusoidal output voltage. The control equations for the (S_1, S_2,S_3 andS_4) are given in(6)–(9), respectively. The same scenario is applied to inverter poles and after shifting the basic sinusoidal voltage with -120^0, 120^0, respectively.

Therefore, the required switching signals for the overall three poles can be generated

$$S_1 = P_1 + P_4 \quad (6)$$

$$S_2 = P_2 + P_3 \quad (7)$$

$$Q_1 = P_1 + P_2 + P_3 + P_4 \quad (8)$$

$$Q_2 = P_5 + P_6 \quad (9)$$

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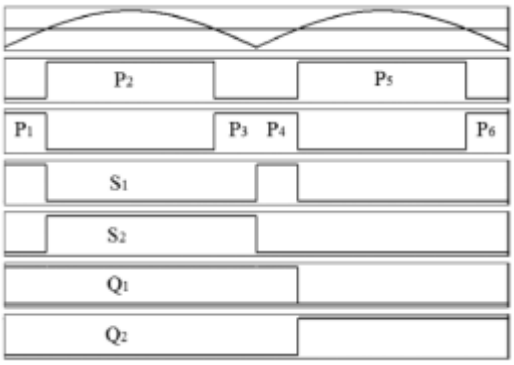

. Fig 2 Switching patterns for low frequency modulation technique.

B. Sinusoidal Pulse-Width Modulation Technique (SPWM):

The straight way to generate the *SPWM* signals is to compare a sinusoidal waveform signal with a triangular waveform. The comparison operation will produce the Boolean signals that are required to synthesize the switches control pulses. The *SPWM* technique is successfully applied for the proposed topology. Two different approaches have been proposed as follows.

1) Scheme I: *SPWM Using Single Carrier Signal:* This scheme uses one carrier signal centered with the sinusoidal modulation signal (sine waveform), and it has an amplitude equal to peak-to-peak value of the modulation signals as shown in Fig. 4. It worth mentioning that the modulation signal is shifted by dc level equals to (CR/2), where CR is the carrier signal amplitude. The resulted Boolean output from the comparison between the carrier and the modulating signal produces the main pulse signal G_1. Also the pulse signal GP_1 is generated by comparing the modulating signal with zero value. After logical processing on $G_1$and GP_1, the switching pulses S_1, S_2,Q_1, and Q_2 can be generated as specified in (10)–(13).

$$S_1 = (G_1 \; X \; \overline{GP_1}) + (\overline{G_1} \; X \; GP_1) \quad (10)$$

$$S_2 = (G_1 \; X \; GP_1) \quad (11)$$

$$Q_1 = GP_1 + \{(G_1 \; X \; \overline{GP_1}) + (\overline{G_1} \; X \; GP_1)\} \quad (12)$$

$$Q_2 = \overline{\{\overline{GP_1} \; X \; \overline{(G_1 \; X \; \overline{GP_1})}\}} \quad (13)$$

Where stands for logic AND, stands for logic OR stands for invert, and are the signals which will Be applied to the gates drive belongs to switches respectively. In order to avoid dc-power sources short circuit operate in a complementary mode with dead time.

2) Scheme II: *SPWM Using Two Carrier Signals:* This scheme compares single modulating signal with two identical and shifted in level carrier signals. Both of them have amplitude equal the modulating signal peak. In addition, the carrier signals are shifted by a dc offset equals to the carrier signal amplitude as shown in Fig. 5. Using the same procedure followed

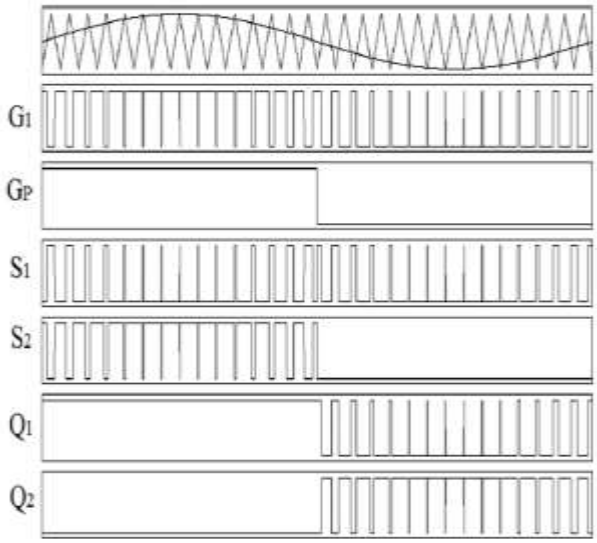

Fig. 3 . Switching patterns of the proposed MLI for scheme I.

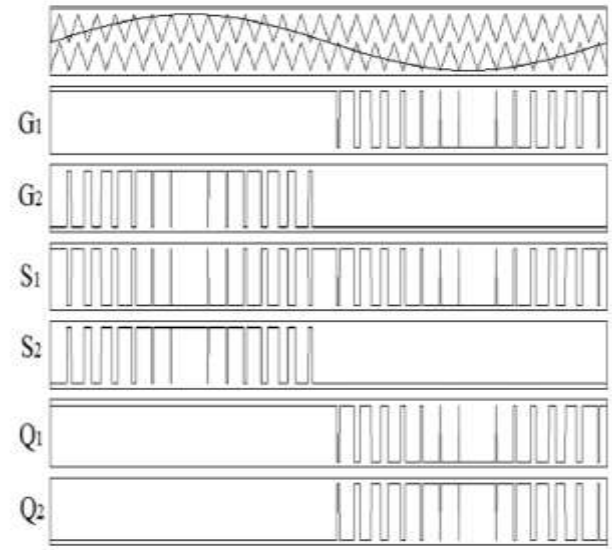

Fig. 4. Switching patterns of the proposed MLI for scheme II.

in scheme I, scheme II can be executed. However, due to using two carrier signals, there are two Boolean signals named and resulted from the comparison. By Carrying out several logical operations on these two signals as given in (14)–(17), the required control pulses for can be obtained

$$S_1 = (G_1 \; X \; \overline{G_2}) \quad (14)$$

$$S_2 = G_2 \quad (15)$$

$$Q_1 = \overline{G_2}\ X\ \overline{(G_1\ X\ \overline{G_2})} \quad (16)$$

$$Q_2 = \overline{G_2}\ X\ \overline{(G_1\ X\ \overline{G_2})} \quad (17)$$

V.SIMULATION RESULTS

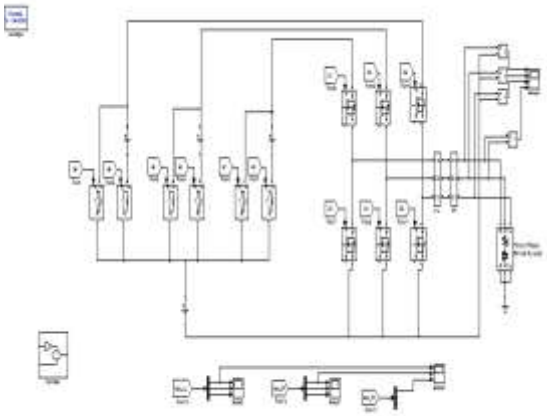

Fig 5 SIMULINK MODEL Of proposed system

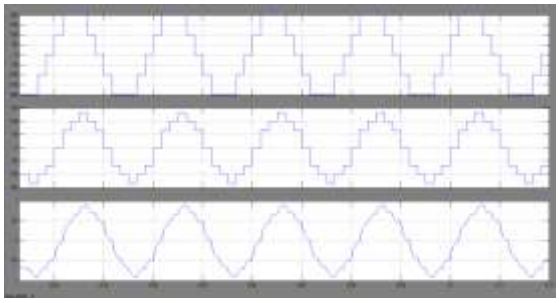

Fig 6 line to line, phase voltages and phase current with low frequency modulation

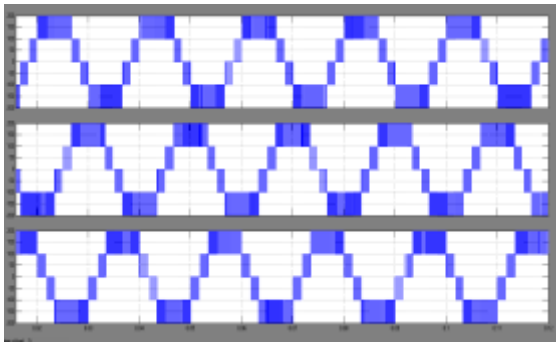

Fig 7line to line voltages with SPWM modulation technique

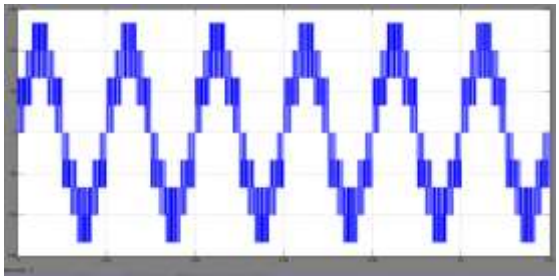

Fig 8 phase voltages with SPWM modulation technique

VI.CONCLUSION

A novel three phase multilevel inverter topology has been proposed in this paper. The most important feature of the system is being convenient for expanding and increasing the number of output levels simply with less number of switches. This method results in the reduction of the number of switches, losses, cost and also place. With present switching algorithm, the multilevel inverter generates nearly sinusoidal output voltage with very low harmonic content.

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BIOGRAPHY

Ms.B.TEJASVI, working as Teaching Assistant in JNTU Anantapuramu. And She received M.Tech in M.TECH (power electronics) in pullareddy engineering college kurnool A.P. She has 5 years' experience in teaching for Engineering students at UG and PG level and area of research: multi-level inverters and renewable energy sources