Design of Modified 64-Bit Parallel Prefix Technique B-K Adder

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ABSTRACT:

A parallel-prefix adder provides us the most excellentpresentation in VLSI design.On the other hand, presentation of Brent-kung adder all the way throughblack cell takes large area. So, gray cell can be replaced instead of black cell which gives the Efficiency inBrent-kungAdder. The projected system hastwo stages of actions they are pre-processing stage and generation stage. The pre-processing stage having propagated and generate. Generation stage spotlights on generation of carry and final result. In ripple carry adder (RCA) each bit having operation of addition is waited for the preceding bit operation of addition. In efficient Brent -Kungadder, addition operation does not wait for preceding bit operation of addition and modification is done at gate level toimprove the speed and decreases the area.

INDEX TERMS: Ripple carry adder; Efficient Brent–Kung adder; Black cell; Gray cell

I INTRODUCTION

Ripple carry adder is used for the addition task i.e., if N-bits addition process is presented by the full adder with N- bits. In ripple carry adder every full adder operation consists of sum and carry, and that carry will be given to next bit full adder operation.That processes is constant till the bit of Nth operation. The N-1th bit full adder operation carry will be given to the Nth bit full adder operation present in the ripple carry adder.[1]

Addition procedure is the majorprocess in the digital signal processing and control systems. The high-speed and accurateness of a processor or system depends on the performance of the adder. Multiplexer is the circuit combinational which consists of Inputs of multiple and a single output. In general processors of purpose and processors of DSP the addition operation addresses are taken from simple ripple carry adder.

The ripple carry adder of 3-bit is shown in Fig.1. The primary bit carry is given to second full adder of bit and similarly the second bit carry is known to the third bit full adder. The addition process is performed from least considerable bit to most considerable bit in ripple carry adder[1]. Configuration logic and routing resources in FieldProgrammable Gate Array.

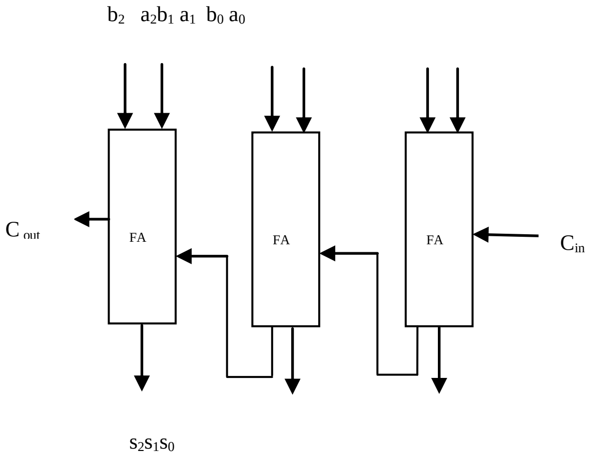


Fig.1: Three Bit Ripple Carry Adder

II BRENT-KUNG ADDER

BrentKung adder is used for high presentation addition operation. The Brent-kung is the adder of parallel prefix used to perform the operation of addition [3]. It is looking like tree structure to perform the arithmetic operation. The Brent-kung adder consists of grey cells and black cells. [2] Each black cell consists of one OR gate and two AND gates [4]. Each gray cell consists of only one AND gate.p_i denotes propagate and it consists of only one AND gate[5] given in equation 1. g_i denotes generate and it consists of one AND gate and OR gate given in equation 2. [6]

$$p_i= A_i \text{ XOR } B_i \text{ -------------- } (1)$$

$$g_i= A_i \text{ AND } B_i \text{ -------------- } (2)$$

G_i denotes carry generate and it consists of one AND gate and OR gate given in equation 3 used for first black cell. [8]

$$G_i=p_i \text{ OR } [g_i \text{ AND } c_{in}] \text{ --- } (3)$$

IIIPROPOSED BRENTKUNG ADDER

The proposed Brent-kung adder is flexible to speed up the binary addition and the arrangementlooks like tree structure for the high performance of arithmetic operations.

Field programmable gate arrays [FPGA's] are mostly used in recent years since they improve the speed of microprocessor based applications like mobile communication, DSP and telecommunication. Research on operation of binary fundamentals and motivation gives device development. The construction of efficientBrent-kung adder consists oftwo stages. They are pre-processing stage and generation stage.

Pre-Processing Stage:

In the pre-processing stage, generate and propagate are from each pair of the inputs. The propagate gives "XOR" operation of input bits and generates gives "AND" operation of input bits [7]. The propagate (P_i) and generate (G_i) are shown in below equations 4 & 5.

$$P_i=A_i \text{ XOR } B_i \text{ ------ } (4)$$

$$G_i=A_i \text{ AND } B_i \text{ ------ } (5)$$

Generation Stage:

In this stage, carry is generated for every bit is called carry generate (C_g) and carry is propagate for each bit is called carry generate (C_p). The carry propagate and carry generate is generated for the further operation, final cell present in the each bit operate gives carry. The preceding bit carry will help to sum of the next bit simultaneously till the last bit. The carry generate and carry propagate are given in below equations 6 & 7.

$$C_p=P_1 \text{ AND } P_0 \text{ ---------------- } (6)$$

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ } (7)$$

The above carry propagate C_p and carry generation C_g in equations 6&7 is black cell and the below shown carry generation in equation 8 is cell i.e., gray cell. The carry propagate is generated for the further operation. The final cell current in the each bit operation gives carry. The last bit carry will lead tosome of the next bit concurrently till the last bit. This carry is used for the next bit sum operate, the carry generate isgiven in below equations 8.

$$C_g=G_1 \text{ OR } (P_1 \text{ AND } G_0) \text{ ------ } (8)$$

The carry of a first bit is XORed with the after that bit of propagates then the output is given as sum and it is shown in equation 9.

$$S_i=P_i \text{ XOR } C_{i-1} \text{ ------- } (9)$$

It is used for two thirty-two bit addition operations and each bit undergoes pre-processing stage and generation stage then gives the final sum.

The primary input bits goes under pre-processing stage and they will produce propagate and generate. These propagates and generates undergoes generation stage produces carry generates and carry propagates then gives final sum. The step by step process of well-organizedBrent-kung adderis shown in Fig.2.

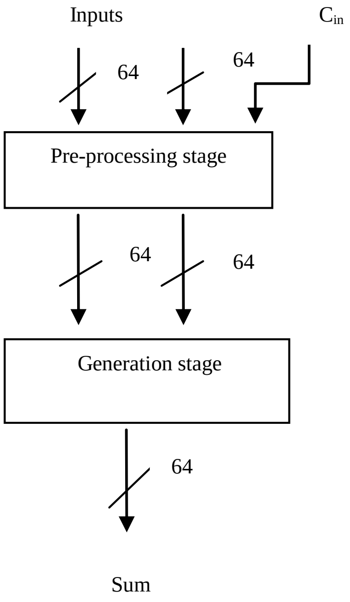


Fig.2: Block Diagram

The efficient Brent-kungadder arrangement is looking like tree structure for the high performance of arithmetic operations and it is the high speed adder which focuses on gate level logic. It designs with a reduction of number of gates. So, it diminishes the hindrance and memory used in this architecture.

The efficient Brent-kung adder is shown in fig.3 which improves the speed and decrease the area to the operation of 16-bit addition. The input bits A_i and B_i concentrates on generate and propagate by XOR and AND operations respectively. The propagates and generates undergoes the operations of black cell and gray cell and gives the carry C_i. That carry is XORed with the propagate of next bit, that gives sum.

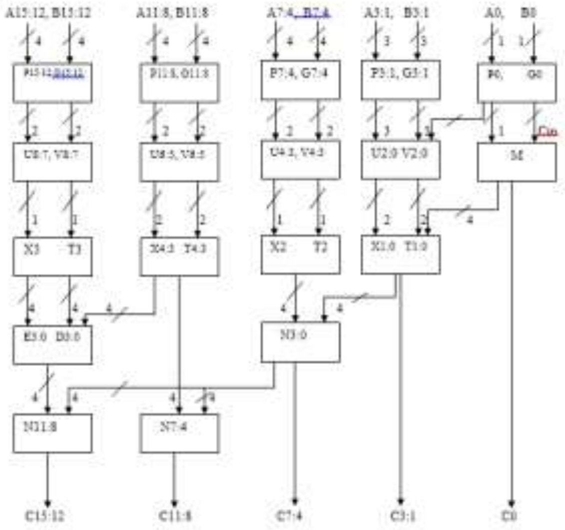


Fig.3: 16-Bit Efficient Brent-kung Adder

The properties of the operations are evaluated in parallel with accept the trees to overlap which leads to parallelization. The architecture ofEfficient Brent-kung adder gives the less memory and less delay for the operation of 16-bit addition.

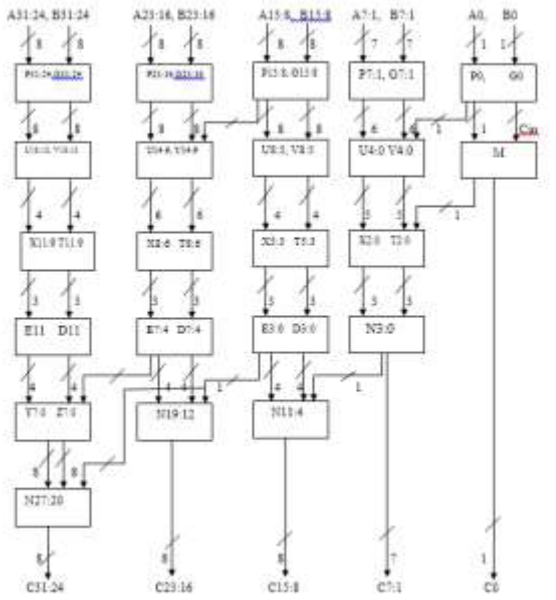


Fig.4: 64-bit Efficient Brent-kung Adder

The structural design of 64-bit Efficient Brent-kung adder is shown in Fig.4. The logical circuit is using multiple adders to find the ans i.e., sum of N-bit numbers. Everyoperation of addition has a carry input (C_{in}) which is the earlier bit carry output (C_{out}).

Study on binary addition innovatively motivates gives progress of devices. A lot of parallel prefix networks explain the literature of parallel addition operation.The parallel prefix adders are Brent-kung, Kogge-stone, Brent-kung, Sklansky, etc,. The fast and precisepresentation of an adder gives toused in the very large scale integrated circuits design and digital signal processors.

IV SIMULATION RESULTS

The well-organizedBrent-kung adder is design with an VHDL (very high speed integration hardware description language). Xilinx project navigator 14.1 is used andSimulation results of 16-bit efficient Brent-kungare shown in Fig.5.

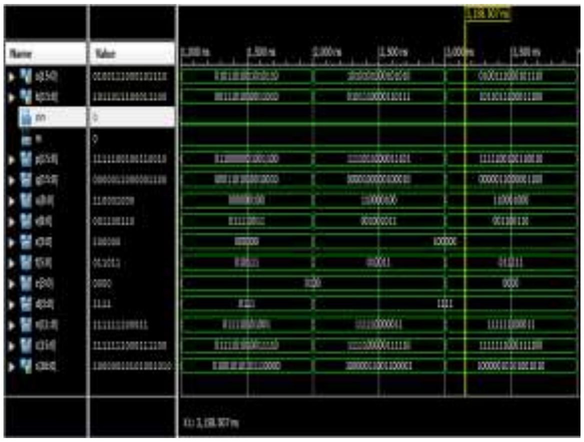


Fig.5: 16-Bit Efficient Brent-kung Adder Simulation Waveform

The structural design of 64-bit Efficient Brent-kung adder is shown in Fig.4 and the Simulation results is shown in Fig.6.

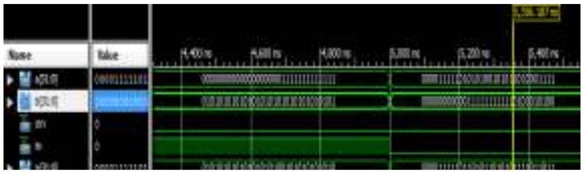
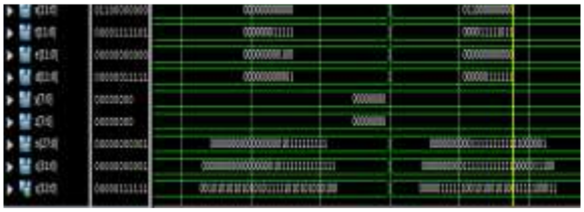


Fig.6: 64-Bit Efficient Brent-kung Adder Simulation Waveform



The design of adders is done on VHDL. The memory and delay performance Efficient Brent-kungadder (EBK) is shown in Table.1

Adder	Delay(ns)	Memory used(MB)
8-bit Efficient Brent-kung adder	11.2	181
16-bit Efficient Brent-kung adder	12.2	184
64-bit Efficient Brent-kung adder	13.275	208.9

Table.1: Delay and memory used in EBK

V CONCLUSION

In this paper, new approaches to design an efficient Brent-kung adder look like tree structure and cells in the carry generation stage are decreased to pace up the binary addition. It concentrates on gate levels to perk upthe speed and decreases the memory used.The proposed adder addition operation offers elude great advantage in reducing delay.

REFERENCES

[1] A. Omondi and B. Premkumar, Residue Number Systems: Theory andImplementations. London, U.K.: Imperial College Press, 2007.

[2] B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs,2nd ed., New York, NY, USA: Oxford Univ. Press, 2010.

[3] J. Chen and J. Hu, “Energy-efficient digital signal processing via voltageoverscaling-based residue number system,” IEEE Trans. Very LargeScale Integr. (VLSI) Syst., vol. 21, no. 7, pp. 1322–1332, Jul. 2013.

[4] C. H. Vun, A. B. Premkumar, and W. Zhang, “A new RNS based DAapproach for inner product computation,” IEEE Trans. Circuits Syst. I,Reg. Papers, vol. 60, no. 8, pp. 2139–2152, Aug. 2013.

[5] S. Antão and L. Sousa, “The CRNS framework and its application toprogrammable and reconfigurable cryptography,” ACM Trans. Archit. Code Optim., vol. 9, no. 4, p. 33, Jan. 2013.

[6] A. S. Molahosseini, S. Sorouri, and A. A. E. Zarandi, “Researchchallenges in next-generation residue number system architectures,” inProc. IEEE Int. Conf. Comput. Sci. Educ., Jul. 2012, pp. 1658–1661.

[7] K. Navi, A. S. Molahosseini, and M. Esmaeildoust, “How to teachresidue number system to computer scientists and engineers,” IEEETrans. Educ., vol. 54, no. 1, pp. 156–163, Feb. 2011.

[8] Y. Wang, X. Song, M. Aboulhamid, and H. Shen, “Adder based residueto binary numbers converters for (2n − 1, 2n, 2n + 1),” IEEE Trans.Signal Process., vol. 50, no. 7, pp. 1772–1779, Jul. 2002.

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