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# Bridgeless PFC Converter for SMPS & BLDC Drive Applications

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**Abstract** – *The devices generally used in industrial, commercial and residential applications need to undergo rectification for their proper functioning and operation. Hence there is a need to reduce the line current harmonics so as to improve the power factor of the system. This has led to designing of Power Factor Correction circuits. This concept presents a power factor corrected (PFC) bridgeless (BL) buck–boost converter-fed SMPS. The brushless DC (BLDC) motor is becoming increasingly popular in sectors such as automotive (particularly electric vehicles (EV)), HVAC, white goods and industrial because it does away with the mechanical commutator used in traditional motors, replacing it with an electronic device that improves the reliability and durability of the unit. Because a BLDC motor dispenses with the brushes – instead employing an "electronic commutator" – the motor's reliability and efficiency is improved by eliminating this source of wear and power loss. In addition, BLDC motors boast a number of other advantages over brush DC motors and induction motors, including better speed versus torque characteristics; faster dynamic response; noiseless operation; and higher speed ranges. This paper deals with the design, analysis, simulation, and development of a power-factor-correction (PFC) multiple output switched-mode power supply (SMPS) using a bridgeless buck–boost converter at the front end. Single-phase ac supply is fed to a pair of back-to-back-connected buck–boost converters to eliminate the diode bridge rectifier, which results in reduction of conduction losses and power quality improvement at the front end. The performance of the proposed multiple-output SMPS is evaluated under varying input voltages and loads by simulating this circuit in MATLAB/Simulink environment.*

***Index Terms***—Bridgeless buck–boost converter, discontinuous conduction mode (DCM), multipleoutput switched-mode power supply (SMPS), power factor (PF) correction (PFC), BLDC Motor.

## I. INTRODUCTION

Efficiency and cost would be the major concerns in the development of low-power motor drives targeting household applications such as for example fans, water pumps, blowers, mixers, etc. The utilization of the brushless direct current (BLDC) motor in these applications is becoming very common due to options that come with high efficiency, high flux density per unit volume, low maintenance requirements, and low electromagnetic-interference problems [1]. These BLDC motors are not limited to household applications, but they're ideal for other applications such as for example medical equipment,transportation, HVAC, motion control, and many industrial tools.

A BLDC motor has three phase windings on the stator and permanent magnets on the rotor. The BLDC motor can be referred to as an electronically commutated motor because an electronic commutation based on rotor position can be used rather than mechanical commutation which includes disadvantages like sparking and wear and tear of brushes and commutator assembly [2-4].

The use of non-isolated PFC converters at the front end of these power supplies is a commonly accepted solution to achieve a good power quality at varying input voltages and loads [5]. Discontinuous

conduction mode (DCM) operation of these converters results in inherent PFC and reduction in sensor requirements. Furthermore, DCM can also be implemented with simple control strategy. Recent advancements in the field of power electronics have enabled the elimination of DBR at the front end of the power supplies, thereby improving the power quality at the ac mains. Various bridgeless singleended primary-inductance converter and Cuk converters are proposed in the literature, which result in low voltage stress, improved thermal management, and low conduction losses [6]–[9]. However, the component count is increased in these converters, which is not suitable for low-power SMPS applications, although the output voltage range is fairly large. A bridgeless buck PFC converter is proposed in [10], which acts as a voltagedoubler. A bridgeless boost converter is reported, which eliminates one diode drop in the current path.

Due to these issues, improved-power-quality SMPSs are extensively being researched, which are expected to draw a sinusoidal input current at a high PF. Improvement in power quality also results in better reliability and enhanced efficiency [11]. To achieve a perceivable improvement in power quality, PF correction (PFC) circuits are employed in these SMPSs at the utility interface point. Active power factor correction refers to the method of increasing PF by using active electronic circuits with feedback that control the shape of the drawn current. High-frequency switching techniques have been used to shape the input current waveform successfully [12].

Multiple output DC-DC converters are desirable for a variety of applications to reduce the number of power supplies, complexity, space and cost than a large number of single output converters. Now a days, a DC-DC converter consisting of two stages is becoming popular as the use of first stage eliminates the second harmonic voltage effect that is reflected at the output because of single phase AC mains input. The first stage converter can be a non-isolated DC-DC converter and the second stage should be an isolated DC-DC converter having multiple outputs. To reduce the complexity, cost and space, only a single output (the most sensitive one) is sensed and regulated by feedback control. Generally, in the front end, a diode bridge is used to convert AC mains voltage to unregulated DC voltage which results in poor power factor (PF). To compensate for this, in the present work, a DC-DC converter is used with power factor correction (PFC) circuit to meet the IEEE and IEC standards [13-14].

## II. CONFIGURATION OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The system configuration of the proposed multiple-output SMPS is shown in Fig.1. Single-phase ac supply is fed to two buck–boost converters through an inductor–capacitor (Lin–Cin) filter to eliminate the high-frequency ripples. The upper buck–boost converter that conducts during the positive half cycle of the ac supply consists of one high-frequency switch Sp, inductor Lp, and two diodes Dp1 and Dp2. Similarly, the lower buck–boost converter that operates during the negative half cycle consists of one high-frequency switch Sn, inductor Ln, and two diodes Dn1 and Dn2. Both inductors Lp and Ln of buck–boost converters are designed in DCM to obtain inherent PFC at the input ac mains. The input capacitor of the halfbridge VSI acts as the filter at the output of the buck–boostconverter. The voltage and current stresses on the switches of the buck–boost converters are evaluated to estimate the switch rating and heat sink design. The output dc voltage of the buck–boost converter is regulated by using closed-loop control. The regulated dc output voltage of the buck–boost converter is fed to the half-bridge VSI for obtaining multiple dc voltages. The half-bridge VSI consists of two input capacitors C11 andC12, two high-frequency switches S1 and S2, and one multipleoutput high-frequency transformer (HFT). The HFT is having one primary winding and four secondary windings which are connected in center-tapped configuration to reduce the losses.

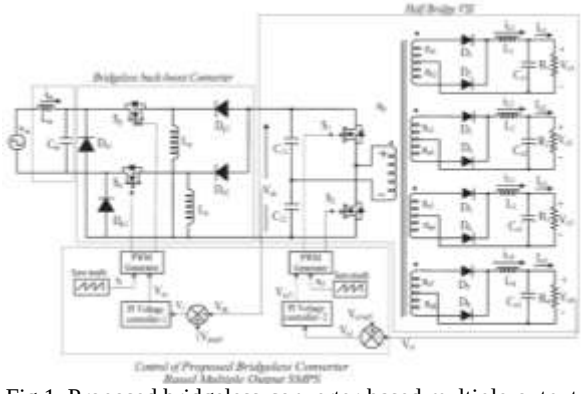

Fig.1. Proposed bridgeless-converter-based multiple-output SMPS.

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At the secondary side of the HFT, filter inductors L1, L2, L3,and L4 and capacitors Co1, Co2, Co3, and Co4 are connected to each winding to reduce the current and voltage ripples, respectively. The output voltages are regulated by using closedloop control of one of the output voltages. The highest rated dc voltage is sensed for this purpose. The other three outputs are controlled through duty ratio control of the half-bridge VSI because a common core is used for all other secondary windings of the HFT with proper winding arrangements. The effect of varying input voltages and loads is studied to reveal the improved performance of the proposed bridgeless-converter-based multiple-output SMPS. The hardware of the SMPS is implemented in a laboratory prototype to verify the simulated results.

## III. OPERATING PRINCIPLE OF BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The proposed bridgeless-converter-based multiple-output

SMPS consists of a single-phase ac supply feeding two back-to-back-connected buck–boost converters with a half-bridge VSI and multiple-output HFT at the load end. The buck–boost converters are controlled suitably to obtain a high PF and low input current THD. The half-bridge VSI at the output takes care of high-frequency isolation with multiple dc output voltages being regulated. The operation of both converters in one switching cycle is described in the following subsections.

### *A. Operation of Buck–Boost Converter*

The switches in the upper and lower buck–boost converters are switched on and off alternately in the positive and negative half cycles of the ac voltage, respectively. The operation of the upper buck–boost converter in DCM during the positive half cycle of the ac input voltage is shown in Fig. 3. The lower one operates in the same way but during the negative half cycle. Three states are observed in DCM operation in each switching cycle. In the first state, when the upper switch Spis on, inductor Lp starts storing energy from the input, and the inductor current increases to the maximum value, as shown in Fig. 2(a). Diode Dp1 completes the current flow path in the input side. In the second state, Sp is turned off, and the energy in inductor Lp is transferred to the output, thus reducing its current from maximum value to zero, as shown in Fig. 2(b). In the last state of one switching cycle, neither the switch and nor the diode conducts, and the inductor current remains zero, ensuring DCM operation [Fig. 2(c)]. Fig. 2(d) shows the waveforms for one complete pulse width modulation (PWM) switching cycle. In the next switching cycle, the same sequence of operationrepeats itself. Similarly for negative half cycle of the input voltage, the lower buck–boost converter operates, and the same sequence of operation continues.

### *B. Operation of Half-Bridge VSI*

The controlled output dc voltage of the dual buck–boost converter is fed to the half-bridge VSI for high-frequency isolation, for voltage scaling, and for obtaining multiple dc output voltages. The operation of the half-bridge VSI in one switching cycle is described in four states. The second and

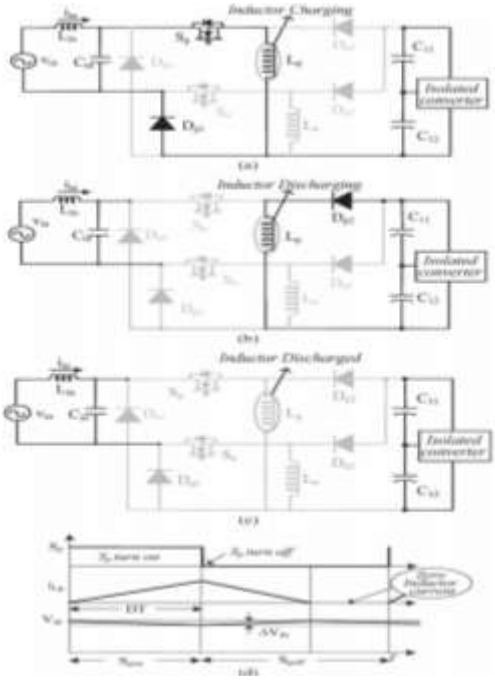

Fig.2. Operating modes for under (a) upper switch Sp is on, (b) upper switch Spis off, (c) both switch and diode are off, and (d) waveforms in one switching cycle.

fourth states are similar and occur twice in each switching cycle, as shown in Fig. 3(b). In the first state, the upper switch S1 is turned on; the input current circulates through the primary winding of the HFT to the lower input capacitor C12. Diodes D1, D3, D5, and D7 start conducting, and the inductors associated with the windings start storing energy, as shown in Fig. 3(a). Therefore, inductor currents iL1, iL2, iL3, and iL4 increase, and output filter capacitors Co1, Co2, Co3, and Co4 discharge

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through the loads. In the second state [Fig. 3(b)], both switches are turned off, and all secondary diodes D1–D8 freewheel the stored energy until the voltage across the HFT becomes zero. Therefore, inductor currents iL1, iL2, iL3, and iL4 start decreasing. In the third state of the switching cycle,

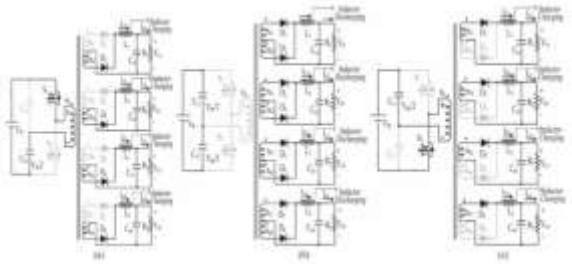

Fig.3. (a) When the first switch S1 is on, (b) when both switches are off, (c) and when the second switch S2 is on.

The second switch S2 is turned on, and the input current flows through upper capacitor C11 and the primary winding, as shown in Fig. 3(c). Associated diodes D2, D4, D6, and D8 in the secondary windings conduct, and inductors L1, L2, L3, and L4 start storing energy. When the energy stored in the inductors reaches maximum values, the switch is turned off. In the last state, all secondary diodes start conducting, which is similar to the second state. The same operating states repeat in each switching cycle.

## IV. CONTROL OF PROPOSED BRIDGELESS-CONVERTER-BASED MULTIPLE-OUTPUT SMPS

The control of the SMPS is carried out using two independent controllers. The front-end bridgeless buck–boost converter utilizes the voltage follower approach, while the half-bridge VSI utilizes the average current control.

### *A. Control of Front-End Converter*

The control of the PFC bridgeless converter generates the PWM pulses for both switches (Sp and Sn) according to the polarity of input ac mains voltage. In this technique, voltage error Ve, i.e., the difference between the reference voltage Vdcref and the sensed dc output voltage Vo1, is fed to a proportional–integral (PI) voltage controller, as shown in Fig. 1. The voltage error signal (Ve) is expressed as

$$V_e(n) = V_{\text{dcref}}(n) - V_{\text{dc}}(n)$$

Where n represents the nth sampling instant.

This error voltage signal (Ve) is fed to the voltage PI controller 1 to generate a controlled output voltage (Vcc). It is expressed as

$$V_{cc}(n) = V_{cc}(n-1) + k_p\{V_e(n) - V_e(n-1)\} + k_i V_e(n)$$

Where kp and ki are the proportional and integral gains of the voltage PI controller 1. Finally, the output of the voltage controller 1 is compared with a high-frequency saw tooth signal (St) to generate the PWM pulses

$$\text{For } v_{\text{in}} > 0; \quad \begin{cases} \text{if } s_t < V_{\text{cc}}, & \text{then } S_p = \text{on} \\ \text{if } s_t \geq V_{\text{cc}}, & \text{then } S_p = \text{off} \end{cases}$$

$$\text{For } v_{\text{in}} < 0; \quad \begin{cases} \text{if } s_t < V_{\text{cc}}, & \text{then } S_n = \text{on} \\ \text{if } s_t \geq V_{\text{cc}}, & \text{then } S_n = \text{off} \end{cases}$$

Where Sp and Sn represent the switching signals of PFC bridgeless buck–boost converter.

### *B. Control of Half-Bridge VSI*

For controlling the output voltage of the half-bridge VSI, an average current control scheme is used. The highest ratedwinding output voltage Vo1 is sensed and compared with a constant reference value Vo1ref. The voltage error signal (Ve1) is fed to PI controller 2, and its output is compared with the saw tooth signal to generate PWM switching signals to maintain the output voltage constant. Thus, the control is able to take care of the impact of any individual output on the overall variationin the duty ratio and also the contribution of the present loadcondition of any of the outputs to the variations in Vo1, Vo2, Vo3, and Vo4. If the load on any of the other windings is varied, the duty cycle undergoes a change according to the impact felt on the highest rated output, and hence, voltage regulation is taken care of. However, the response of the other windings is slightly slower as compared to the winding whose output is sensed. Switches S1 and S2 are switched on and off alternately in each half cycle of one PWM period with sufficient dead time to avoid shoot-through.

## V. PRINCIPLE OF BLDC MOTOR

BLDC engine comprises of the perpetual magnet rotor and an injury stator. The brushless engines are controlled utilizing a three stage inverter. The engine obliges a rotor position sensor for beginning and for giving legitimate compensation arrangement to turn on the force gadgets in the inverter extension. In light of the rotor position, the force gadgets are commutated consecutively every 60 degrees. The electronic compensation takes out the issues connected with the brush and the commutator plan, in particular starting and destroying of the commutator brush course of action, along these lines, making a BLDC engine more rough contrasted with a dc engine. Fig.4. demonstrates the stator of the BLDC engine and fig.5 shows rotor magnet plans.


Fig.4. BLDC motor stator construction

Fig.5. BLDC motor Rotor construction.

The brush less dc engine comprise of four fundamental parts Power converter, changeless magnet brushless DC Motor (BLDCM), sensors and control calculation. The force converter changes power from the source to the BLDCM which thus changes over electrical vitality to mechanical vitality. One of the remarkable highlights of the brush less dc engine is the rotor position sensors, in view of the rotor position and order signals which may be a torque charge, voltage summon, rate order etc; the control calculation s focus the entryway sign to every semiconductor in the force electronic converter.

The structure of the control calculations decides the sort of the brush less dc engine of which there are two principle classes voltage source based drives and current source based drives. Both voltage source and current source based commute utilized for perpetual magnet brushless DC machine. The back emfwaveform of the engine is demonstrated in the fig.5. Be that as it may, machine with a non-sinusoidal back emf brings about diminishment in the inverter size and lessens misfortunes for the same influence level.

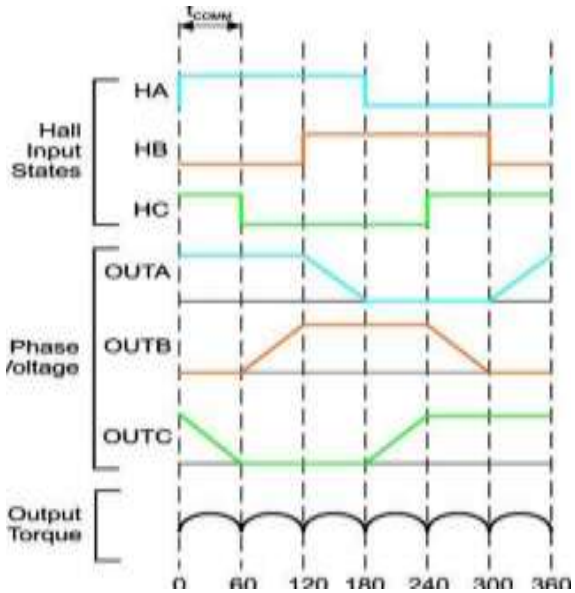


Fig.6.Hall signals & Stator voltages.

## VI.MATLAB/SIMULATION RESULTS

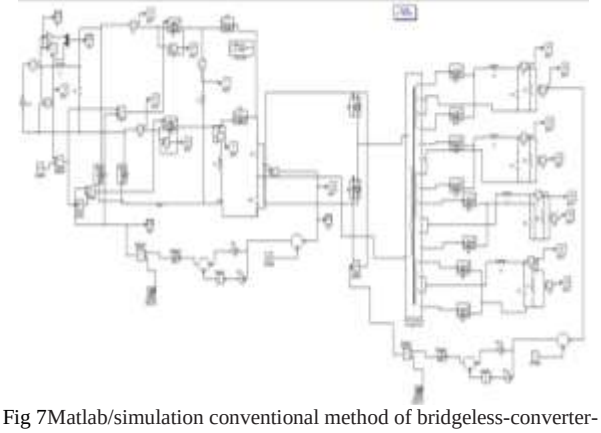

Fig 7Matlab/simulation conventional method of bridgeless-converter-based multiple-output SMPS.

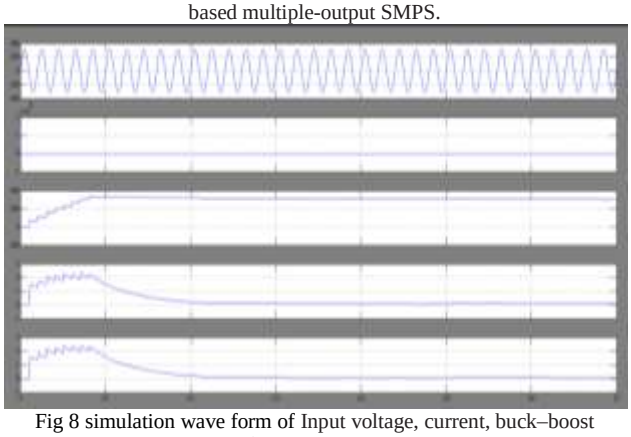

Fig 8 simulation wave form of Input voltage, current, buck–boost converter output voltage, half bridge VSI output voltages, and currents at 220 V and full load.

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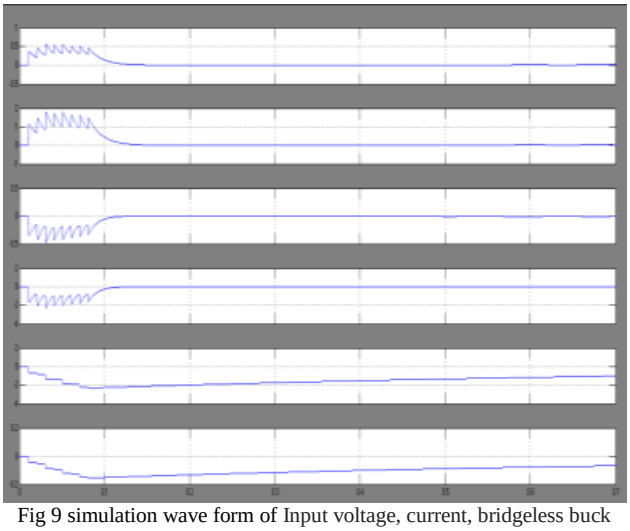

Fig 9 simulation wave form of Input voltage, current, bridgeless buck boost converter output voltage, half-bridge VSI output voltages, and currents at load variation in +12- and +5-V outputs at 0.25 s.

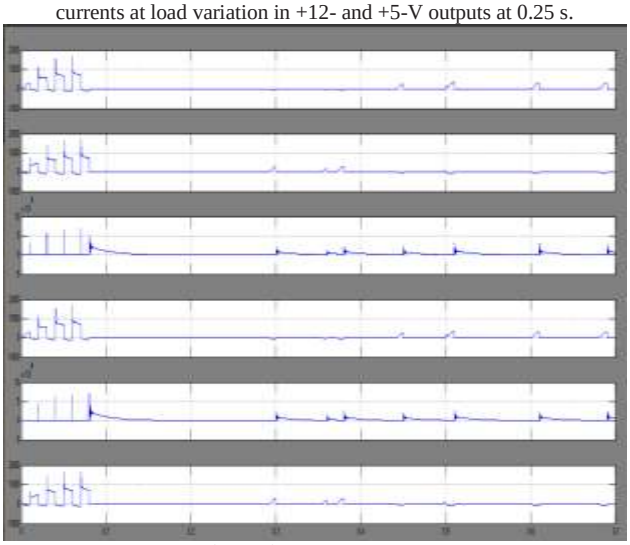

Fig 10 simulation waveform of input current and its harmonic spectrum at 220 V and full load.

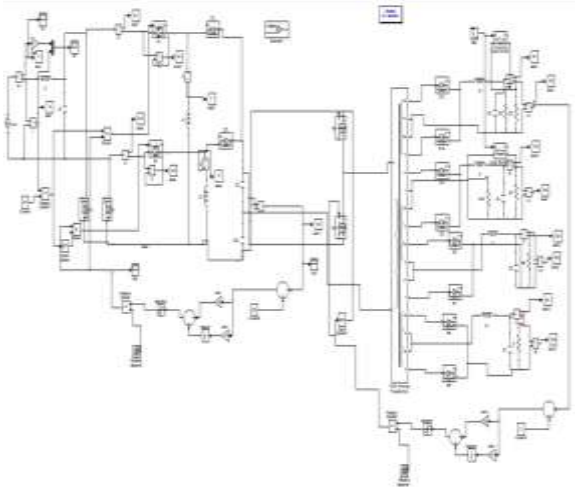

Fig 11Matlab/Simulation proposed method of bridgeless-converter-based multiple-output SMPS with variable load.

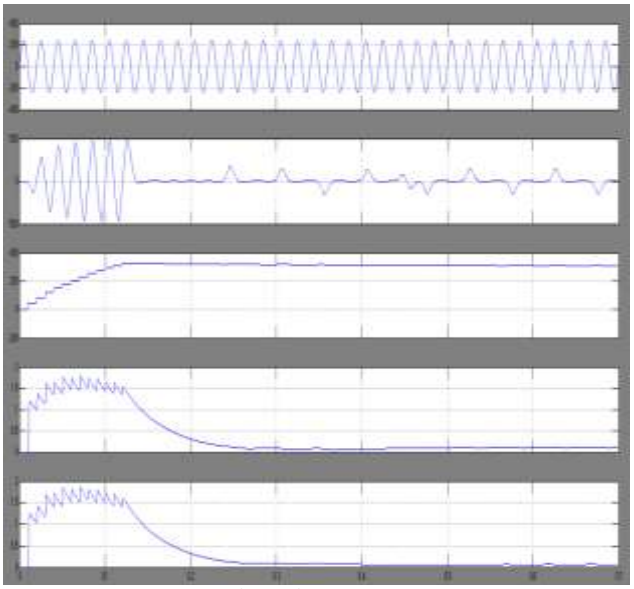

Fig 12.simulation wave form of Input voltage, current, buck–boost converter output voltage, half bridge VSI output voltages, and currents at 220 V and full load with variable load

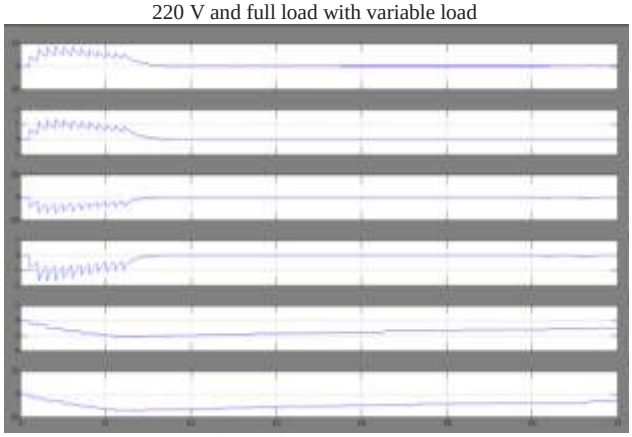

Fig.13.simulation wave form of Input voltage, current, bridgeless buck boost converter output voltage, half-bridge VSI output voltages, and currents at load variation in +12- and +5-V outputs at 0.25 s with variable load

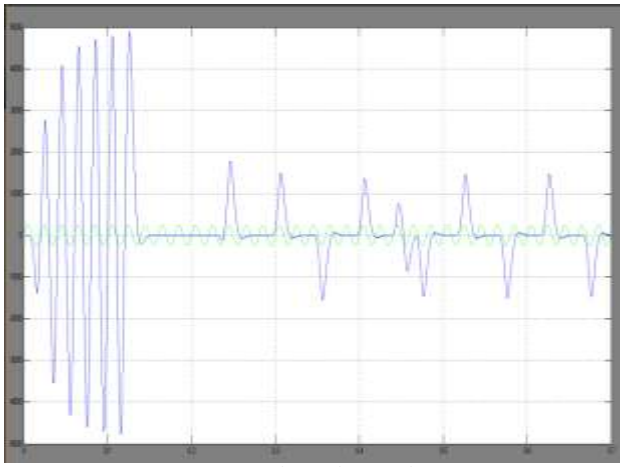

Fig.14.simulation wave form of power factor correction.

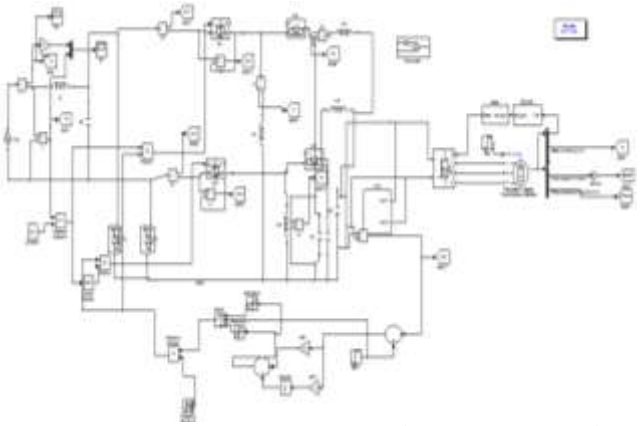

Fig.15.Matlab/Simulation proposed method of bridgeless-converter fed BLDC Motor Drive.

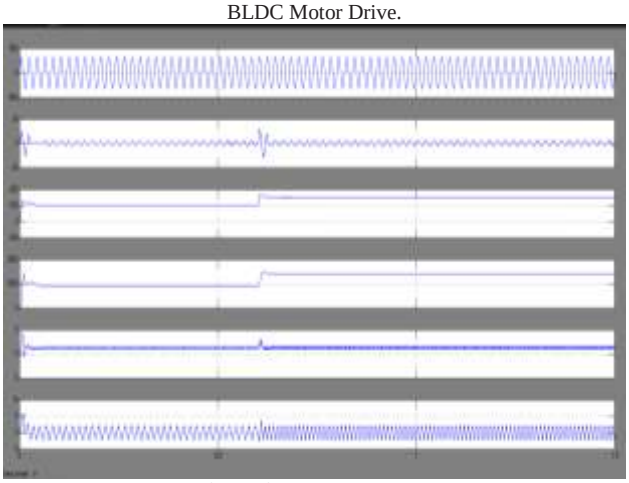

Fig.16.SimulationWaveform of the Source Voltage, Source Current, DC-Link Voltage, Speed, Torque and Armature Current.

## VII.CONCLUSIONS

A bridgeless-converter-based multiple-output SMPS has been designed, modeled, simulated, to demonstrate its capability to improve the power quality at the utility interface. The output dc voltage of the first-stage buck–boost converter has been maintained constant, independent of the changes in the input voltage and the load, and it is operated in DCM to achieve inherent PFC at the single-phase ac mains.The PMBLDCM speed has been identified to be proportional to the dc link voltage. Therefore, by controlling the dc link voltage, a smooth speed control has been achieved. The usage of the rate limiter in the reference dc link voltage has limited the motor current within the desired value at the time of transient conditions. In this proposed topology, a satisfactory performance for both speed control and supply voltage variation has been achieved. Moreover, the power quality indices are within the IEC 61000-3-2 limits. The proposed topology has achieved satisfactory performance which is useful for low power BLDC motor drive.

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