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A survey on PCM using Non-Binary Orthogonal Latin Square

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Abstract

This manuscript proposes non-binary orthogonal Latin square (OLS) codes that are amenable to a multilevel phase change memory (PCM). This is based on the property that the proposed (n symbols, k symbols) t-symbol error correcting code uses the same H matrix as an (n bits, k bits) binary t-bit error correcting OLS code. The new codes are shown to have a shorter check bit length and better probability in encoding/decoding than conventional binary OLS codes. Extensive results are provided for assessment and comparison. The proposed codes are also shown to be always better than the matrix codes, i.e. independently of the metric and the parameters employed in the comparison.

Keywords: Error correcting code (ECC), phase change memory (PCM), orthogonal Latin square (OLS) codes, multi-symbol error correcting code, parallel decoder.

1. Introduction

THE phase change memory (PCM) has emerged in recent years as one of the most promising technologies for future non-volatile solid-state memories with significant implications on the entire storage hierarchy [1]. PCM has attracted considerable attention due to its low latency, good endurance, long retention and high scalability compared to other non-volatile memories. PCM relies on the reversible thermally-assisted phase transformation of the chalcogenide alloy Ge2Sb2Te5, (GST), as occurring between two structurally different phases of electrical properties: the amorphous phase with a high resistivity and the poly-crystalline phase with a low resistivity [1].

These two phases are usually referred to as the RESET and SET states, respectively [1], [2], [3]. There is a large resistance margin between the amorphous and the crystalline phases, so a PCM can store multiple bits of information in a single cell; this is accomplished through a

multilevel storage implementation based upon incomplete phase transitions [1]. Advantages such as increased storage density and hence lower cost are of primary importance for the successful development of multilevel memory systems using PCM [4]. However, the resistance of a phase change material such as GTS tends to drift over time [4], [5]. The change in resistance severely degrades the margin between adjacent levels, leading to a serious data integrity challenge [6]. For

PCM, the occurrence of the drift requires both compensation techniques in the management of the resistance range of the cells and efficient error correcting codes (ECC) [7], [8]. [8] has proposed error correction using orthogonal Latin square (OLS) codes; the OLS code provides both multiple-bit error correction and highspeed decoding [9]. However, the OLS code is a binary code and thus, it targets only bit-errors. Advances in PCM technology have already made possible the design and commercialization of quaternary cells [1], [10]; it is envisioned that in the next few years, an octal cell could be ready available as multilevel PCM. It is well known that to control non-binary data with binary codes is not very efficient. Hence, the following three features are highly desirable for PCM storage: 1) non-binary, 2) multiple-error correction and 3) parallel decoding.

The objective of this manuscript is to propose non-binary OLS codes that are amenable to a multilevel PCM addressing the above three features. The new codes are shown to have a shorter check bit length and better probability in encoding/decoding than the conventional binary OLS codes of [8]. In addition, the proposed non-binary OLS codes provide better parallel implementations for the encoder and decoder circuits in terms of area, power consumption and delay. Extensive results are provided for assessment and comparison. The proposed codes are also shown to be always better than the matrix codes of [11], [12], i.e. independently of the metric and the parameters employed in the comparison.

2. Related Work

2.1 Phase Change Memory:

This section reviews different aspects as related to PCM, resistance drift behavior and multilevel storage. As described previously, PCM is regarded as one of the most viable candidate for the next generation of non-volatile memories [1]. A PCM relies on the reversible phase transformation of the chalcogenide alloy (e.g. Ge2Sb2Te5, GST) between the amorphous and

the crystalline states. The amorphous state has a high resistance and is commonly referred to as the reset state; the crystalline phase has a low resistance and is referred as the set state. If the PCM is in the Reset state (amorphous) and the voltage across the PCM cell is higher than the threshold value, then a snapback behavior occurs and the resistance of the PCM is switched to the ON state value. If the PCM is in the ON state, it will switch back to the OFF state if and only if the voltage across the PCM is less than the so-called ON/OFF Intersection Point. A PCM cell can be used as a multilevel memory to increase capacity; this is made possible by its high resistance range, i.e. the difference between the resistances of the SET and RESET states.

However, after a PCM cell is programmed, its resistance increases with time; this phenomenon is generally known to as the resistance drift. The resistance drift is believed to be the result of structural relaxation (SR) phenomena that are thermally activated as an atomic rearrangement of the amorphous structure [10], [13]. A multilevel PCM experiences a difference in resistance drift over time, leading to a significant degradation in data integrity [13]. Fig. 1 shows the basic principles of resistance drift in a multilevel PCM cell. The resistance at each level varies according to a Gaussian distribution and accounts for less (more) drift when the PCM is in the (amorphous) crystalline phase. The resistance of each level changes during T (Fig. 1) and it could pass the threshold value (as separating two adjacent levels). This results in an erroneous output following a read. The erroneous effects of the resistance drift in a PCM cell can be alleviated if the threshold resistances could also vary with time. In [14], a time-aware fault-tolerant scheme is used for correcting the resistance drift of a PCM. The drift behavior of the threshold resistance is taken into account by keeping the socalled lifetime of the PCM in the form of time tag bits and using them to find the threshold resistances.

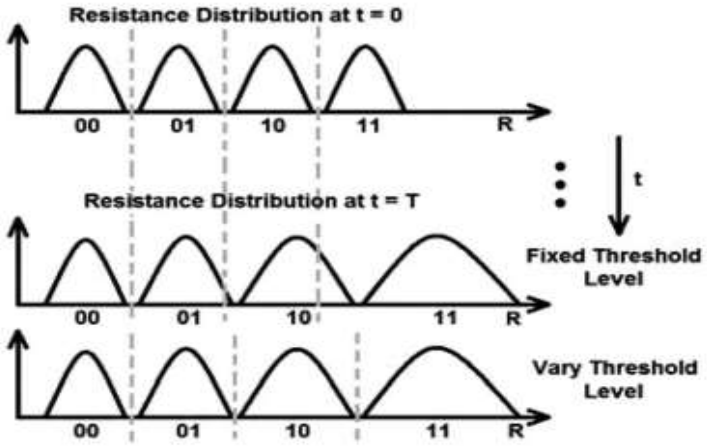

Fig 1. PCM resistance distribution over time.

Multilevel storage is achieved through an accurate programming of the PCM cell into

intermediate resistance values, i.e. the values between the SET and RESET states [1]. This scheme however, is susceptible to process and material variability; for example, the emperature that is generated in the PCM by using the same programming pulse, varies from cell to cell. Therefore, a single pulseprogramming arrangement is not a viable option for multilevel PCM storage, because the resulting resistance level distributions are rather broad and difficult to predict [15]. A possible solution is to employ an iterative programming strategy that starts by reading the most recent resistance value of a PCM and comparing with a reference value; then, a programming current is utilized to bias and adjust the resistance of the PCM cell to the desired value. However, mitigation schemes such as the ones proposed in [14] are not sufficient to deal with the issue of drift once a multilevel PCM is considered. This is mostly caused by the reduced resistance values between two adjacent levels and the characteristic that the drift is more pronounced at higher values of resistance in the PCM range. Moreover, the additional number of operations to be performed may further degrade the endurance of a non-volatile memory cell, such as a PCM [13].

2.2 Coding Techniques

The Hamming code is one of the most frequently ECCs used in a memory system [7]; it covers both binary and non-binary data, but it only corrects single errors. To control multiple errors, BCH codes and Reed-Solomon codes have been widely adopted [7]. A universal parallel decoding method has been proposed in [16]; any multiple-symbol error correcting codes, including RS codes, can be decoded in parallel using this method. However, this method incurs in a large hardware overhead when utilized for multiplesymbol error correction. Better codes can be obtained by arranging the data in the memory array and using codes with a weak capability for each row and column; these are generally known as matrix codes (also referred as product codes) [7]. Decoding of matrix codes is generally difficult; recently, a decoding algorithm for a double-error correcting matrix code has been proposed in [11], [12] that partially alleviates this negative feature. The low- density parity check (LDPC) code is another wellknown class of codes capable of correcting multiple errors. LDPC codes are usually decoded by iterative decoding schemes, such as the one used for PCM in [14]. However, this scheme requires a long time for decoding. Chen et al. have proposed a high-speed decoding scheme for LDPC codes by satisfying the so-called

rowcolumn (RC) constraint [17]. It has been proved [17] that if and only if a code satisfies the RC constraint in the parity check H matrix, no two rows or two columns have more than one place where they both have nonzero elements. This scheme is based on one-step majority-logic decoding (OSMLGD) [7]. Hsiao et al. [9] has proposed an OLS code capable of correcting multi-bit errors.

As it satisfies the RC constraint, this code can be decoded at highspeed using OSMLGD [10], thus confirming the excellent suitability of the OLS code for a memory system [17]. Datta and Touba [8] has shown that the OLS code can be used in a PCM; it should be noted that the OLS code is a binary code targeting only bit-errors.

3. Implementation

This section presents the proposed non-binary multi-symbol error correcting OLS codes to accomplish the following features as highly desirable for PCM storage: 1) non-binary, 2) multipleerror correction and 3) parallel decoding. They are reflected in the H matrix and the encoder/decoder designs as treated next. The proposed non-binary OLS code can be constructed over finite rings. However, PCM requires codes over only GFð2bÞ; so, the hardware amount of decoder can be reduced for codes over GFð2bÞ. Consider first the H matrix. The proposed code is over a finite ring. The proposed (n symbols, k symbols) t-symbol error correcting code uses the same H matrix as an (n bits, k bits) binary t-bit error correcting OLS code (the H matrix consists of only additive and multiplicative identities, 0 and 1). This condition is valid because the H matrix of the non-binary OLS code satisfies the RC constraint.

In addition, the minimum column weight of the H matrix is the same, i.e. 2t. Therefore the minimum distance of the proposed nonbinary OLS code is 2t þ 1, and the proposed code is capable of correcting t-symbol errors. The relation between the information symbol length k, the check symbol length r and the number of correctable error symbols t is the same as that for the binary OLS code, i.e. r 2td Ffiffiffi pke. Figs. 2 and 3 illustrate the block diagrams of the encoder and decoder for the proposed code. These circuits have a traditional structure, so the check symbol generator in the encoder, and the syndrome generator and the adder in the decoder can also be implemented in a traditional scheme using additional circuitry for the ring (i.e. the XOR gates for codes over GF(2b)).

Next, the construction of the error pattern calculator in the decoder is described. This uses

OSMLGD [7]. Let Sj be a vector that contains all ith elements si in a syndrome (s0;s1; . . .;sðr

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1Þ), such that h i,j in the H matrix is 1. The error magnitude ej in the jth symbol of the received word is found by calculating the majority in Sj and a value 0 when a t-symbol error occurs. This is valid because if the value of the jth symbol changes from vj to vj þ ej, at least t þ 1 symbols in Sj are equal to ej. Moreover, f the value of the jth symbol does not change, at least t symbols are 0. Next consider GF(2b). A circuit of reduced complexity can be used as majority circuit in a decoder for a non-binary OLS codes over GF(2b). The circuit does not use b-to-2b decoders and 2b-to-b encoders. Instead, it counts the number of 1's in the binary-coded digits. It does not always work as a majority circuit; however, it has sufficient functionality for use in the decoder. For example, if Sj ¼ ð3; 3; 4; 5Þ ¼ ð011; 011; 100; 101Þ over GF(23), then it outputs 1 ¼ (001) although the majority is 3.

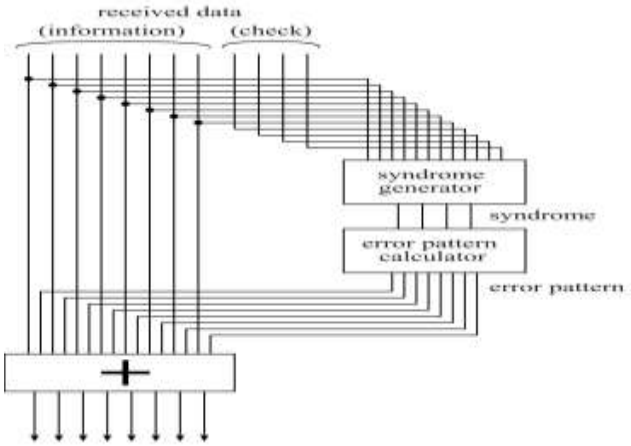
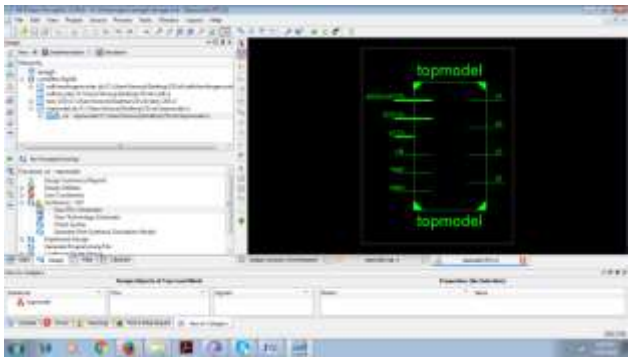
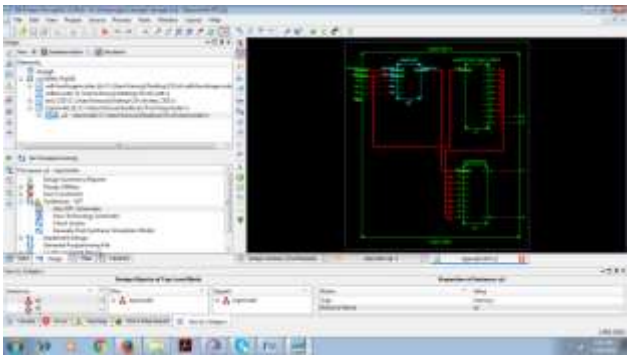


Fig 3. Proposed decoder design.

However, such Sj does not appear when a t-symbol error occurs (as previously discussed). At least t þ 1 symbols in Sj are equal to the error magnitude ej, and thus, every bit in the binary-coded ej is selected as the majority for each digit.

4. Experienced Work:





5. Conclusion

This paper has presented a non-binary OLS code as applicable to multilevel a PCM. A PCM utilizes a multilevel scheme that permits to increase the storage density using ternary, quaternary and in the near future, octal cells. The resistance drift that occurs in a multilevel PCM due to the resistive characteristics of GST, may cause errors in the stored information, thus degrading data integrity. The proposed codes utilize a non-binary scheme that is capable of correcting multi-symbol errors with a parallel decoder. The proposed (n symbols, k symbols) t-symbol error correcting code uses the same H matrix as an (n bits, k bits) t-bit error correcting binary OLS codes. It utilizes a shorter check length and higher reliability for information symbol length of approximately 103 or less than binary OLS codes. In addition, the parallel schemes for encoding and decoding in the proposed codes have been shown to be better than those for binary OLS codes in terms of area, power consumption and delay.

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