

A Design Approach for Compressor Based Approximate Multipliers

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Abstract:

Approximate computing is best suited for error resilient applications, such as signal processing and multimedia. Approximate computing reduces accuracy, but it still provides meaningful and faster results with usually lower power consumption; this is particularly attractive for arithmetic circuits. In this paper, a new design approach is proposed to exploit the partitions of partial products using recursive multiplication for compressor-based approximate multipliers. Four multiplier designs are proposed using 4:2 approximate compressors. Extensive simulation results show that the proposed designs achieve significant accuracy improvement together with power and delay reductions compared to previous approximate designs. An image processing application is also presented to show the efficiency of the proposed designs.

Keywords—Approximate computing, compressor, multiplier

I. INTRODUCTION:

scientific and engineering Many problems are computed using accurate, precise and deterministic algorithms. However, in applications involving signal/image manv processing and multimedia, exact and accurate computations are not always necessary, because these applications are error tolerant and produce results that are good enough for human perception [1]. In these error resilient applications, a reduction in circuit complexity, and thus, area, power and delay is very important for the operation of a circuit. Hence, approximate computing can be used in error tolerant applications by reducing accuracy, but still providing meaningful results faster and/or with lower power consumption [2].

Addition and multiplication are often used in these applications. For addition, full adders have been analyzed in detail and a number of approximate designs have been proposed [1]. In [3], several new metrics are proposed and a comparison is made among some of the adder designs. The error distance (ED) is defined as the arithmetic distance between an erroneous and the correct outputs for a given input. The mean error distance (MED) and normalized error distance (NED) are then proposed.

Recently, approximate multipliers have also gained significance because of their



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importance in arithmetic operations [4–10]; several approximate 4:2 compressors have been proposed in the reduction of the partial products of a Dadda tree. In this paper, the approximate compressors of [10] are utilized to design 8x8 bit multipliers by a novel partition of the partial products. The newly-designed approximate multipliers are more accurate than the ones proposed in [10] and require approximately the same power and delay; it is shown that the improvement in accuracy is significant, albeit at a slightly increase in area.

This paper is organized as follows. Section II reviews approximate multipliers and the compressors used in the proposed designs. Section III presents the proposed multipliers. Section IV provides the simulation results for the multipliers and compares the proposed design with [10]. Section V presents an image processing application using the approximate multipliers and Section VI gives the conclusion.

II. Approximate multipliers:

An error tolerant multiplier (ETM) uses accuracy as a design parameter and divides the operands into two parts – multiplication and non–multiplication, depending on the required accuracy [4]. It performs the multiplication only in the first part, thus saving power and delay at the cost of accuracy. A novel 2x2 bit underdesigned multiplier (UDM) is proposed and used to build a larger multiplier [5]. [6] presents a 6x6 bit broken array multiplier (BAM), that is faster than an accurate array multiplier. [7] proposes a 4x4 imprecise counter-based multiplier (ICM) that uses a 4:2 inaccurate counter to reduce the partial product stages of a Wallace tree multiplier. It leads to a power efficient design, which can then be used to implement multipliers of large sizes. Four different modes of an approximate Wallace tree multiplier (AWTM) are presented in [8]. This design uses a carry-in prediction method, resulting in hardware reduction and thus, less power, area and delay compared to the accurate Wallace tree multiplier. Also, AWTM uses the simple recursive multiplication technique that has also been used in this paper and explained in Section II.C. [9] proposes a fast and powerefficient multiplier based on an approximate adder that can process data in parallel by cutting the carry propagation chain. Two new approximate 4:2 compressors and four approximate multipliers are proposed in [10]. Similar compressors have been used in the partial product reduction stage in the multipliers proposed in this paper. Most of the approximate multipliers aim for a tradeoff in accuracy, power, delay and area.

Recursive multiplication:

This technique used in this paper for designing 8x8 multipliers using 4x4 multipliers is known as recursive multiplication. Suppose there are 2 numbers A and B of 2a bits each. It is possible to break the two numbers into 2 halves, i.e., most significant a bits and least significant a bits. So ah denotes the upper a bits of A. al denotes the lower a bits of A and similarly. Bh and bl denotes the upper and the lower a bits of B respectively. Then instead of performing a 2ax2a multiplication. Four axa multiplications are performed and added to get the final output.



Accurate compressor:

Compressors are used to reduce the number of partial product stages. The basic structure of an accurate 4:2 compressor chain utilized in the partial product reduction. Compressor produces a sum for the same order of the next stage, and a carry for one order higher in the next stage. Also a carry out is generated and becomes the carry in of the next higher order compressor. A 4:2 accurate compressor is implemented using two full adder circuits. There are many other designs for implementing the accurate compressor. It describes a design for the 4:2 accurate compressor using three xor-xnor gates. One xor gate and two 2:1 multiplexers. The logic equations for these compressor are as follows:

> $Sum = A \oplus B \oplus C \oplus D \oplus C_{in}$ $C_{out} = (A \oplus B)C_{in} + AB$ $Carry = (A \oplus B \oplus C \oplus D)C_{in} + |(A \oplus B \oplus C)D$



An accurate compressor using two full adders **Approximate compressors utilized:**

The two designs of inaccurate compressors as proposed and have been used in this paper when designing multipliers. Both designs are based on the modification of the truth table of the accurate compressor to reduce the hardware. The carry signal is directly connected to the cin, signal and the columns of the sum and cout signals are modified to reduce the hardware, and hence reducing the delay. The logic functions are given as:

$$Sum = (\overline{(A \oplus B)} + \overline{(C \oplus D)})\overline{C_{in}}$$
$$C_{out} = (\overline{(A + B)} + \overline{(C + D)})$$
$$Carry = C_{in}$$

It is completely removed from the circuit and hence, there is no need of cin, as well. Hence, this design further simplifies the



circuit and gives better results in terms of accuracy. The logic functions are given as:

$$Sum = \overline{(A \oplus B)} + \overline{(C \oplus D)}$$
$$Carry = \overline{(\overline{A + B}) + (\overline{C + D}))}$$





Logic diagram for the 4:2 compressor

III. Proposed design:

The proposed 8x8 multiplier designs are presented. Since the technique of recursive multiplication is used, 4x4 multipliers are required for the implementation of the 8x8 product. Hence, the 4x4 multiplier design are presented too. The method of recursive multiplication gives partial product tree to illustrate its difference from a conventional design.

4X4 bit designs:

Three 4x4 bit multipliers have been implemented and further used in the 8x8 bit multiplication. All three designs are implemented using the Dadda tree technique by making use of difference 4:2 compressors in the reduction stage. Using the compressors, the 4x4 bit product requires one reduction stage, making the product calculation faster.

For the accurate 4x4 multiplier, the Dadda tree multiplier implementation is the same because the accurate compressor use the same type of circuits. Hence, only accurate compressors need to be used in place of the compressors. In this multipler, two accurate compressors are required in the reduction stage.



Use of compressor for partial product generation



IV. Simulation results:



Simulation results for compressor based multiplication

V. Conclusion:

In this paper, four designs of 8x8 bit approximate multipliers have been proposed. Simulation results have been reported for design and error metrics. Also, an image processing application has been presented in detail. The proposed designs show significant improvements in accuracy, power and latency at a cost of a slightly larger area.

For accuracy, the proposed Mul88_1 and Mul88_2 achieve improvements of 76.67% and 93.55% over design 4 of [10] (as the most accurate design in [10]). The four proposed designs are also efficient in terms of power, showing improvements of 4.36%, 3.21%, 20.27% and 14.24%, respectively, compared to design 4 of [10]. An improvement in delay is also obtained in the proposed multipliers, but the circuit areas of the proposed designs are higher than design 4 of [10] by 11.07%, 11.21%, 3.35% and 3.78%, respectively. This is due to the use of an additional 9- bit adder (in [10], only one 16-bit adder is required).

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