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A New PWM technique for Voltage balancing in High power Cascaded Converters

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ABSTRACT: For single-phase supplies adedicated pulse width modulation (PWM) methoddesigned for cascaded H-bridge converters isoffered to scale down the DC-link voltageunbalance independently from the amplitude of theDC-link voltage reference and compensatesswitching devices voltage drops and on-stateresistances with that an expand in waveformgreat can be done most often, relevant in excessivepower low frequency operations. Eliminatesfurther control loop for DC-hyperlink voltagebalancing capacity to actively stability the DC-linkvoltage on each and every H-bridge which simplifies themanipulate constitution. The proposed modulationprocedure has been validated by means of the use ofsimulation based on fuzzy logic controller.

KEYWORDS-Multilevel converters,predictive control, smart grid, fuzzy logic controller.

I. INTRODUCTION

In recent years, multilevel inverters have gained much attention in the application areas of medium voltage and highpower. Multilevel converters utilize several DC voltages to synthesize a desired AC voltage. For this reason, multilevelconverters can reduce (dv/dt) to conquer the motor failure problem and EMI problems. Multilevel converters alsohave emerged as the solution for working with higher voltage levels. Multilevel converters include an array of powersemiconductors and capacitor voltage sources, which generate output voltages with stepped waveforms. Thecommutation of the switches permits the addition of the capacitor voltages, which reach high voltage at the output,while the power semiconductors must withstand only reduced voltages.Voltage steps in multilevel inverters might not be the same. Available DC sources of the cascade multilevel invertersare batteries, photovoltaic arrays, fuel cells, rectifiers…etc. In cascade multilevel inverter based photovoltaic systems,the operating DC voltages of standard photovoltaic cells range from 15V to 35V. In the cascade multilevel inverterbased energy storage system with batteries, the voltages of batteries also change due to their states of charge. Thevarying voltages of DC sources result in varying voltage steps in the multilevel output waveform. The varying voltagesteps (varying DC source voltages) bring challenges to the algorithms in determining switching angles. Not onlyswitching angles, but also the variations of voltage steps, will determine the harmonic distortion of output voltages.

The main issues with the CHBconverter is the requirement for isolated DC-Linkvoltages as well as the significant effect of devicevoltage drop and on-state resistance inapplications with high number of levels andrelatively low application ac side voltages.Furthermore, in the active rectifier configuration,balanced DC-Link voltages are required toachieve optimal operation considering asymmetrical (and therefore fully modular)configuration. DC-Link voltage balancingmethods have been proposed in literature for CHBactive rectifiers and they can be divided into twomain groups depending on whether the DC-Linkvoltage balancing method is integrated in thecontroller [8], using additional controlloops, or directly into the modulator. Inthis paper, the latter case is considered and anovel modulation technique, developed for singlephase systems and suitable for high powermultilevel CHB converters, is introduced. Theproposed modulation strategy is based on theDistributed Commutation Modulator (DCM),described. DCM is a pulse widthmodulation (PWM) technique specificallydesigned for multilevel CHB converters. The aimof DCM is to minimize the

commutationfrequency of the individual devices, distributingthese commutations evenly among the converterHB cells. As a result, the converter losses areequally distributed across the devices, increasingthe converter reliability, without compromisingoutput voltage waveform quality. However, thebalancing of the DC-Link voltages represents anissue for the DCM strategy as such a technique isable to passively balance the DC Link voltagesonly when balanced dc currents are demanded.Moreover, in the DCM technique, the devicesvoltage drops and on-state resistances are notconsidered. In order to overcome these issues, anactive DC-Link voltage balancing algorithm hasbeen designed for DCM which accounts for thedevice voltage drops and on-state resistances,improving the output voltage waveform qualityand maintaining good performances even whenunbalanced dc currents are demanded. In theconcept of DC-Link voltage balancing algorithmis introduced as well as the device voltage dropand on-state resistance compensation.

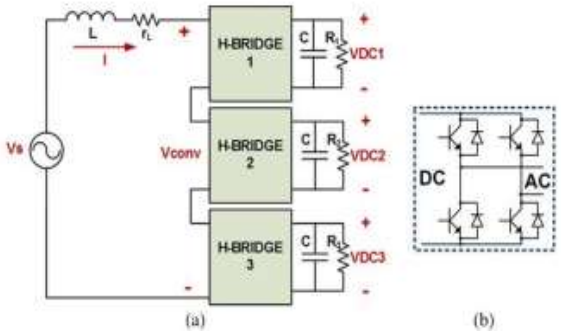

Fig. 1.(a) Schematic diagram of a 7-level CHB inactive rectifier configuration, and (b) a single HBcircuit.

The maintarget of the proposed modulation strategy is, incontrast with DCM, to minimize the DC-Linkvoltage unbalance among the different convertercells in order to maintain the converter modularityand produce high quality waveforms, even if alow switching frequency is considered. Referringto Fig. 1, the DC-Link voltage affects thedistribution of the commutations among thedevices only for unbalanced loads, i.e., when $R_1 \neq R_2 \neq R_3$. When the loads are balanced, i.e.,when $R_1 = R_2 = R_3$, the device commutations areequally distributed among the CHB cells. Whencompared to other DC-Link voltage balancingtechniques, the proposed algorithm presents avery fast and accurate response, avoiding the useof additional control loops. The device voltagedrops and on state resistances are alsocompensated, producing higher quality outputvoltage waveforms, in particular, in applicationswhere a large number of CHB cells are used witha relatively low target ac side waveformmagnitude, i.e., automotive applications.

II. PROPOSEDCONTROL STRATEGY

As stated in the introduction, the maingoal of the proposed modulation method is tominimize DC-Link voltage imbalances andcompensate the device voltage drops and on stateresistances. To achieve such a result, a fastresponse to any unbalance on the dc loads isrequired. For this reason the balancing algorithmis fully integrated into the modulation scheme,without using any additional controllers. It isimportant to note that since one of the targets ofthe proposed algorithm is to equalize the voltageson the capacitors; their average value isconsidered as the reference voltage for each DClink capacitor in the algorithm, while the totalDC-Link voltage is set to the reference valueusing a Proportional-Integral action external to themodulator. In order to reduce stress on the powerswitches and improve their reliability, thecommutations are permitted only betweenadjacent voltage levels i.e., it is possible to switchonly one leg of one H-Bridge cell during everysampling interval. The algorithm is modular andapplicable to a generic *n-level*CHB converter;however increasing the number of voltage levelsrequires an obvious increase in computationaleffort.

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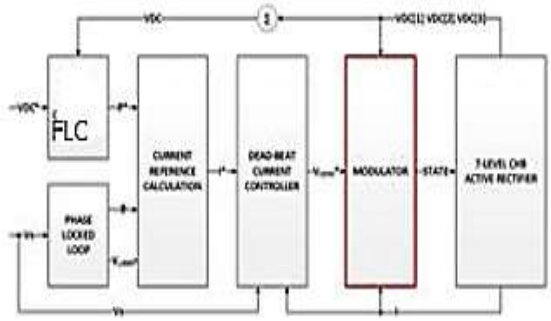

Fig.2. Overall control scheme

A. Control Scheme

Fig. 2, shows the control block diagramimplemented for the converter of Fig. 1, where V_{DC} denotes the total DC-Link voltage and $V_{DC}*$ is the desired DC-Link voltage. A singlephase Phase-Locked-Loop (PLL) is used in thecontrol scheme to obtain the supply phase angle, θ ,and RMS value, $V_{S,RMS}$. The PLL scheme isobtained by cascading the orthogonal systemgenerator proposed in [37], based on the SecondOrder Generalized Integrator, with the three-phasePLL presented in [38], based on a steady-statelinear Kalman filter. The line current is controlledin order to obtain the required DC-Link voltage;to achieve this goal, the current reference I∗iscalculated, at every sampling period T_s of thecontroller, as follows [39]:

$$I^*(t_k + iT_s) = \frac{P^*}{V_{s,RMS}\sqrt{2}}\sin(\theta + iT_s), i = 1,2\ldots..(1)$$

Where P^* is the required power, imposed by thevoltage fuzzy logic controller and t_k is the currenttime instant. The current reference I^* is predictedat two sampling instants, $T_s$and $2T_s$, in order toobtain a Dead-Beat current control law, describedin [40]–[42] for various converter configurations,and in [23], [39] specifically for the proposed 7-Level CHB. The obtained control law is used toderive the desired voltage reference V^*_{CONV} according to the following expression:

$$V^*_{CONV}(t_k + T_s) = V_s(t_k + T_s) - \frac{L}{2T_s}[I^*(t_k + 2T_s) - I(t_k)] + r_L I^*(t_k + T_s) \quad \ldots\ldots\ldots(2)$$

The control output represents the desiredconverter voltage average value during the nextsampling interval, applied using the proposedmodulation scheme.

B. Distributed Commutation Modulator(DCM)

As mentioned in the introduction, the proposedtechnique can be seen as an improvement to theDCM technique [30], [31] where thecommutations are distributed among the three HBridges in order to reduce the device switchingfrequency, and optimize the converter losses.Under normal operating conditions, the nconverter cells are able to commutate sequentiallyso that each one can perform only onecommutation every n sampling periods.Commutations are permitted only betweenadjacent voltage levels. As a consequence, thetotal switchingfrequency is half of the sampling frequency, whilethe device switching frequency of a single cell isapproximately1/(n−1) for an *n-level*CHB.

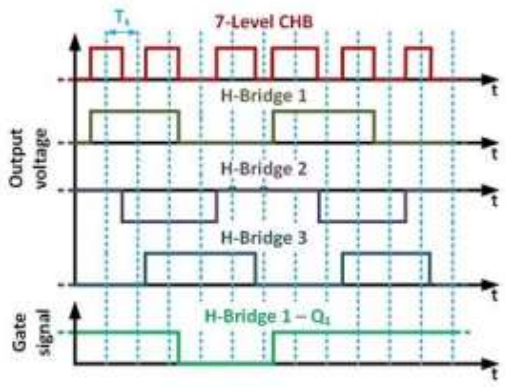

Fig.3. DCM technique working principle.

Anexample of normal operation is given in Fig. 4where the 7-Level CHB of Fig. 1 is controlled inorder to obtain a positive square waveform. As itis possible to see from the first waveform in Fig.3, given a sampling frequency $f_s = 1/T_s$, thewaveform produced by the 7 level CHB has aswitching frequency $f_{sw} = f_s$. The H-Bridges areforced to commutate sequentially obtaining aswitching frequency for a single H-Bridgeof $f_{swHB} = f_{sw}/3$ Taking advantage of the zerovector redundancy, it is

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possible to obtain, for thedevice Q_1 of the H-Bridge 1, a switchingfrequency equal to . Clearly thisoperation condition is not always feasible when amulti-level waveform is produced and themodulation algorithm attempts to distribute thecommutations among the devices. Two mainissues have been identified using this technique.

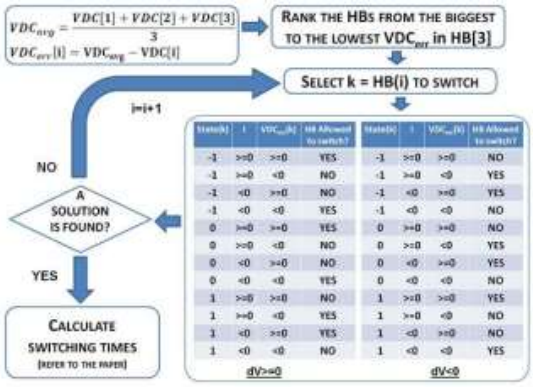

Fig.4. DC voltage balancing basic principle.

The DC-Link voltage balance is achieved with asymmetrical load on the three HBs and in anyother case an additional control is required. Thesecond issue appears in the case of high-powerbut relatively low voltage applications utilizing alarge number of CHB cells, where the devicevoltage drops and on-state resistances cannegatively affect the behavior of the modulator.An additional algorithm, described below, hasbeen implemented to overcome these issues.

III. OPERATION PRINCIPLE OF DG

FLC containsthree basic parts: Fuzzification, Base rule, andDefuzzification. FLC has two inputs which are: errorand the change in error, and one output. The FuzzyController structure is represented in fig.5. The roleof each block is the following:

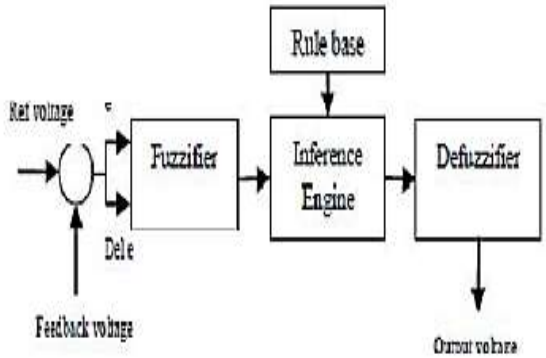

Fig.5. The general structure of Fuzzy LogicController

Fuzzifier converts a numerical variable into a linguistic label.. In a closed loop control system, the error (e) between the reference voltage and the output voltage and the rate of change of error (del e) can be labeled as zero (ZE), positive small (PS), negative small (NS), etc. In the real world, measured quantities are real numbers (crisp). The FLC takes two inputs, i.e., the error and the rate of change of error. Based on these inputs, The FLC takes an intelligent decision on the amount of field voltage to be applied which is taken as the output and applied directly to the field winding of generator. Triangular membership functions were used for the controller.

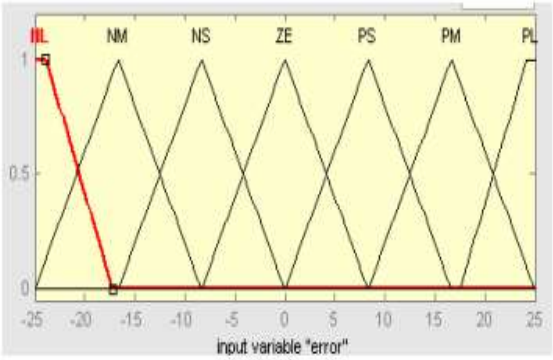

Fig .6. Membership function of voltage

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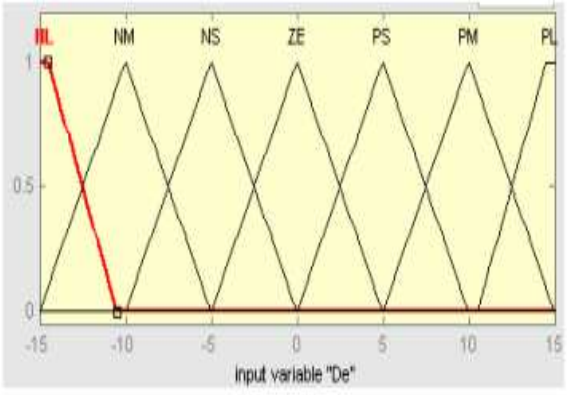

Fig.7. Membership function of voltage error

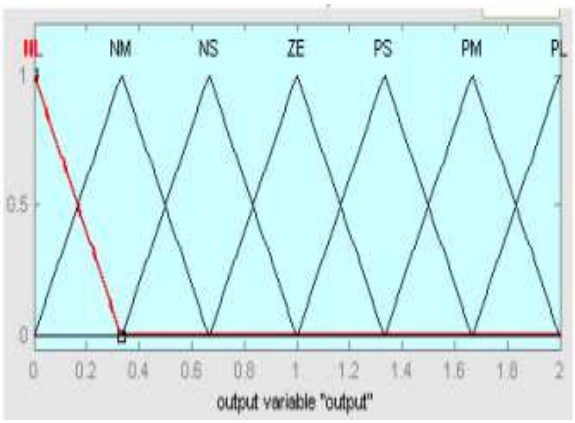

Fig .8. Membership function of output field voltage

Rule base stores the data that defines theinput and the output fuzzy sets, as well as the fuzzyrules that describe the control strategy. Mamdanimethod is used in this paper. Seven membershipfunctions were used leading to 49 rules in the rulebase.

Table: Rule base for fuzzy controller

ΔE \ E	NB	NM	NS	ZE	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	ZE
NM	NB	NB	NM	NM	NS	ZE	PS
NS	NB	NM	NS	NS	ZE	PS	PM
ZE	NB	NM	NS	ZE	PS	PM	PB
PS	NM	NS	ZE	PS	PS	PM	PB
PM	NS	ZE	PS	PM	PM	PB	PB
PB	ZE	PS	PM	PB	PB	PB	PB

Inference engine applies the fuzzy rules tothe input fuzzy variables to obtain the output values.Defuzzifier achieves output signals based on theoutput fuzzy sets obtained as the result of fuzzyreasoning. Centroid defuzzifier is used here.

IV. SIMULATION AND RESULTS

Simulations have been carried out inorder to compare the performance of the proposedmodulation strategy. The power rating of theconverter considered in simulation match thepower rating used in the experimental tests (3kW). Operation in rectifier mode has been used toavoid the requirement of isolated high voltagesources. The proposed method, however, isequally as effective in the inverter modeconfiguration. In order tohighlight the effect of parasitic components, largevalues of Vdand Vq are considered duringsimulations. In this paper, the proposed modulatoris compared with the DCM technique illustratedin [31]. A comparison between the DCMtechnique and other well-known modulationtechniques for CHB converters has already beencarried out.

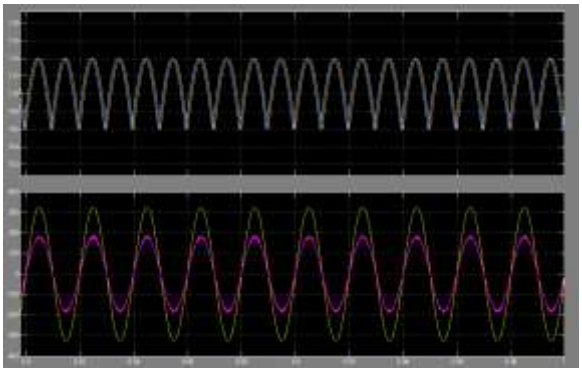

Fig .9.

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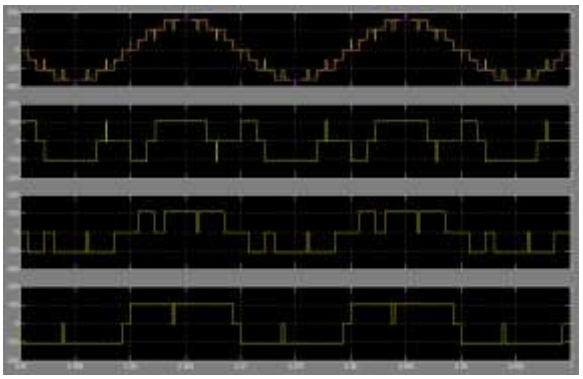

Fig .10

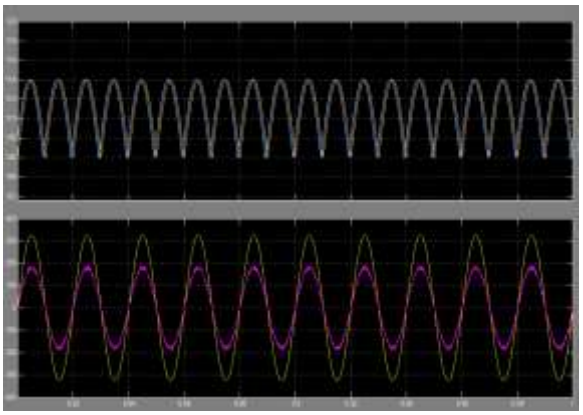

Fig .11

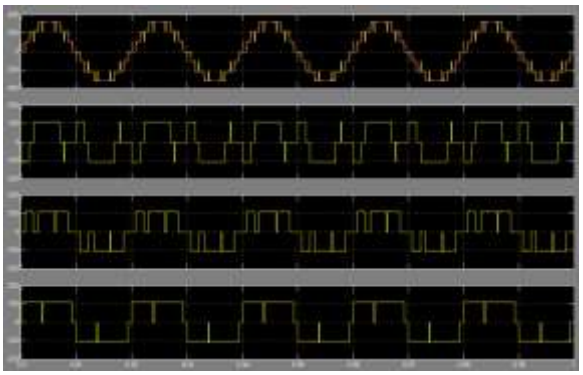

Fig .12

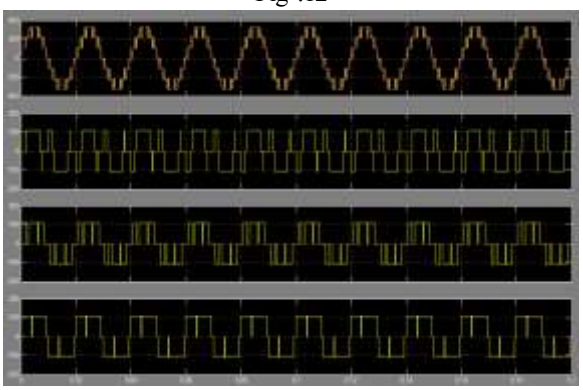

Fig .13

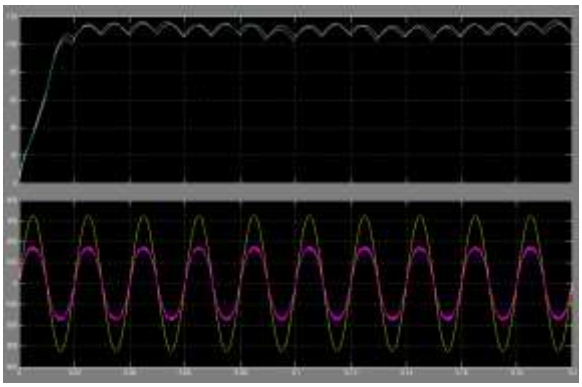

Fig .14

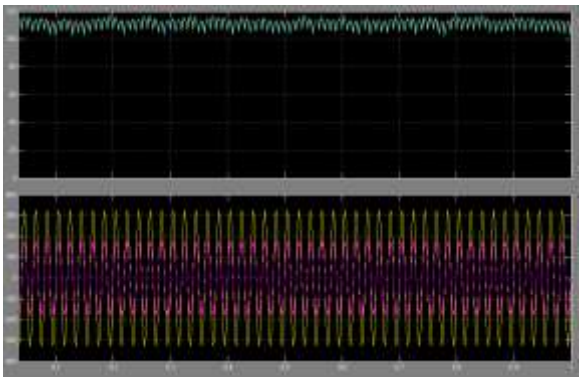

Fig .15

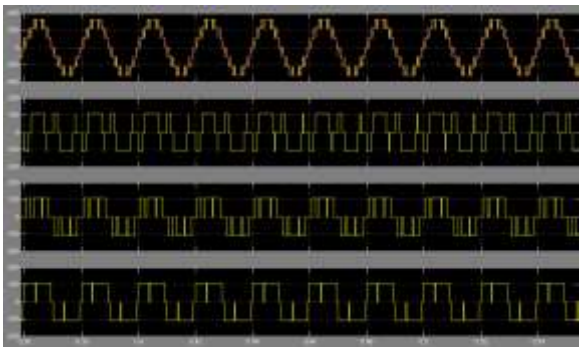

Fig .16

V. CONCLUSION

He purpose of the offeredmodulation manner is to lower theunbalance of the DC hyperlink voltages, for anyamplitude of the voltage reference, as a way toobtain excessive fine waveforms whilst retaingthe modularity of the converter. In order to acquirea

rapid response to unbalance on the dc hundreds, thebalancing algorithm is entirely built-in into themodulation scheme with out making use of any additionalcontrollers.The proposedalgorithm is established through simulation based onfuzzy good judgment controller. The simulations exhibit thatcompared to the DCM modulator, theproposed modulation process presents astability of the DC-hyperlink voltages withoutcompromising the pleasant of the waveforms, intime period of harmonic distortion, with both balancedand unbalanced dc loads. The modulator additionallynaturally distributes the commutations among the manyH-Bridge cells in case of balanced dc masses. Theproposed procedure has been validated in evaluationwith DCM on CHB back-To-again converterdisplaying that the proposed effect will not be suffering fromthe gadget parasitic parameters and converterasymmetries.

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