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Design of B-Encoder and Decoder Using Booth Multiplier

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ABSTRACT: *This paper presents the design of an encoder using booth multiplier for high security purpose. The speed of multiplier operation is of fastidious importance within the general purpose processors. The essential multiplication principle is a twofold i.e., evaluation of the partial products and accumulation of the shifted partial products with the motivation to Booth's algorithm. In this paper, an efficient design of modified Booth Encoder and Decoder scheme for high performance of multiplier has been proposed. The proposed Booth encoder and Decoder logic are competitive with the present schemes and shows enhancements in delay. The proposed system generates B, A and interconnected blocks by extending bit of the operands and generating an additional product for an encoder and similar inverse operation for the decoder. Multiplication operation is performed to operate b-encoder and decoder, which is efficient with the less area and it reduces delay i.e., speed is increased.*

INTRODUCTION

Encoder is a digital circuit that performs the inverse operation of decoder.It has '2^n' input lines and 'n' output lines and it generates the binary code corresponding to the input values. Encoders are of two types.They are incremental encoder (rotary/shaft encoder) and absolute encoder. Shafting encoder is an electro mechanical device which helps to convert the angular position or motion of a shaft or axle to an analog code or digital code. It is a pulse generator that provides a square wave signals and a zero index [7]. To overcome this problem we have gone through the absolute encoder.It has been developed to compensate for the performance and limitations of shaft.This encoder must be reserved after a power interruption zero reset is help to obtain the mechanism angular position and sensitivity of interference [1]. This absolute encoder supplies the shaft position as a binary code.

The output code is unique for each position. In this paper we focused on techniques aimed at adaptive encoding technique of power consumption by the Xilinx software.Here we use encoder and as well as decoder with the help of adders [4]. The proposed encoding schemes which are transparent with respect to the pulses are presented and discussed at both binary/algorithmic level and the architectural level by means of simulation, synthesis and real traffic scenarios.This result shows that by using the proposed encoding scheme,up to 52% of power and 16% of energy can be saved without any significant degradation.

EXISTING STAGE

Booth's multiplication algorithm is an algorithm that multiplies two binary numbers in two's complement notation. Booth multiplier uses desk calculators that were faster at shifting than adding and creates the

algorithm to increase their speed. Booth's algorithm is of interest in the study of computer architecture.

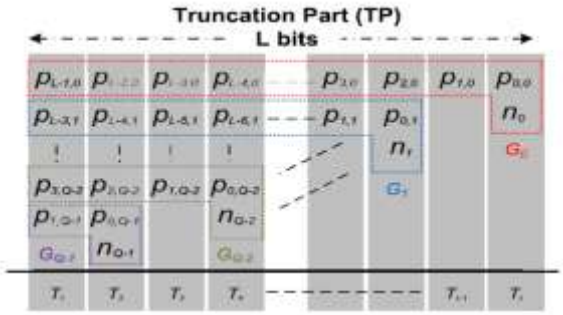

Fig 1: Truncation part

Booth's algorithm examines adjacent pairs of bits of the N-bit multiplier 'Y' in two's complement representation, including an implicit bit below the least significant bit, $y_{-1} = 0$. For each bit y_i, for i running from 0 to $N - 1$, the bits y_i and y_{i-1} are considered. Where these two bits are equal, the product accumulator P is left unchanged. Where y_i=0 and $y_{i-1} = 1$, the multiplicand times 2^i is added to P; and where $y_i = 1$ and $y_{i-1} = 0$, the multiplicand times 2^i is subtracted from P. The final value of P is the signed product.

The representations of the multiplicand and product are not specified, typically, these both are also in two's complement representation, like the multiplier. But any number system that supports addition and subtraction will work as well. As stated here, the order of the steps is not determined. Typically, it proceeds from LSB to MSB, starting at $i = 0$; the multiplication by 2^i is then typically replaced by incremental shifting of the 'P' accumulator to the right between steps. Low bits can be shifted out and subsequent additions and subtractions can then be done just on the highest N bits of P.[1] There are many variations and optimizations on these details.

The algorithm is often described as converting strings of 1s in the multiplier to a high-order '+1' and a low-order '−1' at the ends of the string. When a string runs through the MSB, there is no high-order '+1', and the net effect is interpretation as a negative of the appropriate value.

PROPOSED SYSTEM

B-Encoder: It is a better code for error controlling performance. B-Encoder outputs are not only associated with the encode elements at present, but also affected by several ones before. Data 1 'b' and data 2 'o' are used for describing codes, where Data 1 'b' is the input encode element, Data out 'e' is the output encode element and Data 2 'o' is the shift register element. Data 1 'b' and Data 2 'o' are the inputs of the Encoder. Their architecture design with chip registers perform their operations and gives output of the encoder as Data out 'e' as shown in fig2.

B-Decoder: Two parallel binary bits are inputted into the B-decoder with every clock pulse and then it begins to work when the input enabling signal is valid. Each group consists of two bits because each current state can be reached by decoder path. Here Data out 'e' is the output of the encoder similarly Data out 'e' and Data 2' 'h' are the inputs of Decoder. These inputs will perform as per their chip architecture design and the output of the decoder is Data 'd' as shown in the figure 2.

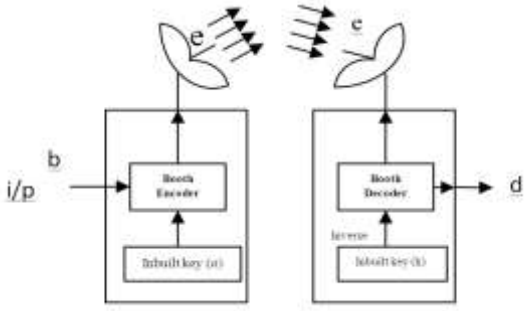

Fig 2: Booth Encoder/Decoder with Adaptive Logic

Figure 2 indicates the block diagram of Booth Encoder and decoder with adaptive logic.It consists of four shift registers and two exclusive-or gates. Every shift register is equivalent to a flip flop. These

four flip flops are connected in series to complete shifting and updating operation under the action of the clock pulse. The exclusive-or gates are used for inner operation of coding data. With every clock pulse the encoder outputs two bits according to the generator polynomials whenever one binary bit is inputted. The output is not only relevant with the current input binary bit, but also influenced by the previous bit for decoder.

Booth Decoder is designed to produce the partial products by multiplying the multiplicand, X by 0, 1, -1, 2 or -2. The output of MBE (Modified Booth Encoder) acts as the selection inputs to the partial product generator. The partial products on each row are obtained as 1's complement numbers for negative encoding. To obtain the 2's complement number, '1' is to be added at the LSB of the obtained partial product. Each partial product row is placed 2-bits to the left with respect to the previous row.

TECHNICAL SCHEMATIC:

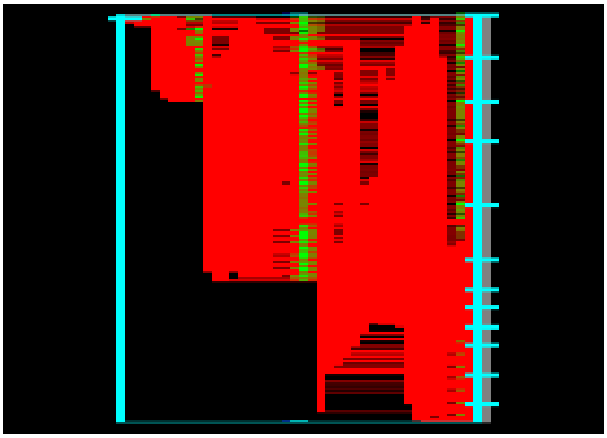

FIG 3: Technical schematic

SIMULATION RESULTS:

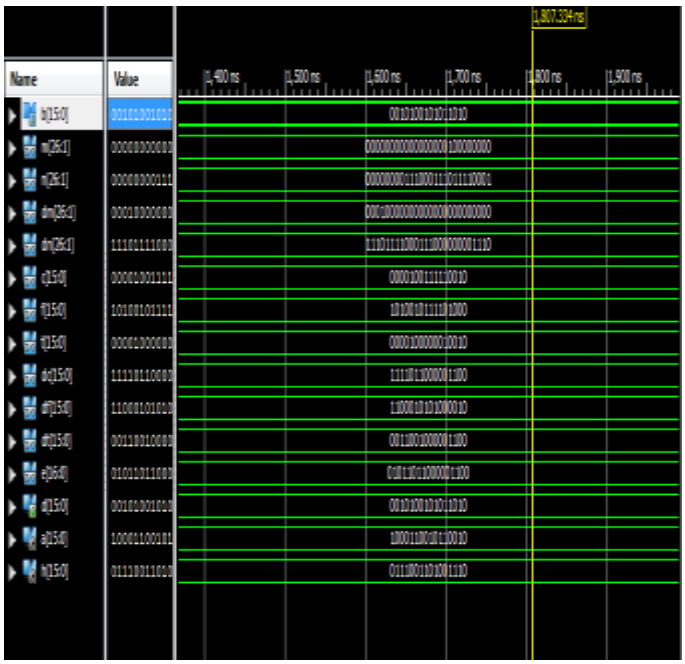

FIG 4: Output Waveform

FIG 4 shows the output waveforms of data adaptive encoding techniques. Here we have given a[15:0] as a input data for encoder and e[16:0] taken as output for encoder. As well as e[16:0] taken as input data for decoder where as d[15:0] is the output for decoder.

Table 1: Comparision table

	Delay(nano secs)	Memory(kilo bytes)
Existing system	17.53	250214
Proposed system	15.51	243412

The Booth Encoder and Decoder with logic decide the proposed algorithm to work with adaptive logic. The registers work with the adaptive techniques.By using this technique, the proposed algorithm increases the speed i.e. decreases the delay.

CONCLUSION

The booth encoding scheme has been used here which reduces the no. of partial products.With the reduced partial products the computation time is

reduced and speed of the circuit has been increased. Booth multiplier technique is used to design a high secured encoding and decoding technique to make wireless communication more efficient. Studying the existing encoding schemes we proposed a Booth encoder and decoder. The proposed encoding is inversion operation which is restricted to some encoding schemes. Booth encoder and decoder technique is very efficient in speed. The effective encoding technique gives better delay. By using proposed system we can reduce delay to 15.51ns.

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