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A Parallel Prefix High Speed KOGGE Stone Adder for Convolution Application

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Abstract— *Parallel prefix adder is used for speeding up the system's logical operation. Execution of parallel prefix adder's structure in VLSI has efficient performance. Parallel prefix adder structures are of different types i.e., Brent-Kung, Han-Carlson Adderetc. Have been projected earlier. Kogge- Stone adder with pipelining is the fastest adder structure among all of them. Kogge-Stone adder is the sub-type of parallel prefix adder in which it uses smaller amount of prefixing operation with black cells as compared with the other adder and final sum is calculated through post processing technique. In this paper, initially pipelining Kogge Stone adder is implemented and that result gives decrease in critical path delay and increase in speed.*

Key Words: Parallel Prefix Adder, pipelined Kogge stone Adder, Carry Select Adder

I. INTRODUCTION

The binary adder is that the vital element in most digital circuit styles collectively with digital signal processors and micro chip information path units. As such, intensive analysis continues to be targeted on raising the facility delay arrangement of the adder. In Very Large Scale Integration implementations, parallel-prefix adders are magnificent to own the most effective performance.

Reconfigurable logic like Field Programmable Gate Arrays has been in advance in quality in current years as a result of it offers enhanced performance in terms of speed and power over DSP-based and microprocessor-based solutions for numerous sensible styles concerning mobile DSP and telecommunications applications and a big decrease in growth time and price over Application Specific computer circuit styles. The ability benefit is particularly vital with the growing quality of mobile and transportable physical science, that create rigorous use of DSP functions.

However, due to the structure of the configurable logic and routing possessions in Field Programmable Gate Arrays, parallel-prefix adders can have aunusual performance than Very Large Scale addition implementations. Exclusively, most up-to-date Field Programmable Gate Arrays use a fast-carry chain that optimizes the carry path for the straightforward Ripple Carry Adder. For the period of this paper, the reasonable problems concerned in coming up with and implementing tree-based adders on Field Programmable Gate Arrays.

II. EXISTED SYSTEM

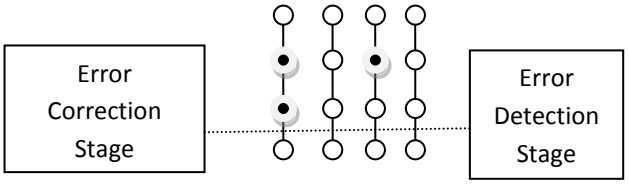

FIG. 1 EXISTED SYSTEM

The existed system consists of error correction stage to clear the errors detected by error detection stage. The working standard of the Arithmetic Logic Units is to examine the data which was send to the ALU. In general, we can compute the values line by line or in the order. It will take some more time than the actual time. There will be lot of time is intense in the process. To rectify this problem, a new technique has been introduced in the digital computer system. That is Parallel Prefix Adder.

III PROPOSED SYSTSEM

Adders are the important components in the digital computer systems due to their fast functionality in their work. The main purpose of these adders is to calculate the address in quick time. Among all the adders Parallel Prefix Adder is the main useful adder. Adders are to calculate the address and to give the solutions to the problems in no time. Kogge Stone Adder is one of the common types of parallel prefix adder. Kogge – Stone adder has been developed by Xilinx 14.7 software which is more advantageous and more developed.

If the complete operation is leaded by the inputs of the initials, that is called prefix. If the execution of the operation is been in parallel condition it is called parallel. This will be done by making the operation into some small pieces. The main profit in this technique is that the operation or the calculation part will be completed in parallel direction. The former calculating techniques will make the calculations in one by one process. But in this technique the calculations will be considered in parallel condition. Then there will be lot of time can be saved.

Parallel Prefix Adder (PPA) will be divided into three parts, i.e., prepossessing stage, carry generation network and post-processing. Pre-possessing stage is to calculate, produce and spread the signals. Carry generation network is to calculate the values in parallel level and these calculations will be segmented in minute pieces. Finally, the Post-processing stage is to complete the calculation part by collecting all the bits.

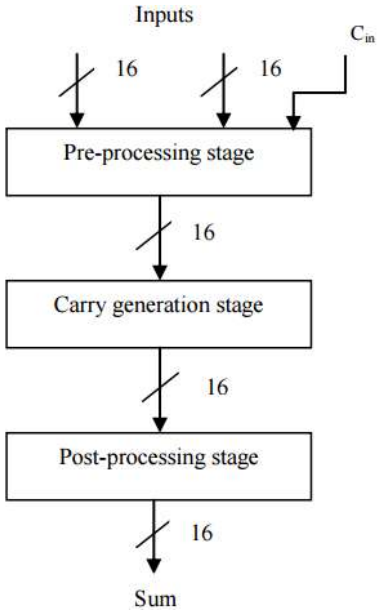

FIG. 2 BLOCK DIAGRAM

PRE-PROCESSING STAGE:

In the pre-processing stage, produce and propagate are from each pair of inputs. The propagate gives the operations of "XOR" of input bits and generates gives "AND" operation of input bits. The propagate (Pi)and generate (Gi) are shown in under equations.

$$P_i = A_i \text{ XOR } B_i$$

CARRY GENERATION STAGE:

In this stage, carry is generated for each one of the bit and this is called as carry generate (Cg). The carry propagate and carry generate is generated for the further process but final cell present in the each bit process gives carry. The last bit carry will help to make sum of the next bit concurrently till the last bit. The carry generate and carry propagate are specified in below equations.

$$C_p = P_1 \text{ AND } P_0$$

$$C_g = G_1 \text{ OR } (P_1 \text{ AND } G_0)$$

The above carry propagate Cp and carry generation Cg in equations is black cell and the below shown carry generation in equation is gray cell. The carry propagate is generated for the additionalprocess but final cell present in the each bit operation gives carry. The last bit carry will help to create sum of the next bit concurrently till the last bit. This carry is used for the next bit sum procedure, the carry generate is given in below equations.

$$SUM = P_i \text{ xor } g_{i\_pre\_last}$$

POST-PROCESSING STAGE:

It is the finishing stage of a resourceful adder, the carry of a primary bit is XORed with the next bit of propagates then the output is given as sum and it is shown in equation.

It is used for two sixteen bit operations of addition and each bit carry is undergoes post-processing stage with propagate, gives the final sum.

The first input bits goes under pre-processing stage and it will create propagate and generate. These propagates and generates undergoes carry generation stage produces carry generates and carry propagates, these undergoes post-processing stage and gives final sum.

The well-organized adder structure is looking like tree structure for the high arrangement of mathematical operations and it is the fastest and best adder which focuses on gate level logic. It designs with less number of gates. So, it decreases the holdup and memory used in this architecture.

Kogge Stone Adder with pipelining is one of the parallel prefix adder and in the form of carry Look-ahead adder but it is done the operation in parallel way with pipelining. This can be represented as parallel prefix graph consisting of nodes of carry operators. Now-a-days all the industries are adopting this technique only for the fastness of the adder. It can send the signals very fast and respond very fast. The performance of the adder also is in accurate. The bounded fan out and minimum logic depth is the main reasons for the fastness of the Kogge Stone Adder. To get the high performance in industries, they are acquiring this technique.

To implement this design, Parallel prefix adder is designed with modeling of data flow style.

Here we are using 32 bit parallel prefix adder and it is useful to avoid the overlap of sub-terms of the prefix.

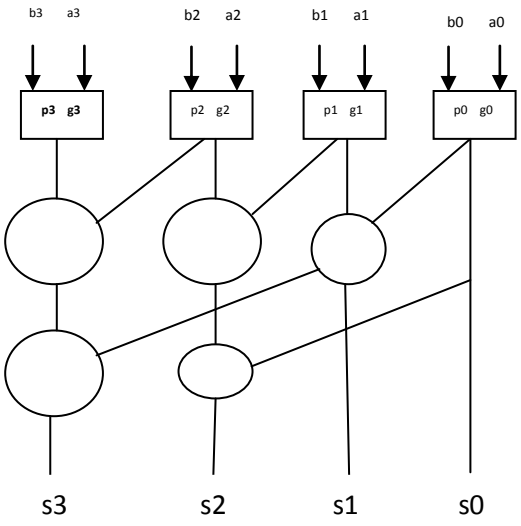

FIG. 3PROPOSED SYSTEM

To minimize the number of calculating steps, dot operator is associated in this technique. In this operator two cells are prepared, one is odd-dot and the second one is even-dot, represented as dark and light symbols like and respectively. The first cells are active in low inputs and produce the active high outputs. And second cells are active in high inputs and low outputs. The proposed system didn't require any error correction and detection circuit because it gives ~99% accuracy.

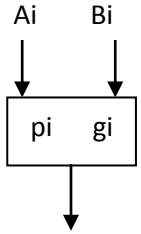

FIG. 4 PRE-PROCESSING STAGE

The above figure 4 is the pre processing operation block. Parallel prefix adder has the lower delay of power when compared with other adders. Power will be saved by using this method than that of other methods. This is more suitable design and method for Arithmetic Logic Unit to work properly and accurately. It is also useful for yielding good performance in the calculating the data.

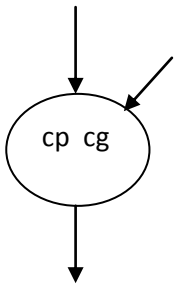

FIG. 5INTERMEDIATE OPERATION

IV RESULTS

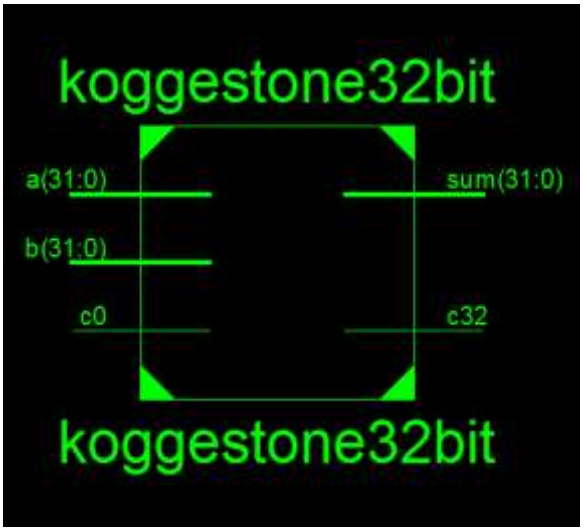

FIG. 6 R.T.L SCHEMATIC

This **schematic** is generated after the HDL synthesis phase of the synthesis process. It shows a representation of the pre-optimized design in terms of generic symbols, such as

adders, multipliers, counters, AND gates, and OR gates, that are independent of the targeted Xilinx device.

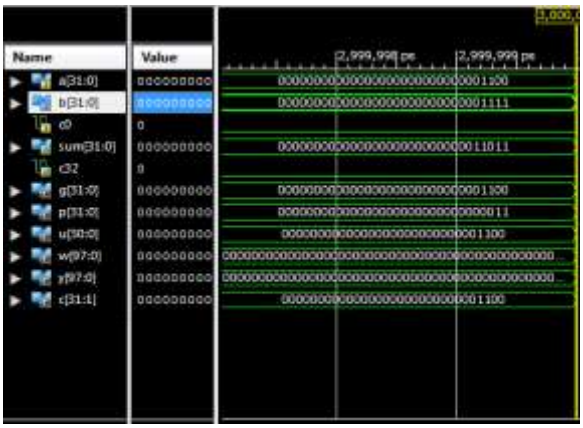

FIG. 7 OUTPUT WAVEFORM

V. CONCLUSION

Parallel Prefix Adder is a type of procedure that amplifies the speed of arithmetic operations of the system. The replication and synthesis of theKogge-Stone adder have been performed on ISim Verilog simulator. The area needed has been measured in terms of slices, flip-flops, LUTs and IOBs. The synthesis results show that consumption of the number of slices has been found to be 138 out of 960, number of LUTs are 241 out of 1920 and with delay of 15.197ns ofKogge-Stone adder. On comparing with Basicadder, it is observed that the customized design shows the development in speed with considerable decrease in delay. In future extent,the parallel prefix adders must be tested for other adders also to optimize the area and timing both.

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