



Available at https://edupediapublications.org/journals

p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017

Analysis and Simulation of Novel Multi level Inverter Topology for Grid Interconnection of PV Systems

YADAM NAGENDRA Assistant Professor Department of Electrical & Electronics Engineering, Narsimha Reddy Engineering College Maisammguda (v) Dhulapally, R R (Dt); T S, India. NARESH BANDI Assistant Professor Department of Electrical & Electronics Engineering, Narsimha Reddy Engineering College Maisammguda (v) Dhulapally, R R (Dt); T S, India. D RAMAKRISHNAM RAJU M-tech Student Scholar Department of Electrical & Electronics Engineering, Narsimha Reddy Engineering College Maisammguda (v) Dhulapally, R R (Dt); T S, India.

Abstract — Photovoltaic energy is a wide kind of green energy, because photo voltaic solar are pollution free, easily erectable, and limitless. Photovoltaic systems are mostly used as they are light, clean and easily installable. Normally PV cells converts sunlight into electricity in the form of dc A high performance on these systems is needed to make the most of energy produced by solar cells. Also, there must be a constant adaptation due to the continuous variation of power production. : In any PV based system, the inverter is a critical component responsible for the control of electricity flow between the dc source, and loads or grid. This paper presents a solar PV generation system integrated to the grid. the comparative op eration of inverter topologies which are the conventional two level inverters and multilevel inverter topology to reduce total harmonic distortions in grid voltage and electromagnetic interference. Unique features of multi-level converters have recently nominated them as significant alternatives for solidst ate power converting units, even in the low and medium power range. The fact that multilevel converters need several DC sources in the DC side makes them attractive for photovoltaic (PV) applications. This project presents a new control strategy to control cascaded multilevel converters in a multi-string configuration for single phase grid connected system. In extension the proposed concept can be implemented for new multilevel inverter concept by using MATLAB/SIMULATION software.

Keywords – Multilevel Inverter, MATLAB, THD and RV Technique. LINTRODUCTION

Power electronics devices are widely used in different fields and for different practical applications. The expansion of their field of applications is related to the knowledge of the device behavior and of their performances. Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. As a result, multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. Power electronic converters, especially dc/ac PWM inverters have been extending their range of use in industry because they provide reduced energy consumption, better system efficiency, improved quality of product, good maintenance, and so on. The most common initial application of multilevel converters has been in traction, both in locomotives and track -side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission, and most recently for medium voltage induction motor variable speed drives. Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, flexible AC transmission system (FACTS), and traction drive systems.

The inverters in such application areas as stated above should be able to handle high voltage and large power. For this reason, two -level high-voltage and largepower inverters have been designed with series connection of switching power devices such as gate -turnoff thyristors (GTOs), integrated gate commutated transistors (IGCTs), and integrated gate bipolar transistors (IGBTs), because the series connection allows reaching much higher voltages. However, the series connection of switching power devices has big problems, namely, non equal distribution of applied device voltage across series-connected devices that may make the applied voltage of individual devices much higher than blocking voltage of the devices during transient and steady-state switching operation of devices.

As alternatives to effectively solve the above mentioned problems, several circuit topologies of multilevel inverter and converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels



increases, so the quantity of output filters can be decreased. A multilevel converter can be implemented in many different ways. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices.

In this paper, a novel cascaded H-bridge multilevel inverter has been proposed using less number of switches. A standard cascaded multilevel inverter requires 4h number of switches for (2h + 1) levels whereas h is the number of dc sources. Multilevel inverters supplied from equal and constant dc sources almost don't exist in practical applications. The variation of the dc sources affects the values of the switching angles required for each specific harmonic profile, as well as increases the difficulty of the harmonic elimination's equations. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Finally the proposed topology is implemented with SHE [7] [8]. The THD values for the Traditional, Conventional and Proposed inverters are compared and analyzed.

II. H-BRIDGE MULTILEVEL INVERTER

The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated. In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages. In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd. Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency. Consider the seven level inverter; it requires 12 IGBT switches and three dc sources. A cascaded H-bridge multilevel inverter is simply a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. The cascaded Hbridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source Vdc. By cascading the AC outputs of each H bridge inverter, an AC voltage waveform is produced.



Fig 1. Cascaded H-bridge 7-level Inverter By closing the appropriate switches, each H-bridge inverter can produce three different voltages: +Vdc, 0 and -Vdc.



Fig 2. Output Voltage of cascaded H-bridge seven level inverter

It is also possible to modularize circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. The number of switches is reduced using the new topology. This circuit is simulated using the MATLAB software. The results are shown in the later sections in detail.

III.PROPOSED TOPOLOGY



International Journal of Research

Available at https://edupediapublications.org/journals

p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017

The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics.

(a) Seven Level Proposed Multilevel Inverter: The seven level proposed inverter uses only six switches compared to cascaded H-bridge inverter which uses ten switches and three separate dc sources. But in proposed inverter, the requirement of separate dc sources is only two and the switching losses are also low. Using proper switching sequence proposed circuit generates seven levels in output voltage [7]. Table I shows the switching sequence used for creating seven levels for the output voltage.

TABLE I: SWITCHING SEQUENCE FOR PROPOSED SEVEN LEVEL INVERTER

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Load Voltage
On	On	off	off	On	ofT	V _{dc}
On	On	off	off	off	On	2V _{de}
On	On	off	on	On	On	3V _{de}
off	Ou	off	On	off	off	0
off	off	On	On	On	off	-V _{de}
off	off	On	On	off	On	-2V _{dc}
off	off	Ou	On	On	On	-3V de

The output waveform has 7 levels: \pm 3Vdc, \pm 2Vdc, \pm V_{dc} and 0. Circuit diagram of proposed seven level multilevel inverter is shown in figure 3.3.

For generating seven levels, the proposed inverter uses two cells that mean it contains two switches and two diodes in addition with the one H-bridge. The output voltage waveform of the ideal seven level inverter is shown in fig 3.



Fig 3 Proposed Power circuit for 7-level output.



Fig 4 Waveforms of the proposed seven level inverter

(b) Thirteen Level Proposed Multi level inverter: The thirteen level proposed inverter uses only seven switches compared to cascaded H-bridge inverter which uses twenty four switches and six separate dc sources. But in proposed inverter, the requirement of separate dc sources is only three and the switching losses are also low. Using proper switching sequence proposed circuit generates seven levels in output voltage. Table 11 shows the switching sequence used for creating thirteen levels for the output voltage.

TABLE 2: SWITCHING SEQUENCE FOR PROPOSED THT RTEEN LEVEL INVERTER

Inernational Journal of Research

International Journal of Research

Availableat https://edupediapublications.org/journals

p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017

Sw1	Sw2	Sw3	Sw4	Sw5	Sw6	Sw7	Vload
On	On	off	off	On	On	On	6V _{dc}
On	On	off	off	off	On	On	5V de
On	On	off	on	On	off	On	4V de
On	On	off	off	off	off	On	3V _{dc}
On	On	off	off	off	On	off	2V _{dc}
On	On	off	off	On	off	off	Vac
off	On	off	On	off	off	off	0
off	off	On	On	On	off	off	-V _{dc}
off	off	On	On	no	On	off	-2V de
off	off	On	Оп	off	off	Оц	-3V de
off	off	On	On	On	off	On	-4V de
off	off	On	On	off	On	On	-5V de
off	off	On	On	On	On	On	-6V du

Circuit diagram of proposed thirteen level multilevel inverter is shown in figure 5.



Fig.5. Circuit diagram of thirteen level proposed inverter

The output waveform has 13 levels: \pm 6Vdc, \pm 5Vdc, \pm 4Vdc \pm 3Vdc, \pm 2Vdc, \pm V_{dc} and 0. The output voltage waveform of the ideal thirteen level inverter is shown in fig.6.



Fig.6. Ideal thirteen level output voltage waveform

The following table III shows the comparison between proposed MLI and conventional multi level inverters.

Topology	Number of switches for 7-level	Number of switches for 13-level		
Diode Clamped MLI	12	24		
Flying capacitor MLI	12	24		
Cascaded II-bridge MLI	12	24		
Proposed MLI	6	7		

TABLE III: COMPARISON BETWEEN DIFFERENT TOPOLOGIES

IV. MATLAB/SIMULINK RESULTS

Here simulation is carried out in different cases in that 1). Conventional Cascaded H-Bridge Multilevel Inverter 2). Multilevel Inverter 3). Proposed Multilevel Inverter with 21 levels

Case 1: Conventional Cascaded H-Bridge Multilevel Inverter



International Journal of Research

Available at https://edupediapublications.org/journals

p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017



Fig.7 Matlab/Simulink Model of Conventional Cascaded H-Bridge Multilevel Inverter



Fig.8 Seven Level Output Voltag





Fig.9.Simulink circuit for proposed multilevel inverter



Fig.10.Simulation result for seven level output voltage



Fig.12.harmonic spectrum for seven level output voltage







Fig.12.Simulation result for 13 level output voltage





p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017

Fig.13.harmonic spectrum for seven level output voltage





Fig.15.Simulation result for 21 level output voltage

VI.CONCLUSION

This proposed model is implemented using Matlab Simulink software and the obtained resultant waveforms were evaluated and the effectiveness of the performance of multilevel inverter has been established. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. In this paper, a new inverter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. So, these new technologies of semiconductor are more suited to high power applications and they enable the design of multilevel inverters.

[1] Ayoub Kavousi, Behrooz Vahidi, Reza Salehi, Mohammad azem Bakhshizadeh, Naeem Farokhnia and S.Hamid Fathi,(April 2012) "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions on power electronics, vol. 27, no. 4, pp1689-1696.

[2] Damoun Ahmadi, KeZou, Cong Li, Yi Huang and Jin Wang, (october 2011) "A Universal Selective Harmonic Elimination Method for High Power Inverters", IEEE Transactions on power electronics, vol. 26, no. 10, pp2743-2752,.

[3] FaeteFilho, Leon M. Tolbert, Yue Cao and Burak Ozpineci, (September/October 2011) "Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation", IEEE Transactions on industry applications, vol. 47, no. 5, pp2117-2124.

[4] Hossein Sepahvand, Jingsheng Liao and Mehdi Ferdowsi, (November 2011) "Investigation on Capacitor Voltage Regulation in Cascaded HBridge Multilevel Converters With Fundamental Frequency Switching", IEEE Transactions on industrial electronics, vol. 58, no. 11, pp5102-5111.

[5] Jason R. Wells, XinGengPatrick L. Chapman Philip T. Kreinand Brett M. Nee, (January 2007) "Modulation-Based Harmonic Elimination", IEEE Transactions on power electronics, vol. 22, no. 1,pp336-340.

 [6] J. Napoles, A. J. Watson, J. J. Padilla, J. I. Leon, L. G. Franquelo, P.
W. Wheeler and M. A. Aguirre, (June 2012)"Selective Harmonic Mitigation Technique for Cascaded H-Bridge Converters with Non-Equal DC Link Voltages", IEEE Transactions on power electronics,pp1-9.

[7] John N. Chiasson, Leon M. Tolbert, Keith J. McKenzie and Zhong Du,(march 2004)"A Unified Approach to Solving the Harmonic Elimination Equations in Multilevel Converters", IEEE Transactions on power electronics, vol. 19, no. 2, pp478-500.

[8] A. Maheswari, S. Mahendran, Dr. I. Gnanambal (August 2012), "Implementation of Fundamental Frequency Switching Scheme on Multi –Level Cascaded H- Bridge Inverter Fed Three Phase Induction Motor Drive" Wulfeniajournal, Klangfurt, Austria, Vol 19, No. 8, pp10-24.

AUTHORS PROFILE



Yadam Nagendra received B.Tech degree from Obul Kandula Reddy memorial College of Engineering (JNTUA) in the year 2012 and received M.Tech in the stream of Power Electronics at St.Martin's Engineering

college (JNTUH) in the year 2014. Currently working as a Assistant Professor in Narsimha Reddy Engineering college for two years. His research interests include current power electronics for photovoltaic (PV) applications and PV generation and monitoring, include multilevel converters, power converters for distributed energy resources.

International Journal of Research



Availableat https://edupediapublications.org/journals

p-ISSN: 2348-6848 e-ISSN: 2348-795X Volume 04 Issue 02 February 2017



NARESHBANDI received B.Tech degree from ramappa Engineering college (JNTUH) in the year 2006 and received M.Tech in the stream of Power Electronics at P.indhra reddy memorial

college of Engineering (JNTUH) in the year 2013. Currently working as a Assistant Professor in Narsimha Reddy Engineering College for one year. And his areas of interest are Applications of Power Systems& Electrical maching Sctronics in "Power



Dandu Ramakrishnam Raju received B.tech from Medak College of Engineering & Technology in the year of 2011 and now pursuing M.Tech in the stream of Power Electronics at Narsimha Reddy Engineering college.