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Design and Implematation of 32-BIT MAC Unit Using Vedic Multiplier and Reversible Logic Gate

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ABSTRACT: *A Vedic multiplier is composed by utilizing Urdhava Triyagbhayam sutra and the viper outline is finished by utilizing reversible rationale door. Reversible rationales are likewise the major prerequisite for the developing field of Quantum processing. The Vedic multiplier is utilized for the increase unit in order to lessen incomplete items and to get leading and smaller range .The reversible rationale is utilized to get less power. The MAC is outlined in Verilog HDL and the reproduction is done in Modelsim, Xilinx 14.2 and blend is finished in both RTL compiler utilizing rhythm and also Xilinx. The chip outline for the proposed MAC is additionally done.*

KEYWORDS- MAC, Reversible logic, Urdhava Triyagbhayam

I. INTRODUCTION

Vedic mathematics is the ancient Indian system of mathematics which mainly deals with Vedic mathematical formulae and their application to various branches of mathematics. The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics was reconstructed from the ancient Indian scriptures (Vedas) by Sri Bharati Krishna Tirthaji (1884-1960), after his eight years of research on Vedas. According to his research, Vedic mathematics is mainly based on sixteen principles or word-formulae which are termed as Sutras. This is a very interesting field and presents some effective algorithms which can be applied to various branches of Engineering such as Computing and Digital Signal Processing. In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The major applications of Multiply-accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage.

The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. Multiplication is the fundamental operation of MAC unit. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two major criterions that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path. The second part of MAC is Reversible logic gate. In modern

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VLSI, fast switching of signals leads to more power dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy are generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc. The main idea of this paper is to obtain less power, area, speed of MAC unit using Vedic mathematics with reversible logic gate.

II. URDHAVA MULTIPLIER

In Urdhava Tiryakbhyam is a Sanskrit word which means vertically and crosswire in English. The method is a general multiplication formula applicable to all cases of multiplication. It is based on a novel concept through which all partial products are generated concurrently. Fig. Demonstrates a 4 x 4 binary multiplication using this method. The method can be generalized for any N x N bit multiplication. This type of multiplier is independent of the clock frequency of the processor because the partial products and their sums are calculated in parallel. The net advantage is that it reduces the need of microprocessors to operate at increasingly higher clock frequencies. As the operating frequency of a processor increases the number of switching instances also increases. This results more power consumption and also dissipation in the form of heat which results in higher device operating temperatures. Another advantage of Urdhava Tiryakbhyam multiplier is its scalability T.

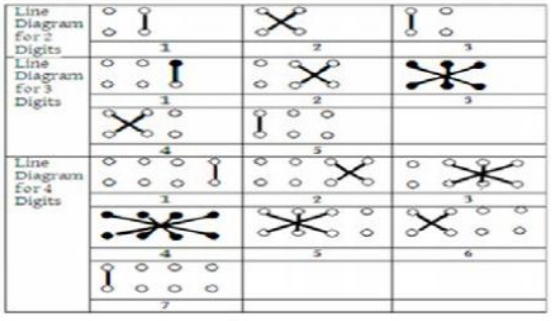


Fig. 1 Line Diagram for Urdhava Multiplication

The processing power can easily be increased by increasing the input and output data bus widths since it has a regular structure. Due to its regular structure, it can be easily layout in a silicon chip and also consumes optimum area. As the number of input bits increase, gate delay and area increase very slowly as compared to other multipliers. Therefore Urdhava Tiryakbhyam multiplier is time, space and power efficient.

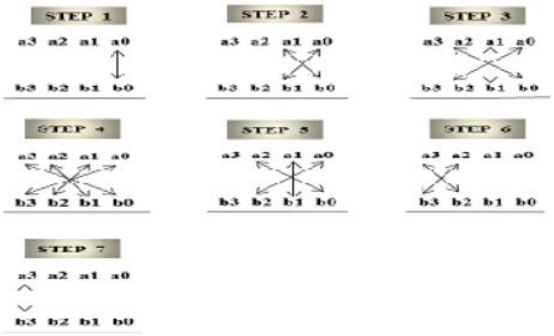
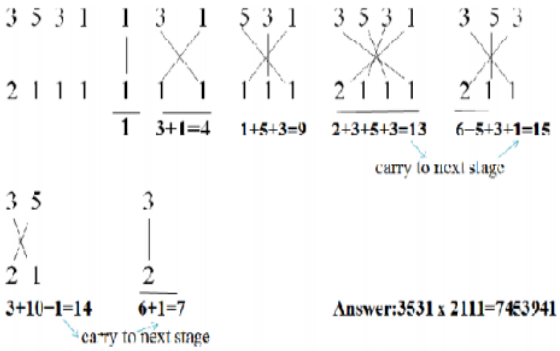


Fig. 2 Multiplication of two 4 bit Numbers using Urdhava Tiryakbhyam Method



Example 3: For the Multiplication of two 4 bit Numbers using Urdhava Tiryakbhyam Method

The line diagram in fig. 3 illustrates the algorithm for multiplying two 4-bit binary numbers a3, a2, a1, a0 and b3, b2, b1, b0. The procedure is divided into 7 steps and each step generates partial products. Initially as shown in step 1 of fig. 2, the least significant bit (LSB) of the multiplier is multiplied with least significant bit of the multiplicand (vertical multiplication). This result forms the LSB of the product. In step 2 next higher bit of the multiplier is multiplied with the LSB of the multiplicand and the LSB of the multiplier is multiplied with the next higher bit of the multiplicand (crosswire multiplication). These two partial products are added and the LSB of the sum is the next higher bit of the final product and the remaining bits are carried to the next step. For example, if in some intermediate step, we get the result as 1101, then 1 will act as the result bit (referred as rn) and 110 as the carry (referred as cn). Therefore cn may be a multi-bit number. Similarly other steps are carried out as indicated by the line diagram. The important feature is that all the partial products and their sums for every step can be calculated in parallel. Thus every step in fig. 3.1 has a corresponding expression as follows:

r0=a0b0 (1)
c1r1=a1b0+a0b1 (2)
c2r2=c1+a2b0+a1b1 + a0b2 (3)
c3r3=c2+a3b0+a2b1 + a1b2 + a0b3. (4)
c4r4=c3+a3b1+a2b2 + a1b3. (5)
c5r5=c4+a3b2+a2b3. (6)
c6r6=c5+a3b3 (7)

With c6r6r5r4r3r2r1r0 being the final product. Hence this is the general mathematical formula applicable to all cases of multiplication and its hardware architecture is shown in fig. 3. In order to multiply two 8-bit numbers using 4-bit multiplier we proceed as follows. Consider two 8 bit numbers denoted as AHAL and BHBL where AH and BH corresponds to the most significant 4 bits, AL and BL are the least significant 4 bits of an 8-bit number. When the numbers are multiplied multiplied according to Urdhava Tiryakbhyam (vertically and crosswire) method, we get,

AH AL

BH BL

_____

(AH x BH) + (AH x BL + BH x AL) + (AL x BL).

The digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry.

III. THE PROPOSED APPROACH

The design of MAC architecture consists of 3 sub designs.

- Design of 32×32 bit Vedic multiplier.
- Design of adder using DKG gate reversible logic.
- Design of accumulator which integrates both multiplier and adder stages.

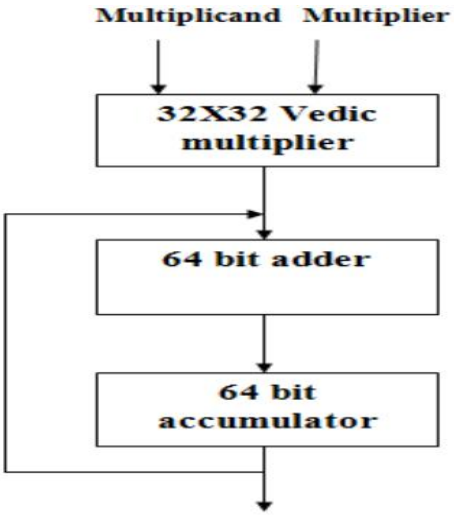


Fig. 3 Modified MAC Architecture

A. Urdhava Triyagbhayam Sutra

It literally means "Vertically and crosswise". Shift operation is not necessary because the partial product calculation will perform it in a single step, which in turn saves time and power. This is the main advantage of the Vedic multiplier Urdhva – Triyagbhayam is the general formula applicable to all cases of multiplication and also in the division of a large number by another large number. It is one of Sixteen Vedic Sutras and deals with the multiplication of numbers.

B. Kogge-Stone adder

It's a parallel prefix adder, which is the one of the fastest adder. Carry stages: log2 n; the number of cells: n (log2n-1) +1; Maximum fan-out: 2 (extra wiring). So, it will reduce the power consumption as well as the power dissipation. The Kogge-Stone adder is a parallel prefix form of carry look-ahead adder. It generates the carry signals in O (log2N) time, and is widely considered as the fastest adder design possible. It is the most common architecture for high-performance adders in industry. The following fig shows the design of a 32×32 Vedic multiplier using an 16×16 Vedic multiplier and with kogge stone adder the design can be implemented using Verilog HDL.

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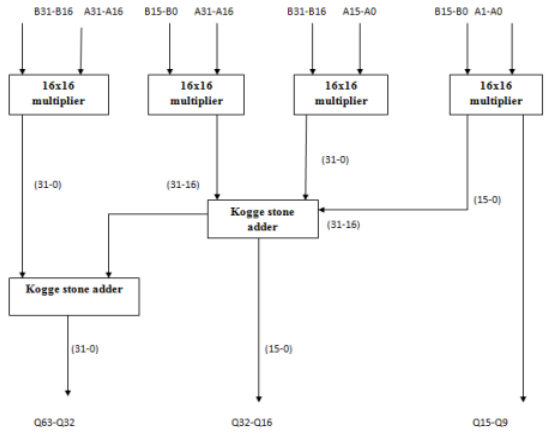

Fig.4 32x 32 MAC unit with kogge stone adder design

C. Accumulator Stage

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit.

IV. DESIGN OF ADDER USING REVERSIBLE LOGIC DKG GATE

A. Reversible logic

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

General consideration for reversible logic gate: A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

- Fan-out is not permitted
- Loops or feedbacks are not permitted
- Garbage outputs must be Minimum¾ Minimum delay
- Minimum quantum cost
- Zero energy dissipation

B. DKG Gate

A 4*4 reversible DKG gate [6] that can work singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique [5], [6].

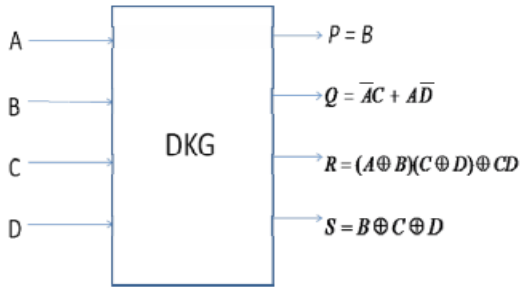

Fig. 5a [6] DKG gate

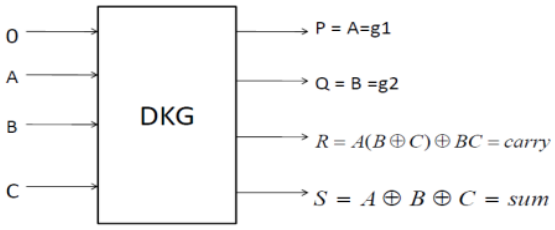

Fig. 5b DKG gate as a Full adder

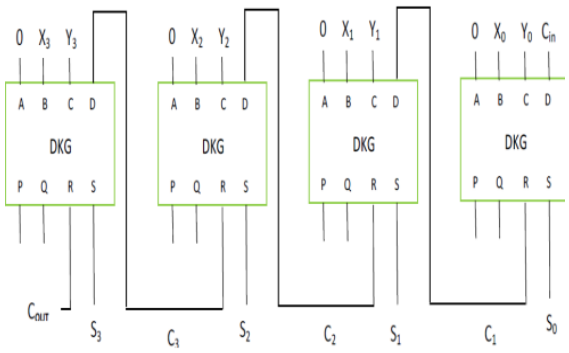

Fig. 5c Parallel adder using DKG gate

IV. RESULT AND DISCUSSION

The design of 32 bit MAC with kogge stone adder is done in Modelsim. The above design is implemented in Verilog Code using mentor graphics modelsim and Xillinx 14.4.

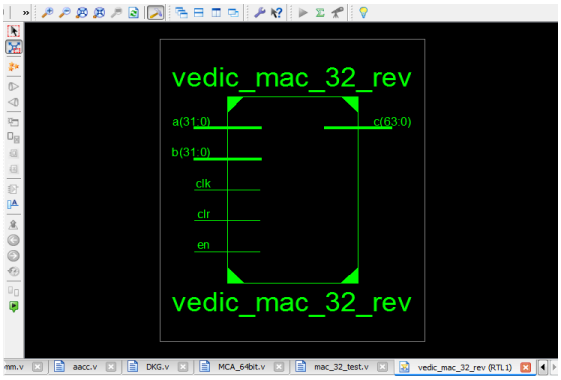

Fig. 6 Block diagram of MAC

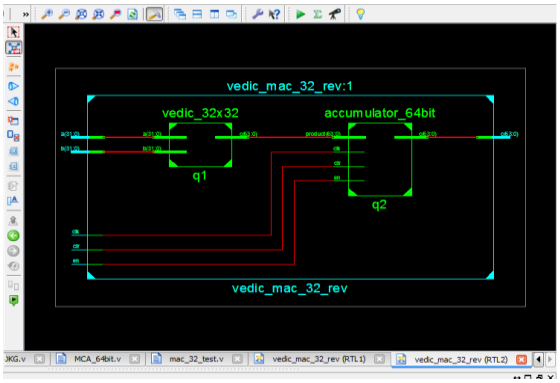

Fig. 7 RTL Schematic of 32x32 MAC unit

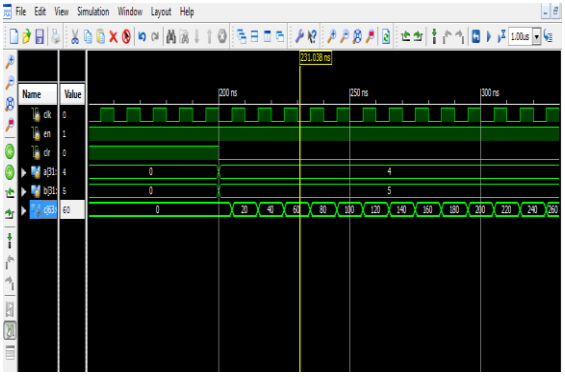

Fig. 8 Simulation output 32x32 MAC unit

V. CONCLUSION

The results obtained by the design of Vedic multiplier with 32 bits and reversible logic are quite good. The work presented is based on 32 – bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity Thus the proposed MAC provides higher performance, less area, less power dissipation for higher order bit multiplication and it also presents a highly efficient method of multiplication "Urdhva Tiryakbhyam Sutra" based on Vedic mathematics. Reversible logic gates are used to obtain the less power. It's more efficient design compare to pervious design.

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