

Dynamic Voltage Restorer (DVR) for Unbalanced and Nonlinear Loads

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Abstract— A simple generalized algorithm based on basic synchronous-reference-frame theory has been developed for the generation of instantaneous reference compensating voltages for controlling a DVR. This novel algorithm makes use of the fundamental positive-sequence phase voltages extracted by sensing only two unbalanced and/or distorted line voltages. The algorithm is general enough to handle linear as well as nonlinear loads. The compensating voltages when injected in series with a distribution feeder by three single-phase H-bridge voltage-source converters with a constant switching frequency hysteresis band voltage controller tightly regulate the voltage at the load terminals against any power quality problems on the source side. A capacitor-supported DVR does not need any active power during steady-state operation because the injected voltage is in quadrature with the feeder current. The proposed control strategy is validated through extensive simulation and real-time experimental studies.

Index Terms—Dynamic voltage restorer (DVR), hysteresis band controller, nonlinear load, voltage-source converter (VSC).

I. INTRODUCTION

POWER quality (PQ) problems in the distribution system and their solutions have received much attention in the recent years. The incorporation of the large numbers of nonlinear loads for improved efficiency and their better controlled use, the nonconventional power production technologies such as solar and wind power, and the various power electronics devices used in the system introduce new problems, like additional harmonic voltage/current distortion, particularly higher order harmonics

[1]–[5]. Under the generic name of custom power devices [2], a new group of devices is developed and used for improving the PQ in the distribution system. As per the standard such as the IEEE 519 [6], a number of custom power devices are installed and used at the consumer premises to protect the critical loads.

(VSC)-based power electronics device connected in series between the supply and the critical loads, which are to be protected from the supply-side voltage quality problems, other than outages, by injecting the required compensating voltage through DVR into the distribution line. A DVR can restore a balanced sinusoidal load voltage of desired amplitude even when the source voltage is unbalanced and/or distorted. The voltage injected by self-supported DVR is in quadrature with the feeder current; hence, it does not need any active power during steady state. However, its disadvantage is that, in case of the voltage sag/swell, the restored voltage may not be in phase with the presag/preswell voltage. The self-supported DVR is used when the phase jump, caused by the quadrature voltage injection, is affordable.

The DVR is an important controller in the custom power park [7]. The analysis, design, and voltage injection schemes of the self-supported DVR are discussed in [2], [10], and [11], and the different control strategies for the DVR have been developed in [8]–[17]. Control techniques based on synchronous reference frame (SRF) theory (SRFT) [8], Adaline-based fundamental extraction [9], instantaneous symmetrical component theory [10], [11], energy optimized control [12], PQR instantaneous power theory [13], symmetrical component estimation [14], etc., for the DVR are reported in the literature.

Different topologies of the DVR are discussed in [19]. The DVR supported by a capacitor has become popular as a cost-effective solution for the protection of sensitive loads from the supply-side voltage quality problems. Currently, most of the research is on DVR dealing with the protection of balanced linear load; however, there are a few which are related to the protection of unbalanced and nonlinear loads [17].

In modern industries, power electronics-based drives such as the current-source-inverter-fed synchronous motor drive, thyristor converter-based dc motor drive, VSC-based induction motor drive, etc., are increasingly used whose performance and control largely depend upon the supply voltage quality.

These nonlinear industrial loads give rise to additional harmonic distortion in the supply voltage at the point of common coupling (PCC) due to the harmonic voltage drop into the feeder impedance, particularly when the feeder impedance is large.

In this paper, a simple generalized control algorithm for the self-supported DVR is developed based on the basic SRFT. This novel algorithm makes use of the fundamental positive-sequence phase voltages extracted by sensing only two unbalanced and/or distorted line voltages. The algorithm is general enough to handle linear as well as nonlinear loads. The self-supported DVR maintains balanced sinusoidal load voltage with desired magnitude against any supply voltage quality problem even when the load is unbalanced and nonlinear in nature.

The algorithm based on instantaneous symmetrical components along with the complex Fourier transform to protect unbalanced and nonlinear load discussed in [17] is computationally demanding and requires huge memory space. The approach discussed here is comparatively simple as it needs only the extraction of the fundamental positive-sequence phase terminal voltages, thus making it computationally simpler with the least memory requirement. The proposed fundamental positive-sequence extractor requires the sensing of only two line voltages of supply. This reduces the analog-to-digital converter (ADC) requirements of a digital controller and corresponding sensing element. Moreover, it is able to extract three fundamental positive-sequence phase voltages irrespective of the distribution system configuration such as three-phase, four-wire or three-phase, three-wire system where the neutral is not available for sensing phase voltages.

In this paper, a hybrid structure of the self-supported DVR is considered in which a shunt capacitor filter is used to provide the low impedance path for higher order harmonics of the load currents [17]. The DVR is realized by three single-phase H-bridge VSCs with a constant switching frequency hysteresis band voltage controller [18].

The proposed control algorithm is validated through extensive simulation and real-time experimental studies performed using an OPAL-RT real-time digital simulator and a dSPACE DS1103 digital signal processor.

II. DVR CONTROL STRATEGY

The main aim of the DVR is to inject a required amount of compensating voltage in series with the supply to regulate the load terminal voltage. In this section, the proposed control algorithm is discussed with an ideal DVR model. The schematic diagram of DVR (ideal voltage sources) connected distribution feeder is shown in Fig. 1. A three-phase supply is represented by the star-connected three single-phase voltage sources (V_{sa}, V_{sb}, V_{sc}) along with their series source impedances (Z_a, Z_b, Z_c). To regulate the load voltages (V_{La}, V_{Lb}, V_{Lc}) to be balanced and sinusoidal against various PQ problems in the terminal voltages (V_{ta}, V_{tb}, V_{tc}), DVR injects the required compensating voltages (V_{Ca}, V_{Cb}, V_{Cc}) in each phase.

The practical implementation of a DVR using three single-phase H-bridge VSCs along with a common dc capacitor is

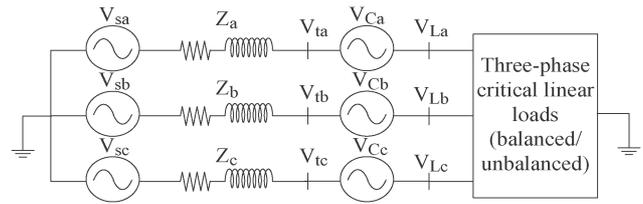


Fig. 1. Schematic diagram of DVR (ideal voltage sources) connected power system.

discussed later. The energy storage device is a capacitor, so the following condition is stipulated on the DVR.

- The DVR should not supply any real power in steady state. This implies that, in steady state, the phase difference between instantaneous DVR voltages and instantaneous line currents must be 90° .

A. DVR Operation Under Balanced Sinusoidal Supply Condition with Balanced Linear Load

In this section, the algorithm is developed to compute instantaneous DVR voltages from the samples of instantaneous terminal voltages and line currents assuming balanced sinusoidal supply and balanced load. The schematic diagram of the DVR-connected power system is shown in Fig. 1.

From Fig. 1,

$$v_{tk} + v_{ck} = v_{Lk}^*; \quad k = a, b, c \quad (1)$$

where v_{tk} , v_{ck} , and v_{Lk}^* are the instantaneous terminal voltages, instantaneous DVR voltages, and instantaneous reference load voltages, respectively. Moreover, k is the phase of the supply.

Taking the line current as the reference frame, the above equation can be converted to SRF as

$$v_{td} + jv_{tq} + jv_{cq} = v_{Ld}^* + jv_{Lq}^*. \quad (2)$$

Note that, for zero DVR active power in steady state, V_C should be at 90° to the line current, so in (2), v_{ck} contributes to the quadrature component v_{cq} only and the terminal voltages are balanced and sinusoidal; therefore, there is no zero-sequence component (v_{t0}) present in (2).

In (2), v_{td} can be computed from the instantaneous samples of terminal voltages as

$$v_{td} = v_{ta} \sin \theta + v_{tb} \sin \left(\theta - \frac{2\pi}{3} \right) + v_{tc} \sin \left(\theta + \frac{2\pi}{3} \right). \quad (3)$$

As terminal voltages are balanced and sinusoidal, v_{td} contains only the constant dc component, and from (2)

$$v_{Ld}^* = v_{td}. \quad (4)$$

Moreover, to regulate the peak of the load voltage (ph-n) to v_{Lp} , v_{Lq}^* can be directly calculated as

$$\begin{aligned} v_{Lq}^* &= \sqrt{v_{Lp}^2 - v_{Ld}^{*2}} \\ &= \sqrt{v_{Lp}^2 - v_{td}^2}. \end{aligned} \quad (5)$$

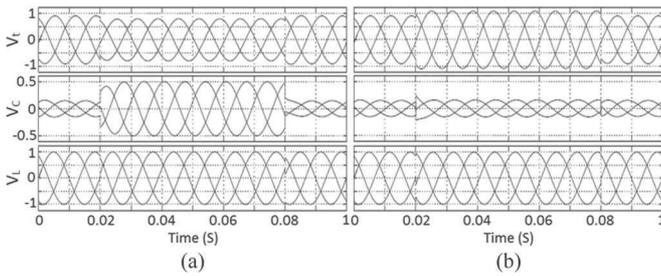


Fig. 2. DVR response for balanced sag and swell.

After computing v_{Ld}^* and v_{Lq}^* , the instantaneous reference load voltages can be computed as follows:

$$\begin{bmatrix} v_{La}^* \\ v_{Lb}^* \\ v_{Lc}^* \end{bmatrix} = \begin{bmatrix} \sin \theta & \cos \theta \\ \sin \left(\theta - \frac{2\pi}{3} \right) & \cos \left(\theta - \frac{2\pi}{3} \right) \\ \sin \left(\theta + \frac{2\pi}{3} \right) & \cos \left(\theta + \frac{2\pi}{3} \right) \end{bmatrix} \begin{bmatrix} v_{Ld}^* \\ v_{Lq}^* \end{bmatrix}. \quad (6)$$

As the load is a balanced linear load, $\sin \theta$ and $\cos \theta$ used in (3) and (6) can be computed directly using instantaneous samples of load currents as

$$\sin \theta = \frac{i_{La}}{i_{Lmag}} \quad (7)$$

$$\cos \theta = -\frac{1}{\sqrt{3}} \left(\frac{i_{La} + 2i_{Lb}}{i_{Lmag}} \right) \quad (8)$$

where

$$i_{Lmag} = \sqrt{\frac{2}{3} (i_{La}^2 + i_{Lb}^2 + i_{Lc}^2)}. \quad (9)$$

From the calculated instantaneous reference load voltages using (6) and the samples of instantaneous terminal voltages, the instantaneous DVR voltages can be computed as per (1).

The response of the DVR-connected balanced sinusoidal power system to compensate balanced sag and swell is discussed in Case 1 to validate the control algorithm just shown.

Case 1: Let the amplitude of the supply voltage (ph-n), feeder impedance, and load impedance be respectively 1 p.u., $0.05+j0.3$ p.u., and $2+j1.5$ p.u. with 50-Hz frequency. Moreover, it is required to regulate the amplitude of the load voltage to 1 p.u.

The DVR-connected power system response with the algorithm discussed earlier during balanced voltage sag is shown in Fig. 2(a). The terminal voltages (V_t), DVR voltages (V_C), and load voltages (V_L) are shown in Fig. 2(a) from top to bottom. It can be seen that the amplitude of the load voltages becomes equal to 1.0 p.u. as DVR is pressed into action at 0.0 s. Then, the balanced sag of 0.2 p.u. is introduced at 0.02 s, and it occurs for four cycles of ac mains as shown in Fig. 2(a). It can be seen that the amplitude of the load voltage is regulated to 1.0 p.u. by injecting a voltage V_C through DVR.

The DVR-connected power system response with 0.2 p.u. balance swell is shown in Fig. 2(b). In this case also, it can be seen that the amplitude of the load voltage is regulated to 1.0 p.u.

The results shown in Case 1 validate the control algorithm to control DVR when the supply is balanced. However, one of

B. DVR Operation Under Unbalanced and/or Distorted Supply Condition With Unbalanced Linear Load

The algorithm discussed in the previous section will fail to compute the desired reference load voltages under the situation, where the unbalanced and/or distorted supply voltages feed the unbalanced load. There are two reasons for this: First, the load currents are not balanced, so $\sin \theta$ and $\cos \theta$ cannot be calculated from (7)–(9) directly, and second, v_{td} calculated from (3) does not only contain a constant component but also contains a varying component because terminal voltages are not balanced.

For the algorithm to work under such situation, the following conditions should be satisfied: 1) $\sin \theta$ and $\cos \theta$ used in (6) should be sinusoidal in shape with their phase locked to fundamental positive-sequence load currents; this can be achieved using a phase-locked loop (PLL) over the load currents, and 2) fundamental positive-sequence components of terminal voltages should be used in the calculation of v_{td} instead of samples of unbalanced and/or distorted terminal voltages.

The unbalanced and/or distorted terminal voltages can be written as

$$v_{tk} = v_{tk1_f} + v_{tk_rest}; \quad k = a, b, c \quad (10)$$

where v_{tk1_f} is the positive-sequence component of v_{tk} and v_{tk_rest} is the remaining portion containing the influence of unbalance and harmonics. The modification is thus to replace v_{ta} , v_{tb} , and v_{tc} in (3) by v_{ta1_f} , v_{tb1_f} , and v_{tc1_f} , respectively

$$v_{td} = v_{ta1_f} \sin \theta + v_{tb1_f} \sin \left(\theta - \frac{2\pi}{3} \right) + v_{tc1_f} \sin \left(\theta + \frac{2\pi}{3} \right). \quad (11)$$

To extract the fundamental positive-sequence terminal phase voltages, a novel fundamental positive-sequence extractor is proposed which requires the sensing of only two distorted and/or unbalanced terminal line voltages.

C. Fundamental Positive-Sequence Extractor

As the line voltages are the difference of different phase voltages ($v_a - v_b$, $v_b - v_c$, and $v_c - v_a$), the summation of three line voltages is always zero irrespective of whether three phase voltages are balanced and sinusoidal or unbalanced. Therefore, by sensing only two line voltages v_{ab} and v_{bc} , the third line voltage v_{ca} can be calculated as

$$v_{ca} = -(v_{ab} + v_{bc}). \quad (12)$$

If Park's transformation is applied to three balanced sinusoidal line voltages v_{ab} , v_{bc} , and v_{ca} using a PLL over the same line voltages, then it gives constant direct-axis component v_d equal to the amplitude of line voltage, quadrature-axis component v_q equal to zero, and zero-sequence component v_0 equal to zero because line voltages are a positive sequence only without

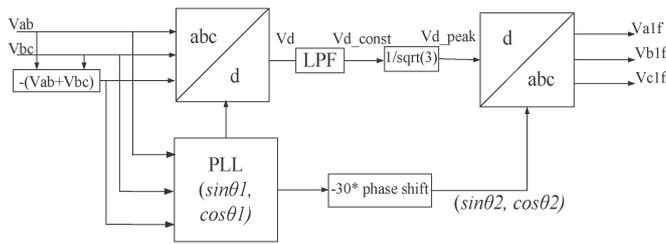


Fig. 3. Block diagram of fundamental positive-sequence extractor.

any harmonics. When line voltages are unbalanced and/or distorted, then, v_d is composed of two parts: a constant component equal to the amplitude of positive-sequence line voltage and a varying component influenced by negative-sequence line voltage and harmonics. While v_q and v_0 are not of interest because, here, the aim is to extract fundamental positive-sequence line voltages and both v_q and v_0 do not contain any information about positive-sequence line voltages, note that v_0 is always zero when Park's transformation is applied to the line voltages.

The direct-axis component $v_d = v_{d_const} + v_{d_var}$ can be calculated using samples of line voltages with PLL over the same line voltages as

$$v_d = v_{ab} \sin \theta_1 + v_{bc} \sin \left(\theta_1 - \frac{2\pi}{3} \right) + v_{ca} \sin \left(\theta_1 - \frac{2\pi}{3} \right). \quad (13)$$

The amplitude of the fundamental positive-sequence line voltage v_{d_const} is then extracted by passing v_d through a low-pass filter (LPF) or moving average filter; LPF is advantageous when distorted line voltages contain interharmonics. After extracting v_{d_const} , the amplitude of the fundamental positive-sequence phase voltage v_{d_peak} can be calculated as

$$v_{d_peak} = \frac{v_{d_const}}{\sqrt{3}}. \quad (14)$$

The three fundamental positive-sequence phase voltages are then computed after shifting $\sin \theta_1$ and $\cos \theta_1$ by -30° as

$$\begin{bmatrix} v_{a1f} \\ v_{b1f} \\ v_{c1f} \end{bmatrix} = v_{d_peak} \begin{bmatrix} \sin \theta_2 \\ \sin \left(\theta_2 - \frac{2\pi}{3} \right) \\ \sin \left(\theta_2 + \frac{2\pi}{3} \right) \end{bmatrix}. \quad (15)$$

The block diagram of the fundamental positive-sequence extractor is shown in Fig. 3.

Case 2: In this case, unbalanced supply voltages with magnitudes of 1.15, 1, and 0.85 p.u. in phases a, b, and c, respectively, are considered in which the fifth and seventh harmonics have also been added with their amplitude being inversely proportional to their harmonic number. The load impedances in each phase are $2+j1.5$ p.u., $2.5+j2$ p.u., and $1+j2.5$ p.u., respectively, and the other parameters are the same as that in Case 1. The DVR-connected power system response with the proposed fundamental positive-sequence extractor and modifications in the algorithm as discussed earlier is shown in Fig. 4.

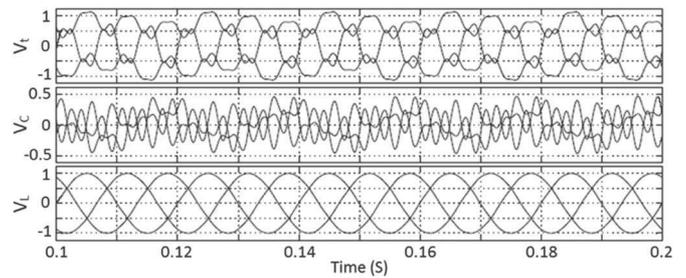


Fig. 4. DVR response for unbalanced and distorted supply with unbalanced load.

III. DVR POWER CIRCUIT

In this section, the power circuit of DVR is discussed. Practically, the DVR is realized by three single-phase H-bridge VSCs along with a common dc capacitor (C_{dc}) as shown in Fig. 5.

The three H-bridge VSCs are connected to each phase of the distribution feeder through the improved structure ripple filter (L_r, C_r, R_r) and an injection transformer. The injection transformer not only reduces the voltage requirement of the converter but also provides isolation between the converter and the distribution feeder. The shunt capacitor filter C_f is used to provide a low impedance path to higher order harmonics of load currents when the load current is nonlinear. The operation of practical DVR with nonlinear load current is discussed in the next section.

To track the reference compensating voltages, an improved filter structure constant switching frequency hysteresis band controller [18] is used in this work. The main advantages of the band controller are unconditional stability, faster response and easy implementation compared to other controllers like carrier-based controllers, dead-beat control [17], state feedback control, combined feedforward and feedback control, etc., which are based on complex mathematical computations and need much information about system parameters. Despite these advantages, the main disadvantage of the band controller compared to carrier-based controllers is variable switching frequency which may cause stress in the switches of the VSC, resulting in the deterioration of its life. The band controller has other drawbacks also like poor controllability, heavy filter currents, parabolic band voltage response, and frequent band violations due to the use of a conventional LC filter which has a second-order characteristic equation.

The constant switching frequency hysteresis band controller with improved filter structure discussed in [18] preserves all the advantages of the band controller and also overcomes its drawbacks by improved filter structure and adaptive hysteresis band which gives constant switching frequency.

The single-phase equivalent circuit of the DVR-connected system in Fig. 5 is shown in Fig. 6 to explain the basic principle of the hysteresis band controller. The reference compensating voltage for the DVR is calculated using the proposed algorithm. To inject this voltage in series with the distribution feeder, appropriate switching pulses for VSC are generated using the

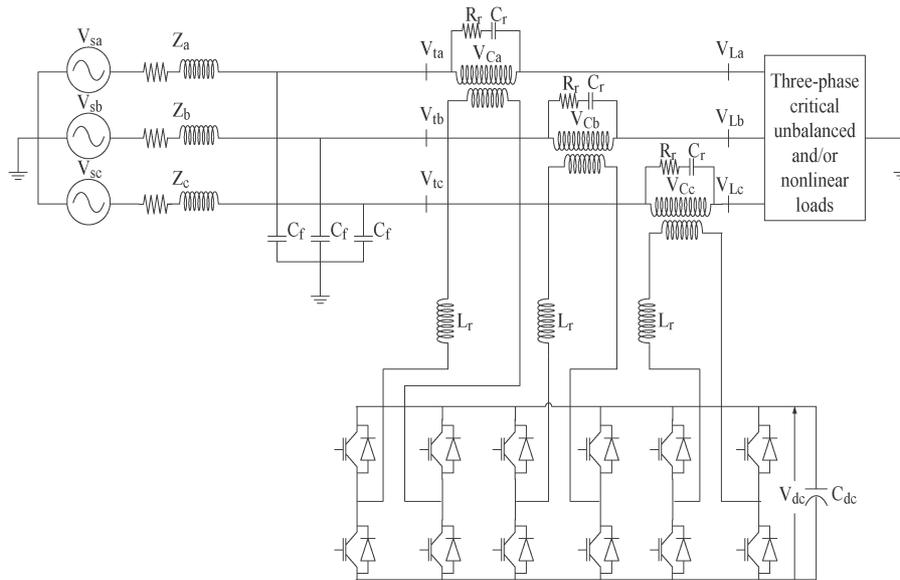


Fig. 5. DVR power circuit.

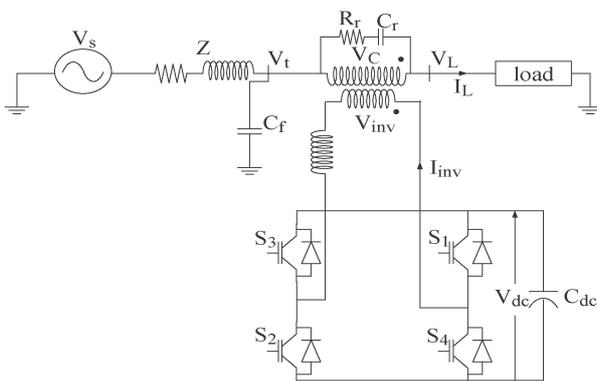


Fig. 6. Single-phase equivalent circuit of DVR-connected system.

TABLE I
SWITCHING LOGIC OF VSC WITH HYSTERESIS BAND CONTROLLER

I_f	S_1	S_2	S_3	S_4
$V_C < v_C^{ref} - h$	on	on	off	off
$V_C > v_C^{ref} + h$	off	off	on	on

hysteresis band controller with hysteresis band h . The VSC output voltage is made to track the reference voltages within upper and lower boundaries $v_C^{ref} + h$ and $v_C^{ref} - h$, respectively. When the DVR voltage V_C goes below the lower boundary, the positive dc voltage is applied across the ac filter combination (C_r, R_r) by turning switches S_1 and S_2 on. If DVR voltage V_C goes above the upper boundary, the negative dc voltage is applied by turning switches S_3 and S_4 on. The switching logic thus can be stated as given in Table I.

In order to improve the performance of the controller, an extra resistance R_r is connected in series with ac filter capacitor C_r as shown in Fig. 6. This resistance dominates the capacitive reactance at switching frequency. At switching frequency, the resistance R_r and combined inductive reactance of the L_r and transformer are very large compared to the capacitive reactance of C_r . Thus, at switching frequency, this improved structure filter circuit behaves as an $R-L$ circuit and gives a linear volt-

age variation within the band compared to the parabolic voltage variation given by the conventional $L-C$ filter circuit. Because of the linear response, this filter has less band violations and, hence, better controllability compared to the conventional filter. Details of the design of filter components can be found in [18].

To make the switching frequency constant, the hysteresis band is made variable, and its value can be calculated as given in [18]

$$h = \frac{R_f}{4v_{dc}f_{sw}L_{total}} (v_{dc}^2 - v_C^{ref}) = K (v_{dc}^2 - v_C^{ref}) \quad (16)$$

where

$$K = \frac{R_f}{4v_{dc}f_{sw}L_{total}} \quad (17)$$

For given switching frequency f_{sw} , dc voltage v_{dc} , total filter inductance (transformer inductance plus L_r), and filter resistor R_r , the value of K is a constant; hence, the variation of the band depends on the reference voltage.

In addition to the hysteresis band controller, an additional controller is required to correct the voltage in the dc-storage capacitor against the losses in the inverter and transformer, which may cause the capacitor voltage to fall. To correct these deviations, a small value of voltage in phase to the current must be injected by the DVR. To accomplish this, a simple discrete PI controller is introduced of the form

$$v_{loss}(n) = v_{loss}(n-1) + K_p \{e(n) - e(n-1)\} + K_i e(n) \quad (18)$$

where $e(n) = v_{dc}^{ref} - v_{dc}^f(n)$ and $v_{dc}^f(n)$ is the sensed instantaneous voltage across the capacitor passed through LPF. Now, (4) and (5) can be modified such that

$$v_{Ld}^* = v_{td} - v_{loss} \quad (19)$$

$$v_{Lq}^* = \sqrt{v_{Lp}^2 - (v_{td} - v_{loss})^2} \quad (20)$$

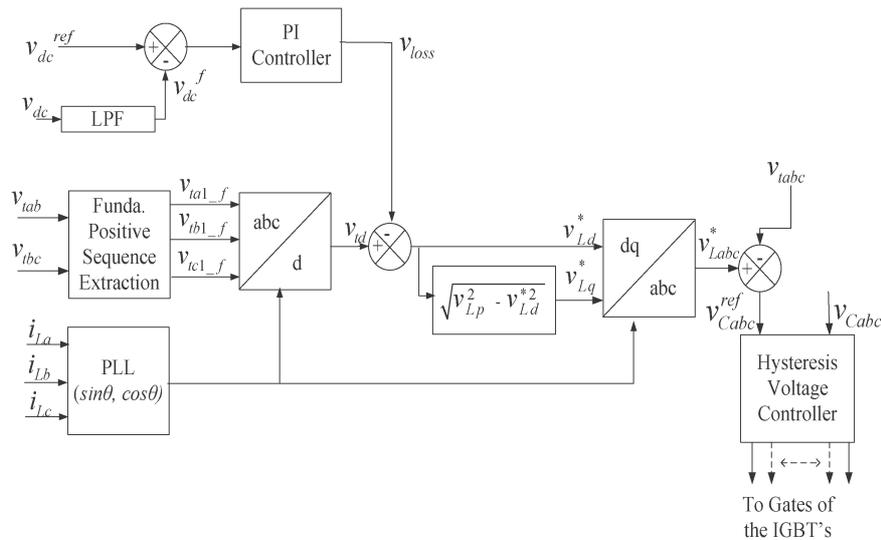


Fig. 7. Complete block diagram of proposed control algorithm.

The complete block diagram of the proposed control algorithm with all modifications is shown in Fig. 7.

IV. HYBRID STRUCTURE OF DVR

In the discussion so far, the case of nonlinear load has not been addressed. In this section, the operation of practical DVR with nonlinear load is discussed. First, it is illustrated that, when the load is nonlinear, then, only DVR without any shunt capacitor filter cannot work satisfactorily. To get satisfactory performance, a low impedance path must be provided to higher order harmonics of nonlinear load currents, which is accomplished by connecting a shunt capacitor filter at PCC as shown in Fig. 5. This combined structure of DVR with the shunt capacitor filter can be stated as the hybrid structure of DVR [17].

Case 3: In this case, highly inductive $R-L$ load supplied by a thyristor converter, which is the current source type of harmonic load, is considered with $R = 50 \Omega$, $L = 1 \text{ H}$, and firing angle $= 35^\circ$. The DVR test system as shown in Fig. 5 is simulated in MATLAB without a shunt filter capacitor C_f . The data of the simulated test system are given in the Appendix. The reference compensating voltage is computed and tracked by the proposed algorithm with a dc voltage control loop included as shown in Fig. 7.

The response of the test system is shown in Fig. 8. It can be seen that the terminal voltages (V_t) and the load voltages (V_L) contain high frequency harmonics and spikes due to discontinuous changes in load currents. Note that the reference dc voltage is set to 300 V, and it can be seen that the DVR is not capable of maintaining the dc voltage to the reference value.

These spikes in V_t and V_L are unacceptable, and to remove these spikes, a low impedance path must be provided to pass high frequency harmonic load currents. To accomplish this, a shunt capacitor filter (C_f) is connected at PCC as shown in Fig. 5 [17]. The single-phase equivalent circuit is shown in Fig. 6. Note that the voltage across the shunt capacitor filter (C_f) is the terminal voltage (V_t). Moreover, note that, after the

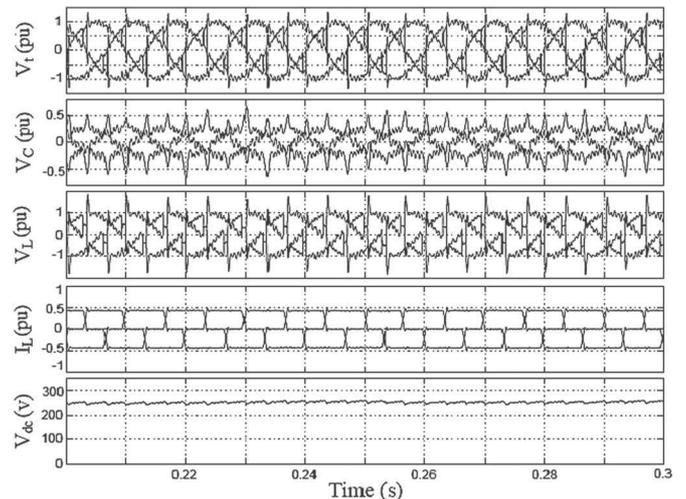


Fig. 8. Response of DVR without shunt capacitor filter for thyristor converter load.

connection of a shunt capacitor filter (C_f), load current (I_L) and source current (I_s) are not the same as shown in Fig. 8.

The judicious choice of C_f is very important. A large value of C_f gives better filtering but unacceptable magnitudes of terminal voltages and source currents, while a low value of C_f gives acceptable magnitudes of terminal voltages and source currents but inadequate filtering. Thus, in the selection of C_f or X_{Cf} , there is compromise between good filtering and acceptable magnitudes of terminal voltages and source currents. After trying different values for X_{Cf} , $X_{Cf} = 3 \text{ p.u.}$ is found to be a good compromise between good filtering and acceptable magnitudes of terminal voltages and source currents.

The response of the test system with $X_{Cf} = 3 \text{ p.u.}$ is shown in Fig. 9. It can be seen that the amplitude of the source current and the terminal voltage is comparable to that of the load current and load voltage, respectively. It can also be seen that the dc voltage is perfectly maintained at its reference value of 300 V. In all further studies, this value of X_{Cf} is considered.

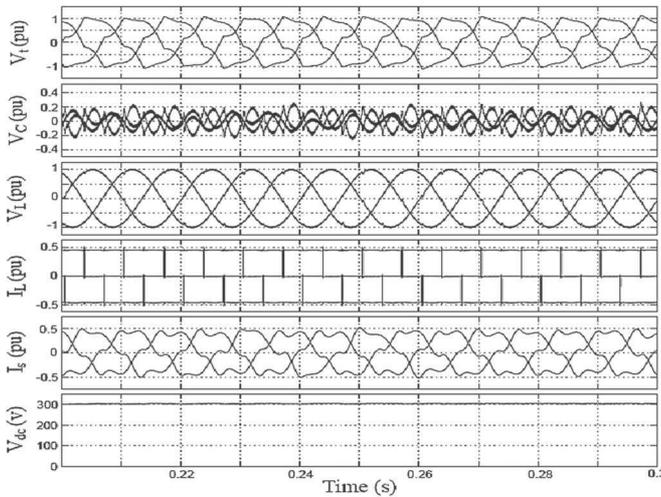


Fig. 9. Response of DVR with shunt capacitor filter for thyristor converter load.

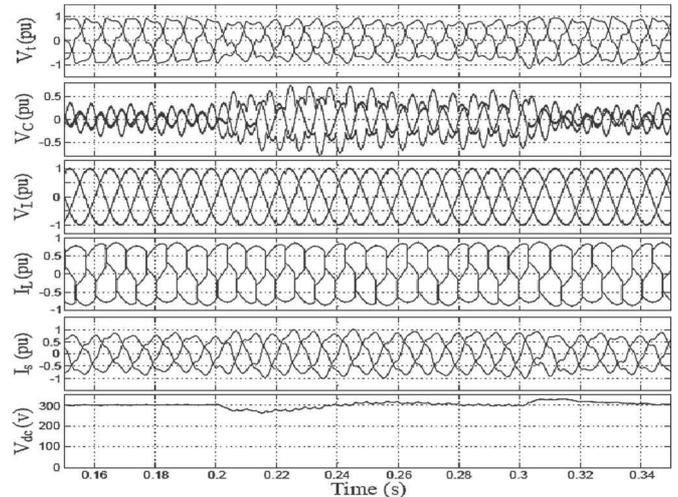


Fig. 11. Response of DVR during voltage sag.

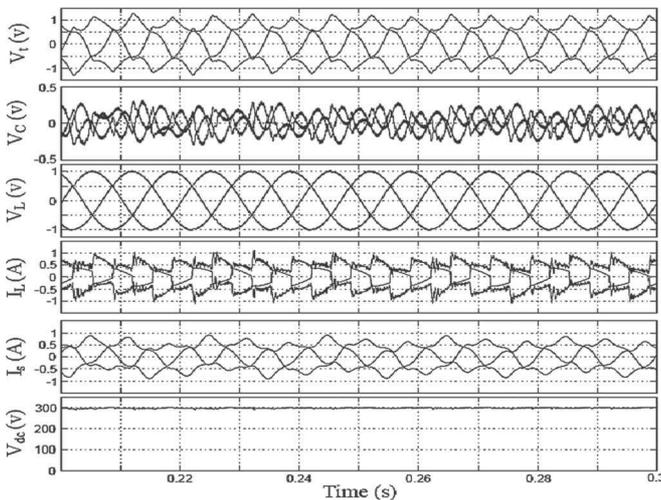


Fig. 10. Response of DVR for combined unbalanced and diode rectifier load.

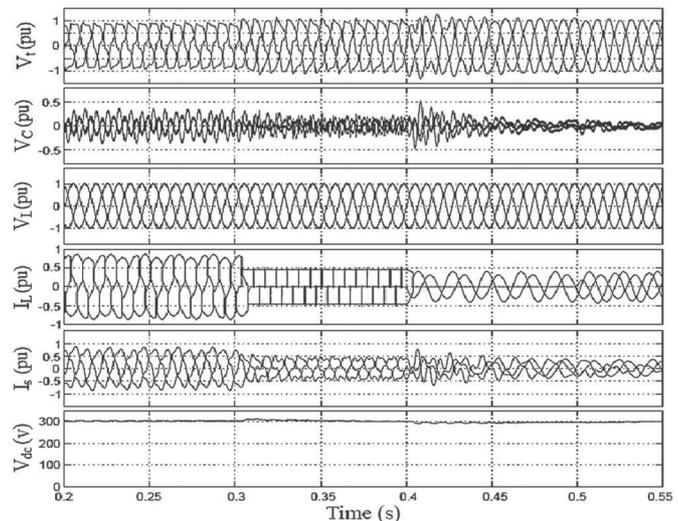


Fig. 12. Response of DVR during load variations.

V. PERFORMANCE EVALUATION

In the previous section, the performance of practical hybrid structure DVR with a thyristor converter load has been illustrated. In this section, DVR performance under different disturbances is evaluated with the same system parameters considered in Case 3.

A. Performance With Harmonic Voltage Source Type of Load

To evaluate the performance of the DVR with harmonic voltage source type of load, a combined diode rectifier load with a capacitive filter ($R = 85 \Omega$ and $C = 50 \mu\text{F}$) and unbalanced load same as Case 2 is considered. The system response is shown in Fig. 10. It can be seen that the performance of DVR is satisfactory in this case too.

B. Performance During Voltage Sag

To evaluate the performance of DVR during voltage sag, combined unbalanced and thyristor converter load same as Cases 2 and 3 is considered.

With the system operating in the steady state, a five-cycle sag of 0.15 p.u. occurs in all the phases of supply voltage at 0.2 s. The sag is cleared after five cycles at 0.3 s. The system response is shown in Fig. 11. It can be seen that, during the voltage sag, V_{dc} reduces slightly at the beginning of the sag due to transient power given to the load. However, it returns to its nominal value within one cycle of ac mains. Then, again at the time of voltage sag clearance, V_{dc} increases slightly and returns to its nominal value within one cycle of ac mains. Moreover, the voltage sag and the dc link voltage variations have no impact on the load voltages as they are maintained during the entire period.

C. Performance During Load Variations

With the system operating in steady state with unbalanced and thyristor converter load, suddenly, at 0.3 s, the unbalanced linear load is switched off. Then, at 0.4 s, suddenly, the thyristor converter load is switched off, and the unbalanced linear load in only phases a and b is applied. Then, at 0.5 s, the load in the c phase is also applied. The system response is shown in Fig. 12.

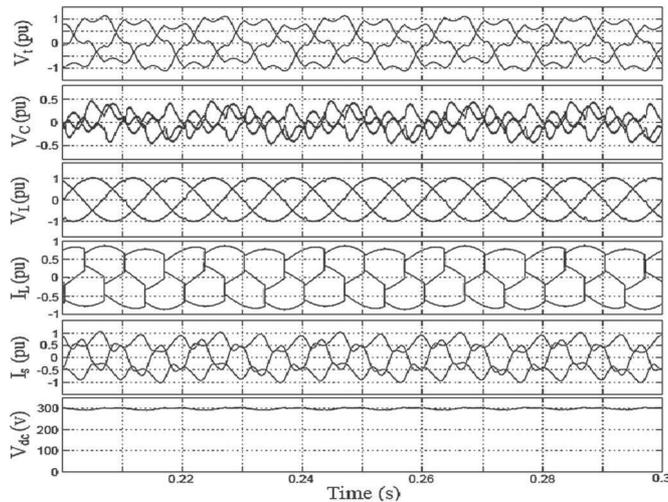


Fig. 13. Response of DVR with unbalanced and distorted supply.

It can be seen that there is no significant impact on system performance even though the load changes are significant.

D. Performance During Unbalanced and Distorted Supply

To evaluate the performance of DVR under unbalanced and distorted supply condition, the supply voltages same as Case 2 are considered with combined unbalanced and thyristor converter load.

The system response is shown in Fig. 13. It can be seen that, even under significant unbalanced and distorted supply conditions, load voltages are balanced and sinusoidal with desired magnitude. The harmonic spectra of phase-c terminal voltage and the load voltage are shown in Fig. 14(a) and (b), respectively. It can be seen that the terminal voltage is significantly distorted with a total harmonic distortion (THD) of 22.62%, but the load voltage has a THD of only 2.97% which is well below the acceptable limit, as per the IEEE Standard 519.

VI. REAL-TIME HIL IMPLEMENTATION

A real-time hardware-in-the-loop (HIL) system is built to validate the feasibility of the proposed algorithm to control DVR. The schematic of the developed laboratory experimental setup is shown in Fig. 15. The real-time HIL system is composed of an OPAL-RT real-time digital simulator and a rapid prototyping digital-signal-processing board from dSPACE, DS1103. The OPAL-RT is a real-time simulation platform with two Intel Xeon QuadCore 2.40-GHz processors working under RT-LAB software environment. OPAL-RT has 16 analog inputs, 16 analog outputs, 32 digital inputs, and 32 digital outputs, while the DS1103 has 20 ADC ports, 8 digital-to-analog converter (DAC) ports, and 32 digital inputs/outputs. As shown in Fig. 15, all the power circuit components such as the three-phase unbalanced distorted source, unbalanced nonlinear load, and DVR are implemented in the OPAL-RT. On the other hand, the digital controller for the DVR is implemented in the DS1103. In a real DVR system, the digital controller will remain the same, whereas the OPAL-RT will

be replaced by the actual power source, load, and inverter with the transformer. The necessary ten signals (three supply voltages, three DVR voltages, three load currents, and the dc bus voltage) are measured and taken out of OPAL-RT through its DAC ports. These real-time signals are given to the ADC ports of DS1103 and are utilized to generate reference DVR voltages (V_C^{ref}) using the proposed control algorithm. These reference DVR voltages are then compared with the actual DVR voltages using a constant switching frequency hysteresis band controller to generate switching pulses of the VSCs. Finally, these switching/gate pulses are transferred to OPAL-RT using digital input-output (I/O) ports and utilized to control the DVR in real time. It should be noted that all the signals are normalized on a 5-V scale ($5\text{ V} = 1\text{ p.u.}$) as the maximum limit on the I/O signals is $\pm 16\text{ V}$ for OPAL-RT and $\pm 10\text{ V}$ for dSPACE. Also, note that the sampling times for both OPAL-RT and DS1103 systems were $20\ \mu\text{s}$ each.

The performance of the proposed control algorithm for DVR with combined unbalanced and thyristor converter load has been verified under the following different conditions:

- 1) steady-state voltage compensation;
- 2) dynamic sag compensation;
- 3) compensation during load change;
- 4) unbalanced and distorted voltage compensation.

The performance of the DVR for steady-state voltage compensation is depicted in Fig. 16(a)–(d). It is worthy to note that the system parameters identical to simulation studies are considered for the experimental validation. The three-phase steady-state terminal voltages are given in Fig. 16(a). The DVR injects the required compensating voltages [see Fig. 16(b)] computed using the proposed algorithm to achieve the desired load voltages depicted in Fig. 16(c). The dc link voltage measured across the dc link capacitor is also shown in Fig. 16(c), and it can be seen that the dc link voltage is maintained constant at its reference value by DVR control. The unbalanced nonlinear load currents measured during this study are given in Fig. 16(d).

The performance of the DVR-connected system during dynamic sag condition is depicted in Fig. 16(e). Initially, the system is in steady-state condition. Suddenly, a voltage sag of 0.2 p.u. for five cycles of ac mains is introduced at PCC. The *phase-a* terminal voltage, the injected voltage by DVR, the load voltage, and the dc link voltage during this dynamic sag condition are shown in Fig. 16(e). It can be seen that the DVR controlled through the proposed algorithm effectively compensates the sag and maintains the desired load voltage at the load terminal. The dc link voltage experiences a change at the starting and ending of the sag condition, but the dc link voltage controller is effective in bringing the dc link voltage back to its reference value within two cycles.

The performance of the DVR-connected system during load change condition is shown in Fig. 16(f). Initially, the load on the system is linear unbalanced and nonlinear loads (thyristor converter load). Suddenly, the unbalanced linear load is switched off to create dynamic load change condition. It can be seen that, during the load change condition, DVR effectively regulates the load voltage to the desired value.

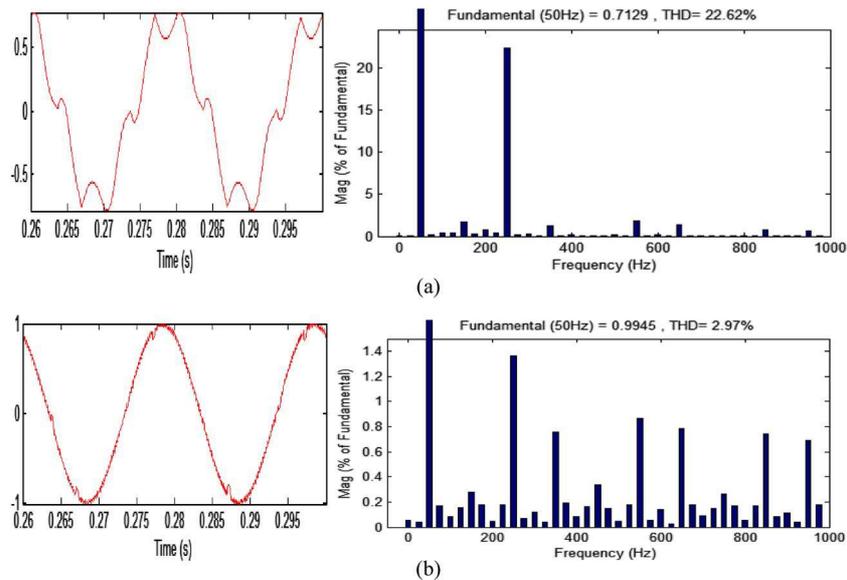


Fig. 14. (a) Phase-c terminal voltage harmonic spectrum. (b) Phase-c load voltage harmonic spectrum.

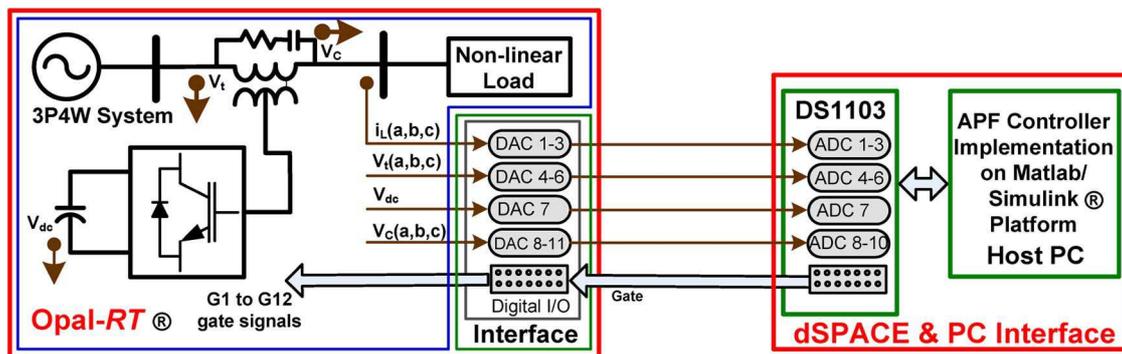


Fig. 15. Laboratory real-time HIL system.

The robustness of the DVR to compensate unbalanced and distorted supply voltages using the proposed algorithm is shown in Fig. 16(g)–(i). The unbalanced and distorted voltages considered here are similar to that of the simulation study, and they are depicted in Fig. 16(g). The injected voltages by DVR to compensate these unbalanced and distorted voltages are given in Fig. 16(h), while the achieved load voltages along with dc link voltage are given in Fig. 16(i).

The detailed experimental studies provided here thus validate that the proposed algorithm to control DVR can perform well under major voltage-related PQ problems.

VII. CONCLUSION

A simple generalized algorithm has been developed for the generation of instantaneous reference compensating voltages for controlling self-supported DVR based on basic SRFT to protect unbalanced and nonlinear loads. A fundamental positive-sequence extractor has been proposed, which extracts three fundamental positive-sequence phase voltages by sensing only two unbalanced and/or distorted line voltages. It has been shown that, when load is nonlinear, only DVR, without a shunt

capacitor filter, is not able to suppress the voltage spikes. The performance of DVR with the proposed control algorithm has been evaluated for both the harmonic current source and the harmonic voltage source type of nonlinear loads with different supply voltage quality problems. The performance of the DVR has been observed to be satisfactory in all the cases. Moreover, it is shown that DVR is capable of providing self-support to its dc bus by taking active power from the ac line at fundamental frequency.

APPENDIX

The parameters of the simulated test system are as follows:

- 1) base kVA: 10 kVA;
- 2) base voltage (ac): 415 V;
- 3) base voltage (dc): 300 V;
- 4) ac source voltage: 415 V, 50 Hz;
- 5) line impedance: $X_{Ls} = 0.3$ p.u., $R_s = 0.05$ p.u.;
- 6) shunt capacitor filter: $X_{Cf} = 3$ p.u.;
- 7) DVR;
- 8) ripple filter: $L_r + L_{transformer} = 4$ mH, $C_r = 60$ μ F, $R_r = 2$ Ω ;

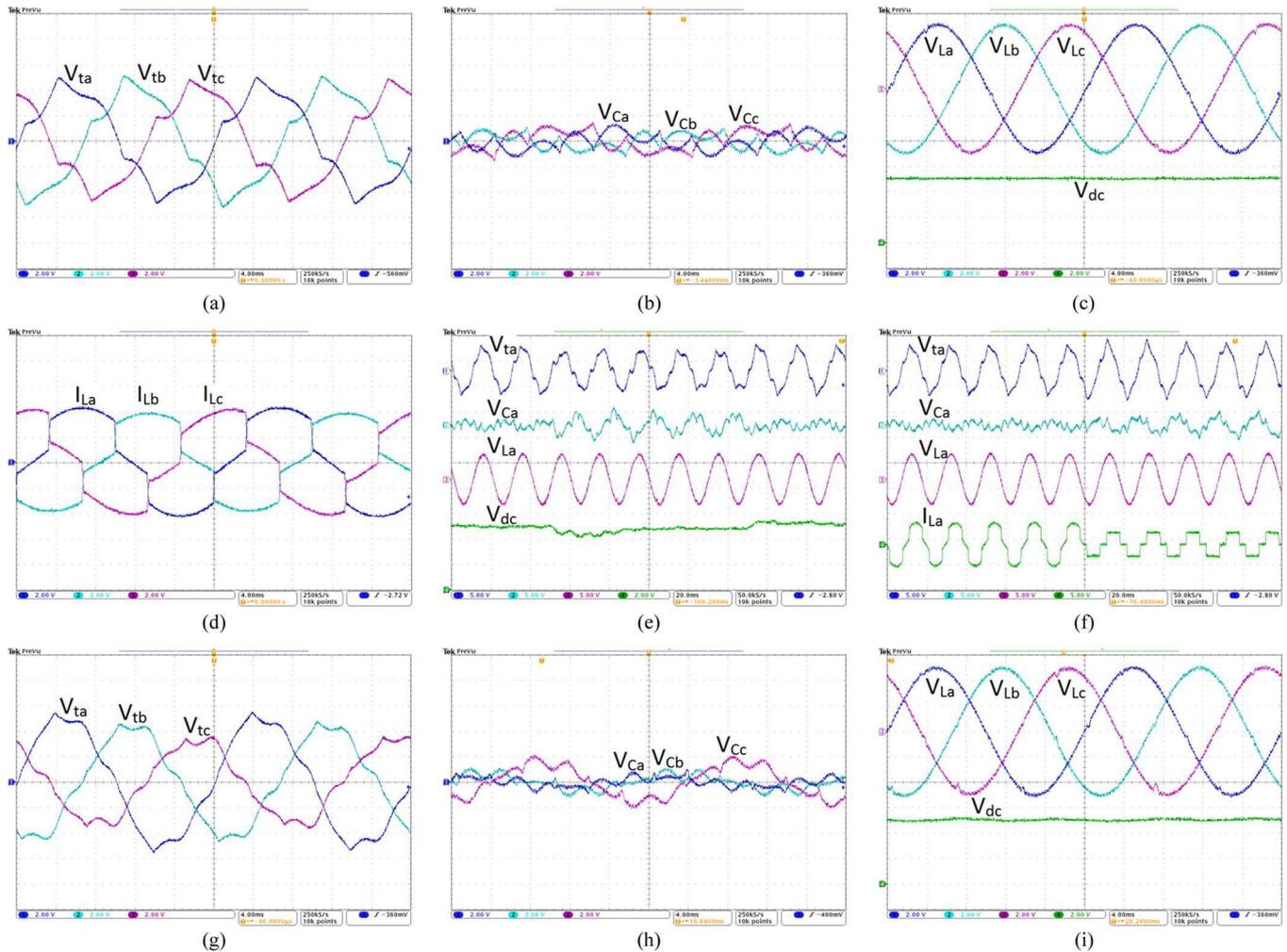


Fig. 16. Real-time experimental results (all the quantities are shown in p.u. where 5 V = 1 p.u.). (a) Steady-state terminal voltages. (b) Injected voltages by DVR (steady state). (c) Steady-state load voltages. (d) Steady load currents. (e) Performance during dynamic sag. (f) Performance during load change. (g) Unbalanced and distorted terminal voltages. (h) Injected voltages by DVR (unbalanced case). (i) Load voltages (unbalanced case).

- 9) dc bus capacitance of DVR: 1000 μ F;
- 10) dc bus voltage of DVR: 300 V;
- 11) series injection transformer: three numbers of single-phase transformers, each with a rating of 3 kVA, 200 V/200 V.

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