

# GRID VOLTAGE SYNCHRONIZATION FOR DISTRIBUTED GENERATION SYSTEMS UNDER GRID FAULT CONDITIONS USING FUZZY LOGIC CONTROLLER

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**ABSTRACT** – In this paper, synchronization of grid voltage of the distributed generation systems was proposed by using fuzzy logic controller. In order to achieve satisfactory results with such systems, it is necessary to count on accurate and fast grid voltage synchronization algorithms, which are able to work under unbalanced and distorted conditions. This paper analyzes the synchronization capability of three advanced synchronization systems: the decoupled double synchronous reference frame phase-locked loop (PLL), the dual second order generalized integrator PLL, and the three-phase enhanced PLL, designed to work under such conditions. Although other systems based on frequency-locked loops have also been developed, PLLs have been chosen due to their link with dq 0 controllers. The simulation was done by using MATLAB/Simulink software.

**Index Terms**— Electric variable measurements, electrical engineering, frequency estimation, frequency-locked loops, harmonic analysis, monitoring, synchronization, Fuzzy logic controller.

## I. INTRODUCTION

In the actual grid code requirements (GCRs), special constraints for the operation of such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand

Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic[7]. Although the LVRT requirements in the different standards are very different, as shown in, the first issue that generation systems must afford when voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel cage induction generators, where the voltage drop in the stator

windings can conduct the generator to an over speed tripping, as shown in[9]. Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions[10],[11],[12].

Likewise, PV systems would also be affected by the same lack of current controllability. Solutions based on the development of auxiliary systems, such as STATCOMs and dynamic voltage regulators (DVRs), have played a decisive role in enhancing the fault ride through (FRT) capability of distributed generation systems, as demonstrated in. Likewise, advanced control functionalities for the power converters have also been proposed[17],[18]. In any case, a fast detection of the fault contributes to improving the effects of these solutions; therefore, the synchronization algorithms are crucial.

In certain countries, the TSOs also provide the active/reactive power pattern to be injected into the network during voltage sag; this is the case for the German E-on and the Spanish Red Electrical Espanola (REE). This trend has been followed by the rest of the TSOs; moreover, it is believed that this operation requirement will be extended, and specific demands for balanced and unbalanced sags will arise in the following versions of the grid codes worldwide. Regarding the operation of the distributed generation systems under balanced and unbalanced fault conditions, relevant contributions, such as, can be found in the literature. These solutions are based on advanced control systems that need to have accurate information of the grid voltage variables in order to work properly, something that has prompted the importance of grid synchronization algorithms[3],[33].

In power systems, the synchronous reference frame PLL (SRF PLL) is the most extended technique for synchronizing with three-phase systems. Nevertheless, despite the fact that the performance of SRF PLL is satisfactory under balanced conditions, its response can be inadequate

under unbalanced, faulty, or distorted conditions. In this paper, three improved and advanced grid synchronization systems are studied and evaluated: the decoupled double synchronous reference frame PLL (DDSRF PLL), the dual second order generalized integrator PLL (DSOGI PLL), and the three-phase enhanced PLL (3phEPLL).

## II. GRID SYNCHRONIZATION SPECIFICATIONS BASED ON GCR

Despite the fact that the detection of the fault can be carried out with simpler algorithms, as shown in and, the importance of advanced grid synchronization systems lies in the necessity of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power required by the TSO. In the German standard, it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the generator transformer to at least 2% of the rated current for each percent of the voltage dip, as shown in Fig. 1. 100% reactive power delivery must be possible, if necessary.

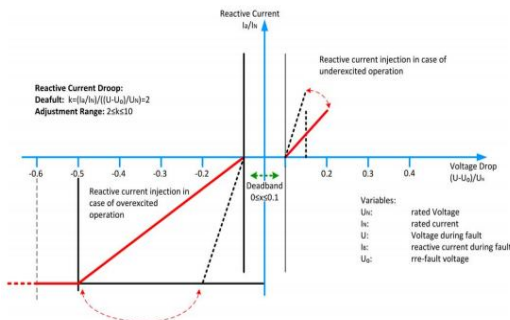


Fig. 1. E-on voltage support requirement in the event of grid fault.

A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and be able to inject full reactive power after 150 ms, as shown in Fig. 2. Considering these demands, this paper will consider that the estimation of the voltage conditions will be carried out within 20–25 ms, as this target permits it to fulfill the most restrictive requirements, in terms of dynamical response, available in the grid codes. T

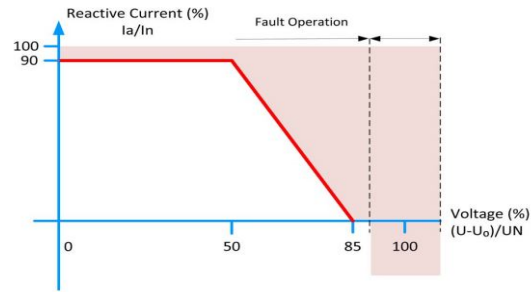


Fig. 2. REE voltage support requirement in the event of grid fault

## DESCRIPTION OF THE THREE SYNCHRONIZATION SYSTEMS

Many authors have discussed different advanced models, which are able to overcome the problems of the classical PLL, using frequency and amplitude adaptive structures which are able to deal with unbalanced, faulty, and harmonic-polluted grids. In the framework of these topologies, three PLL structures will be discussed and evaluated in this paper.

### A. DDSRF PLL

The DDSRF PLL, published, was developed for improving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counterclockwise and another one clockwise, in order to achieve an accurate detection of the positive- and negative-sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF PLL is shown in Fig. 3. When the three-phase grid voltage is unbalanced, the fundamental positive-sequence voltage vector appears as a dc voltage on the dq + 1 axes of the positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the dq– 1 axes of the negative-sequence SRF.

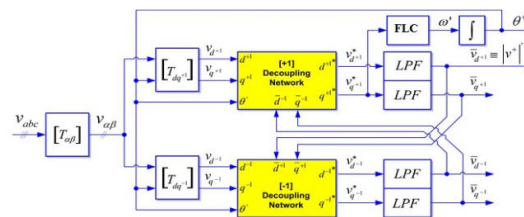


Fig. 3. DDSRF-PLL block diagram

In contrast, the negative sequence voltage vector will cause a dc component on the negative-sequence SRF and an ac oscillation on the positive sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches the dc level on the negative sequence SRF and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes in order to cancel out

such ac oscillations. Low-pass filters (LPFs) in Fig. 3 are responsible for extracting the dc component from the signal on the decoupled SRF axes.

### B. DSOGI PLL

The operating principle of the DSOGI PLL for estimating the positive- and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the  $\alpha\beta$  stationary reference frame as explained in. The diagram of the DSOGI PLL is shown in Fig. 4. As it can be noticed, the ISC method is implemented by the positive-sequence calculation block.

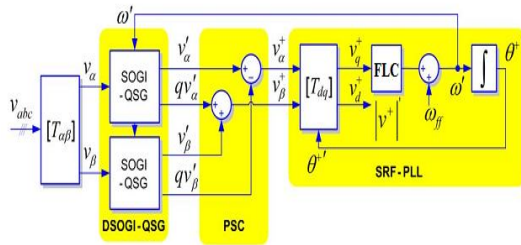


Fig. 4. DSOGI-PLL block diagram.

To apply the ISC method, it is necessary to have a set of signals,  $v_\alpha-v_\beta$ , representing the input voltage vector on the  $\alpha\beta$  stationary reference frame together with another set of signals,  $qv_\alpha-qv_\beta$ , which are in quadrature and lagged with respect to  $v_\alpha-v_\beta$ . In the DSOGI PLL, the signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI), which is an adaptive bandpass filter based on the generalized integrator concept [42]. At its output, the DSOGI provides four signals, namely,  $v_\alpha$  and  $v_\beta$ , which are filtered versions of  $v_\alpha$  and  $v_\beta$ , respectively, and  $qv_\alpha$  and  $qv_\beta$ , which are the in-quadrature versions of  $v_\alpha$  and  $v_\beta$ .

### C. 3phEPLL

The enhanced phase-locked loop (EPLL) is a synchronization system that has proven to provide good results in single phase synchronization systems. An EPLL is essentially an adaptive band-pass filter, which is able to adjust the cutoff frequency as a function of the input signal. Its structure was later adapted for the three-phase case, in order to detect the positive-sequence vector of three-phase signals, obtaining the 3phEPLL that is represented in Fig. 5.

In this case, each phase voltage is processed independently by an EPLL. This block filters the input signal and generates two sinusoidal outputs of the same amplitude and frequency,  $v_n$  and  $jv_n$ , the second one being  $90^\circ$  with respect to  $v_n$ . The resulting signals constitute the input for the

computational unit. Owing to these in-quadrature signals, the instantaneous positive-sequence voltage component,  $v_a^+ v_b^+ v_c^+$ , can be estimated by means of using the ISC method.

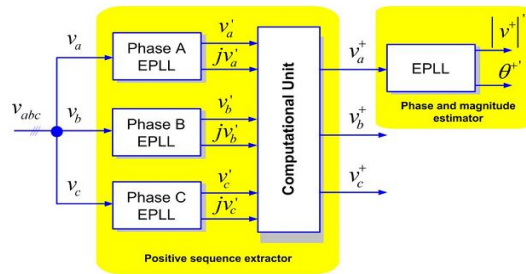


Fig. 5. 3phEPLL block diagram.

## III. DISCRETE IMPLEMENTATION

The performance of the different structures under test is really dependent on their final digital implementation, particularly on the discretization approach made to their continuous equations. This implementation is critical and should be studied in detail as a straightforward implementation can give rise to additional delays in the loop that hinder the good performance of the PLL.

Some methods, such as the forward Euler, the backward Euler, and the Tustin (trapezoidal) numerical integration, offer a good performance when used for discretizing other synchronization systems, as shown. However, Euler methods can be inadequate under certain conditions, due to the need of introducing additional sample delays. Therefore, according to the specific needs of the presented topologies, this section will describe the discrete representation of each PLL individually.

### A. DDSRF-PLL Discretization

The discrete model of this PLL can be easily obtained since the continuous representation of several parts does not change in the discrete domain. This is the case for the transformation blocks  $T_\alpha\beta$ ,  $T_{dq+1}$ , and  $T_{dq-1}$ , whose description can be found in general scope literature.

#### 1) Positive- and Negative-Sequence Decoupling Networks:

The decoupling network constitutes one of the most important contributions of this synchronization method. The discrete equations of these blocks are shown in (1), being almost the same as in the continuous domain [41]. It is just necessary to consider one sample delay of  $\theta$ ,  $v^-d-1$ ,  $v^-q-1$ ,  $v^-d+1$ , and  $v^-q+1$  in order to avoid algebraic loops.

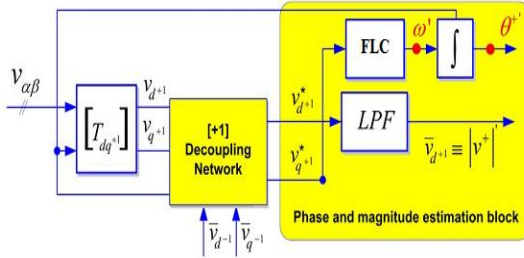


Fig. 6. Phase and magnitude estimation loop of the DDSRF PLL.

## 2) Phase and Magnitude Estimator Discretization:

In the DDSRF PLL, the decoupling network appears embedded in the classical SRF-PLL loop (see Fig. 6). However, this does not affect the discretization of the phase and magnitude estimator since  $v^* d + 1$  and  $vq^* + 1$  act as the input of this block

$$\begin{bmatrix} V_{d+1}^*[n+1] \\ V_{q+1}^*[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{d+1}[n+1] \\ V_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} V_{d-1}[n] \\ V_{q-1}[n] \end{bmatrix} \times \begin{bmatrix} V_{d-1}^*[n+1] \\ V_{q-1}^*[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} V_{d-1}[n+1] \\ V_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} V_{d+1}[n] \\ V_{q+1}[n] \end{bmatrix} \quad (1)$$

The discrete controller and the integrator can be built using a backward numerical approximation. The frequency and phase can then be represented in the z-domain (2), considering  $v^* q+1$  as the error to be minimized. In this equation, a feed forward the nominal frequency is given by means of  $\omega'$

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V_{q+1}^*(z) + \omega' \theta^+ = \frac{T_s z}{z-1} \cdot W'(z) \quad (2)$$

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot V_{q+1}^*[n] + (k_p + k_i \cdot T_s) \cdot V_{q+1}^*[n+1] \theta^+[n+1] = \theta^+[n] + T_s \cdot \omega'[n+1] \quad (3)$$

In these equations, a frequency feed forward has been introduced as an initial condition to  $\omega$ .

## 3) LPF Block Discretization:

The amplitudes of the dq positive- and negative-sequence components are the outputs of the decoupling networks. However, four infinite impulse

responses (IIR) LPFs extract the ripple from each sequence estimation in order to reinforce the performance of the PLL in case of harmonic pollution. A first-order filter with a cutoff frequency  $\omega_f$ , equal to half of the grid frequency, was originally proposed in [41]; hence, the same transfer function has been implemented in this paper for evaluation purposes in

$$y[n] = \frac{1}{T_s \omega_f + 1} \cdot x[n] + \frac{T_s \omega_f}{T_s \omega_f + 1} \cdot u[n] \cdot x[n+1] = y[n] \quad (4)$$

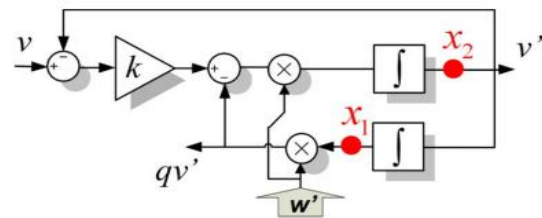
## B. DSOGI-PLL Discretization:

### 1) DSOGI-QSG Block Discretization:

As was previously mentioned in Section II, the DSOGI-based quadrature signal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). Therefore, each SOGI-based quadrature signal generator can be discretized individually, thus facilitating its mathematical description. In Fig. 7, the block diagram of the implemented SOGI is shown. This quadrature signal generator (QSG) is a linear system itself; therefore, a discrete representation can be systematically obtained if the continuous state space is previously deduced. The equations of the SOGI state space appear detailed in (5), where  $v$  constitutes the input while  $v$  and  $qv$  are the two in-quadrature output signals

$$\begin{cases} \dot{x}_n = A \cdot x_n + B \cdot v \\ y_n = C \cdot x_n \end{cases}; x_n = \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}; y_n = \begin{bmatrix} v' \\ qv' \end{bmatrix}$$

$$A = \begin{bmatrix} 0 & 1 \\ -\omega'^2 & -k \cdot \omega' \end{bmatrix}; B = \begin{bmatrix} 0 \\ k \cdot \omega' \end{bmatrix}; C = \begin{bmatrix} 0 & 1 \\ \omega' & 0 \end{bmatrix} \quad (5)$$



SOGI - QSG

Fig. 7. Quadrature signal generator based on a second order generalized integrator (SOGI QSG)

The symbolic values of each matrix of (7) are detailed in (6), shown at the bottom of the page. In these matrices,  $T_s$  is the sampling time of the discrete system,  $\omega[n]$  is the estimated frequency magnitude, which comes from the estimation made at the SRF-PLL block at each computation step, and  $k$  is the SOGI gain.

$$X[n+1] = A' \cdot x[n] + B' \cdot v[n]$$



$$y[n] = c' \cdot x[n] + D' \cdot v[n] \quad (7)$$

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure presented in.

$$A' = \left(1 + \frac{A \cdot T_s}{2}\right) \left(1 - \frac{A \cdot T_s}{2}\right)^{-1}$$

$$B' = \left(1 - \frac{A \cdot T_s}{2}\right)^{-1} \cdot B$$

$$C' = T_s \cdot C \cdot \left(1 - \frac{A \cdot T_s}{2}\right)^{-1}$$

$$D' = C \left(1 - \frac{A \cdot T_s}{2}\right)^{-1} \cdot \frac{B \cdot T_s}{2} \quad (8)$$

Where  $T_s$  is the sampling time. The resulting discrete system is the best option as it reduces the need of using additional delays for breaking algebraic loops that appear using other methods which do not consider the SOGI QSG as a whole.

### 2) SRF PLL Discretization:

The frequency and phase detection is obtained by means of the SRF PLL shown in Fig. 8.

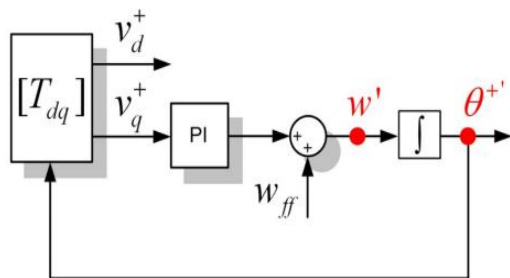


Fig. 8. State variables of the SRF-PLL block.

The discretization of the controller and the integrator is performed using the backward numerical approximation. The frequency and phase can then be represented in the z-domain, as shown in (9), where  $v+q$  constitutes the error to be minimized

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V_{q+1}^*(z) + \omega_{ff} \theta^+ = \frac{T_s \cdot z}{z-1} \cdot W'(z) \quad (9)$$

It can be noticed that the previous equations in (9) are equal to (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample-based representation of (9) can be written as shown in

$$\omega'[n+1] = \omega'[n] - k_p \cdot v_{q+1}^*[n] + (k_p + k_i \cdot T_s) \cdot v_{q+1}^*[n+1]$$

$$\theta^+[n+1] = \theta^+[n] + T_s \cdot \omega'[n+1] \quad (10)$$

### C. 3phEPLL Discretization

This three-phase grid synchronization system exploits the EPLL as a quadrature signal generator. An independent EPLL is used for processing each one of the three-phase voltages. The same EPLL structure is applied again to detect the magnitude and phase of the positive-sequence voltage component.

**1) QSG Block—EPLL Discretization:** The block diagram of the EPLL implemented in this paper is presented in Fig. 9. According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$\dot{A}'(t) = k \cdot e(t) \cdot \cos \theta'(t)$$

$$\dot{\omega}'(t) = -k \cdot e(t) \cdot \sin \theta'(t)$$

$$\theta(t) = \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t) \quad (11)$$

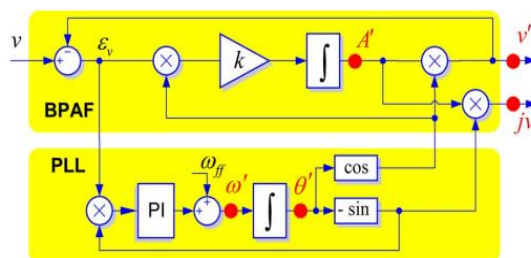


Fig. 9. Quadrature signal generator based on an EPLL structure.

Finally, after the state variables are calculated, the EPLL output can be obtained by (13), generating the two quadrature signals

$$V'[n+1] = A'[n+1] \cdot \cos(\theta'[n+1])$$

$$qv'[n+1] = -A'[n+1] \cdot \sin(\theta'[n+1]) \quad (13)$$

This type of discretization method needs a more accurate tuning, due to the fact that the stable regions of the s-plane and z-plane are different [52]. However, its major simplicity, compared to the Tustin or backward integration, benefits from the computational speed of this block.

**2) Computational Block Unit:** The description for this block is the same in both discrete and continuous domains. Nevertheless, specific equations are used in this paper, as shown in (14).

**3) Phase and Magnitude Detection Block:** This element is based on another EPLL, which is responsible for estimating the phase and the magnitude of the positive-sequence fundamental component.

However, for the phase and magnitude detection block, the outputs are the positive sequence

magnitude and phase, which correspond directly with the states  $\theta$  and  $A$ , respectively.

#### IV. FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC.

The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

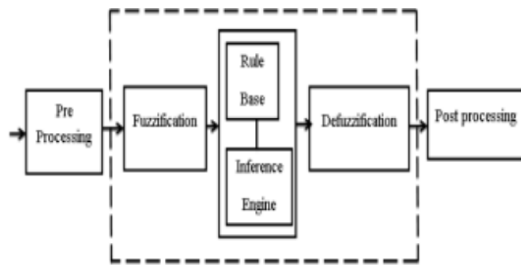


Fig.10.Fuzzy logic controller

**Fuzzification:** Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The Partition of fuzzy subsets and the shape of membership  $CE(k)$   $E(k)$  function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor.

TABLE I: Fuzzy Rules

Change in error	Error						
	NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular  $E(k)$  input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{P_{ph(k)} - P_{ph(k-1)}}{V_{ph(k)} - V_{ph(k-1)}} \quad (13)$$

$$CE(k) = E(k) - E(k-1) \quad (14)$$

**Inference Method:** Several composition methods such as Max-Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the minimum operator and maximum operator. Table 1 shows rule base of the FLC.

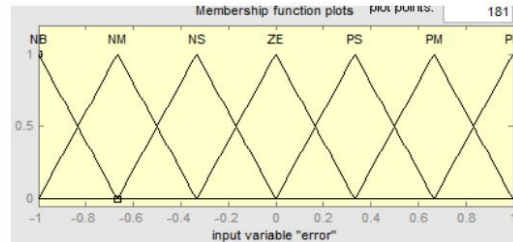


Fig.11.Membership functions

**Defuzzification:** As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height“ method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output

The set of FC rules are derived from

$$u = -[\alpha E + (1-\alpha)C] \quad (15)$$

Where  $\alpha$  is self-adjustable factor which can regulate the whole operation.  $E$  is the error of the system,  $C$  is the change in error and  $u$  is the control variable. A large value of error  $E$  indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible. One the other hand, small value of the error  $E$  indicates that the system is near to balanced state.

#### V. SIMULATION RESULTS

Following the representations in the discrete domain already deducted, the different PLL algorithms have been implemented in a control board based on a floating-point Texas Instruments TMS320F28335 DSP at 150 MHz (6.67-ns cycle time). Their capability to perform a fast and accurate synchronization has been tested in the laboratory under different grid fault scenarios, where the three-phase voltage waveforms experience transients due

to the appearance of voltage sags, frequency variations, and harmonic pollution..

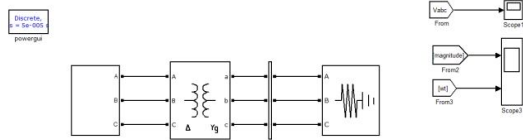


Fig. 12. Matlab model for proposed system

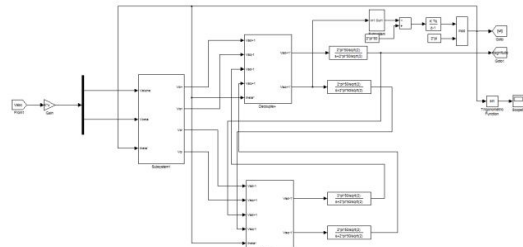


Fig. 13 Matlab model of control strategy with DDSRF PLL

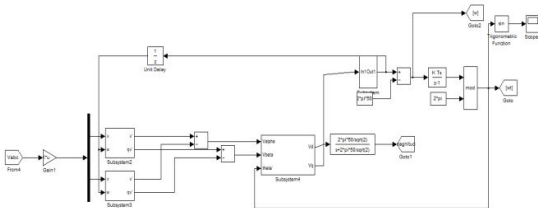


Fig. 14 Matlab model of control strategy with DSOGI PLL

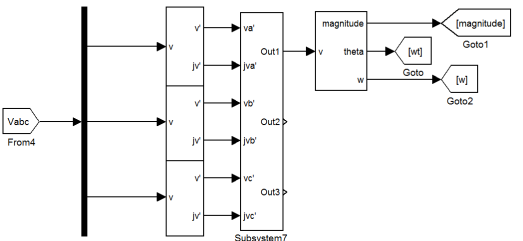
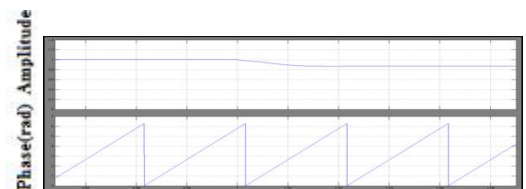
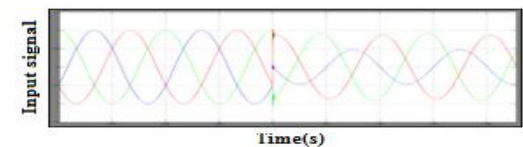
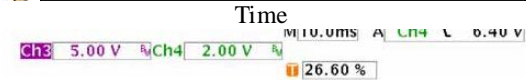
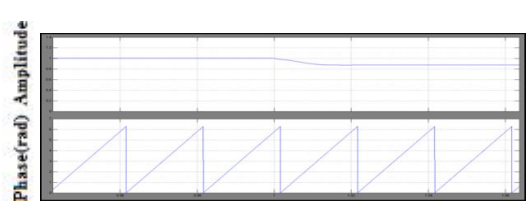
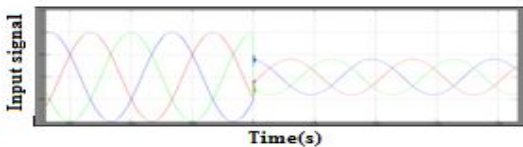
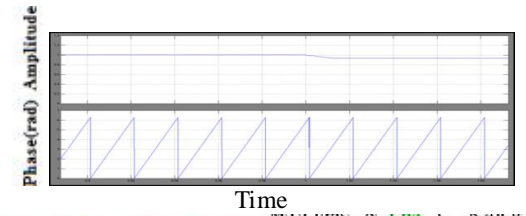
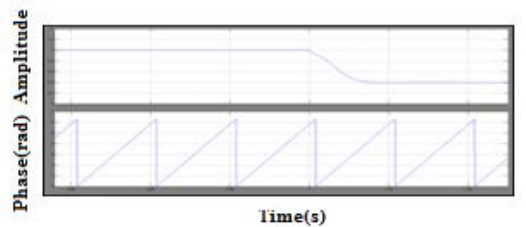
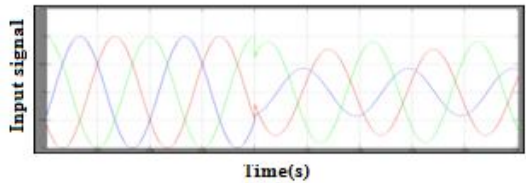
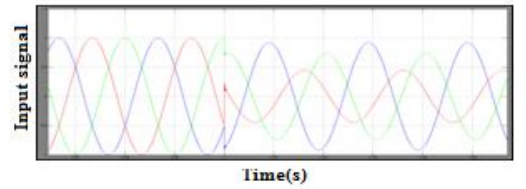


Fig. 15 Matlab model of control strategy with 3phEPLL



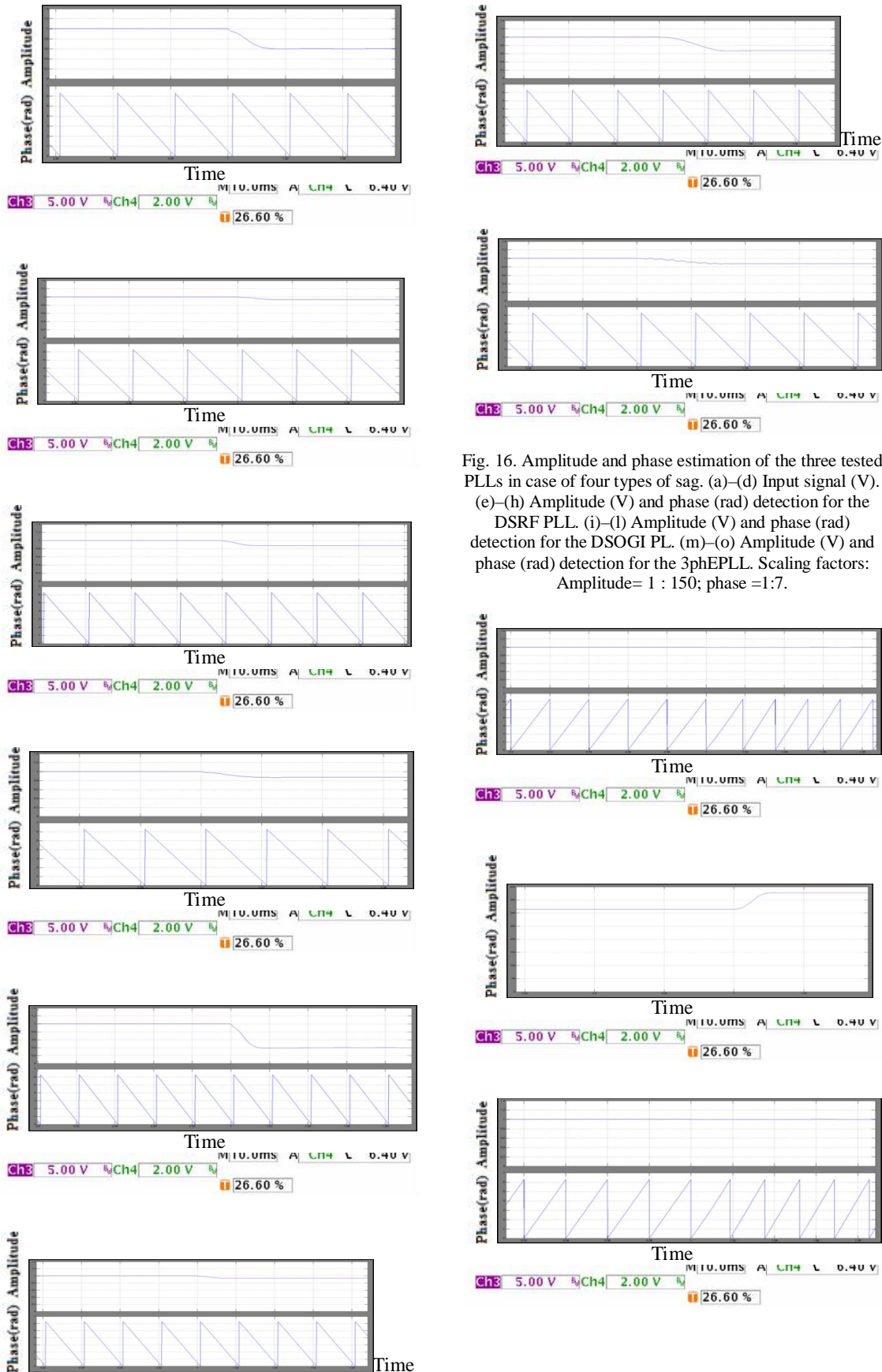


Fig. 16. Amplitude and phase estimation of the three tested PLLs in case of four types of sag. (a)–(d) Input signal (V). (e)–(h) Amplitude (V) and phase (rad) detection for the DSRF PLL. (i)–(l) Amplitude (V) and phase (rad) detection for the DSOGI PL. (m)–(o) Amplitude (V) and phase (rad) detection for the 3phEPLL. Scaling factors: Amplitude= 1 : 150; phase =1:7.



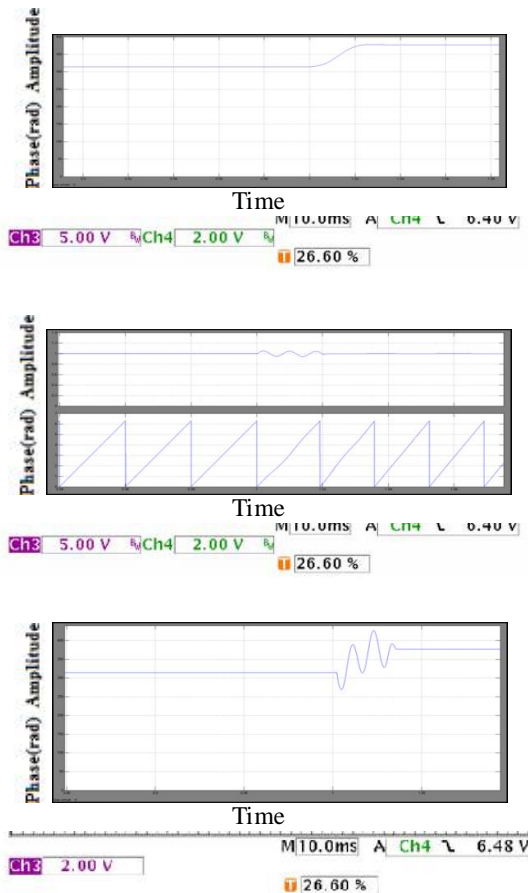


Fig. 17. Amplitude, phase, and frequency estimation of the three tested PLLs in a frequency jump. (a) and (b) Amplitude (V), phase (rad), and frequency detection for the DDSRF PLL. (c) and (d) Amplitude (V), phase (rad), and frequency detection for the DSOGI PLL. (e) and (f) Amplitude (V), phase (rad), and frequency detection for the 3phEPLL. Scaling factors: Amplitude=1:150, phase =1:7, and frequency 1:70.

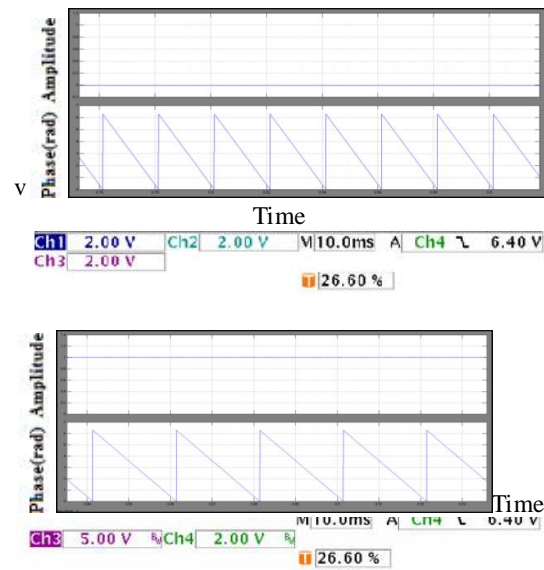
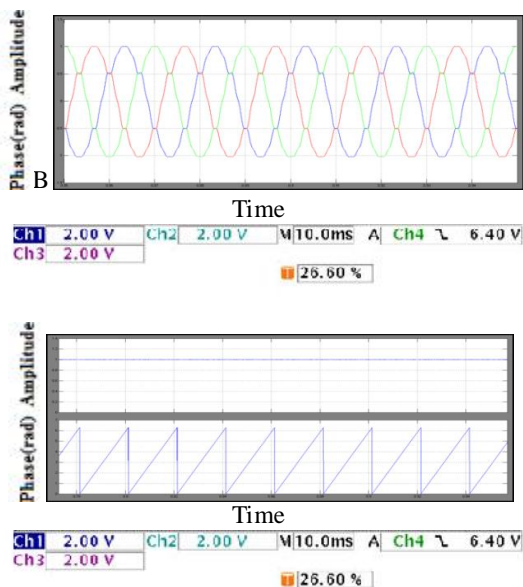


Fig. 18. Amplitude and phase estimation of the three tested PLLs in a polluted grid (THD=8%). (a) Input signal (V). (b) Amplitude (V) and phase detection (rad) for the DDSRF PLL. (c) Amplitude (V) and phase detection (rad) for the DSOGI PLL. (d) Amplitude (V) and phase detection (rad) for the 3phEPLL. Scaling factors: Amplitude= 1 : 150; phase =1:7

## VI CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems by using fuzzy logic controller. Their structures have been presented, and their discrete algorithms have been detailed. The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater band pass and low-pass filtering capabilities. Here we are using fuzzy logic controller instead of using other controllers. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmonics. Although all three have been shown to be appropriate for synchronizing with the network voltage in distributed power generation applications, mainly PV and wind power, the lower computational cost of the DDSRF PLL and the DSOGI PLL, together with their robust estimation of the voltage parameters, offers a better tradeoff between the presented systems, making them particularly suitable for wind power applications. The simulation was done by using Fuzzy logic controller.

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