

A Novel Three Phase Neutral Voltage Modulation Strategy for Eleven Level Inverter with Reduced Number of Switches

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Abstract:

This project illustrates a novel pulse width modulation strategy for a three phase eleven level inverter with a reduced number of switches. Mainly this project includes the balanced line-to-line output voltages to control the modulation index for operation unbalanced dc-links. In the proposed structure, too large of a dc-link imbalance precludes the balancing of the output voltages. This limitation is also discussed. The simulations for a Eleven-level phase-shifted modulated MLCI for electric vehicle traction motor drive show that the proposed method is able to balance line-to-line output voltages as well as to maximize the linear modulation range under the unbalanced dc-link conditions with reduced number of switches

MODELLING OF CASE STUDY

Ii. System Configuration And Voltage Vector Space Analysis

A. Configuration of MLCI for EV Traction Motor Drive

Fig. 1 shows the EV traction motor drive system that is dealt with in this paper. In this configuration, various power ratings can be easily implemented by configuring the number of the single H-bridge modules according to a

required specification such as a neighborhood EV, full-size sedan, and so on. Here, each H-bridge module incorporates voltage and current sensing circuitries, gate drivers, and communication interfaces between the module itself and the main controller. In addition, battery cells can be also included in the H-bridge module. The unipolar modulation technique is applied between two switching legs in the H-bridge module. Consequently, the effective switching frequency in each H-bridge module is twice the carrier frequency. In addition to this, the well-known PS modulation technique is used to implement interleaving and multilevel operation. Therefore, the effective switching frequency f_{sw} in a phase is

$$f_{sw} = 2N \times f_c \quad (1)$$

Where N and f_c represent the number of the H-bridge modules in each phase and the carrier frequency of PWM, respectively. As an example, Fig. 2 shows the carriers for each module, the duty cycles in unipolar modulation, and the output voltage when $N = 2$.

B. Voltage Vector Space Analysis

When the dc-link voltage of a single H-bridge module is V_{dc} , the output voltage v_{pn} has three states, i.e., V_{dc} , 0, and $-V_{dc}$,

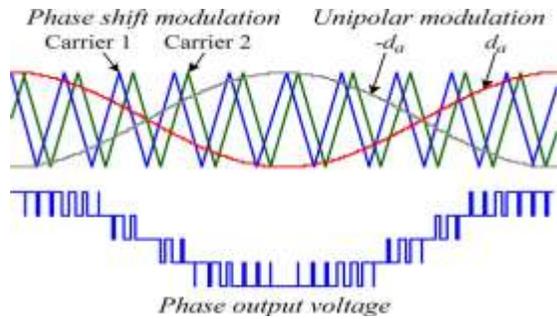


Fig. 2. Unipolar and phase shift modulation for single H-bridge module.

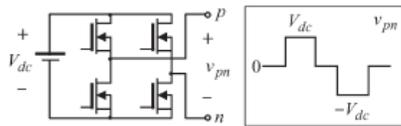


Fig. 3. Output voltage of a single H-bridge module.

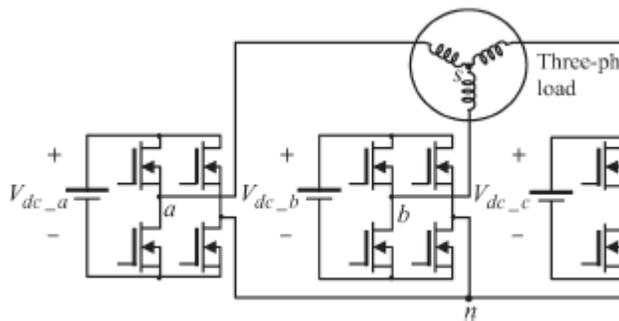


Fig. 4. One-by-three configuration MLCI.

As shown in Fig. 3. By adopting the concept of a switching function, it can be represented as

$$v_{pn} = S_p V_{dc}$$

$$S_p \in \{-1, 0, 1\}_{p=a,b, \text{or}, c} \quad (2)$$

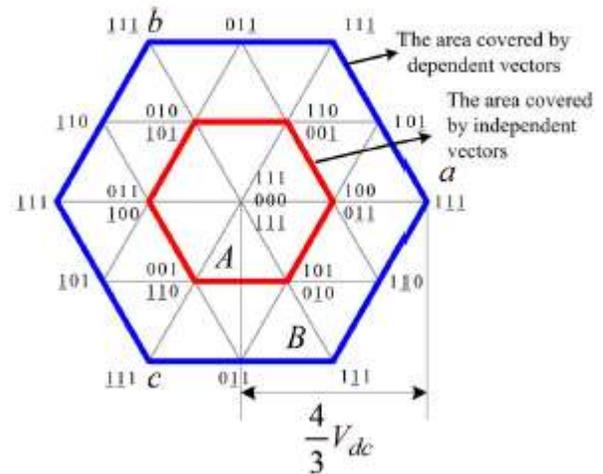
Where S_p is a switching function and p can be replaced with a , b , or c , which represent the phases. Fig. 4 shows a simple one-by-three configuration MLCI. For voltage vector space analysis, the main concept is derived from this simple topology, and then, it is expanded to more levels. In Fig. 4, there are two neutral points s and n in the MLCI. Here, the voltage between the output point of each phase and the neutral point n is defined as the pole voltage. The pole voltages are represented as v_{an} , v_{bn} , and v_{cn} . The voltage between the output point of each phase and the load side neutral point s

is specified as the phase voltage. The phase voltages include v_{as} , v_{bs} , and v_{cs} . By using this concept, the voltage between the two neutral points is defined as v_{sn} and can be written as

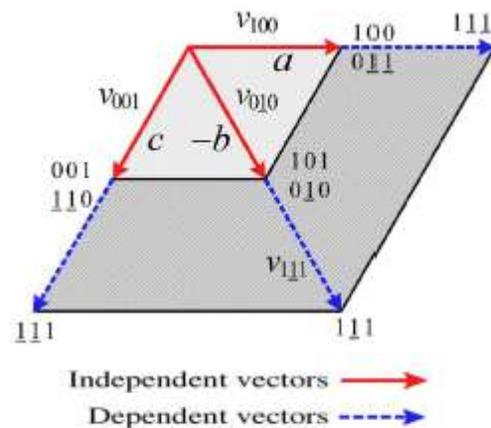
$$v_{sn} = -v_{as} + v_{an} = -v_{bs} + v_{bn} = -v_{cs} + v_{cn} \quad (3)$$

By using the condition that the sum of all phase voltages is zero because the load does not have a neutral line, v_{sn} is rewritten as

$$v_{sn} = \frac{1}{3}(v_{an} + v_{bn} + v_{cn}) \quad (4)$$



(a)



(b)

Fig. 5. Voltage vector space of one-by-three configuration MLCI.

By substituting (4) into (3), the phase voltage of each phase is represented as follows by using the relationship defined in (2):

$$v_{as} = \frac{2}{3}S_aV_{dc_a} - \frac{1}{3}S_bV_{dc_b} - \frac{1}{3}S_cV_{dc_c}$$

$$v_{bs} = -\frac{1}{3}S_aV_{dc_a} + \frac{2}{3}S_bV_{dc_b} - \frac{1}{3}S_cV_{dc_c}$$

$$v_{cs} = -\frac{1}{3}S_aV_{dc_a} - \frac{1}{3}S_bV_{dc_b} + \frac{2}{3}S_cV_{dc_c}$$

(5)

If the magnitudes of three dc links are balanced so that V_{dc_a} , V_{dc_b} , and V_{dc_c} have the same value V_{dc} , the voltage vector space in $\alpha-\beta$ coordinates is defined in Fig. 5(a) by using (5). In the figure, underbars indicate that the switching function has the value of -1 . A part of the hexagon in Fig. 5(a) is shown in Fig. 5(b). In this figure, the vectors v_{010} and v_{111} are placed at the same reference axis, phase b . However, the constituents of those vectors are different. For v_{010} , this vector can be synthesized without the other two phases' assistance. However, v_{111} cannot be produced without other vectors according to (5). From this, let the vectors which do not require other two phases' assistance to be defined as "the independent vectors." Similarly, the vectors which require other phases' support are defined as "the dependent vectors." According to these definitions, v_{100} , v_{001} , and v_{010} are the independent vectors, while v_{111} , v_{111} , and v_{111} are the dependent vectors in Fig. 5(b). Fig. 5(a) also compares the regions that can be composed by the independent

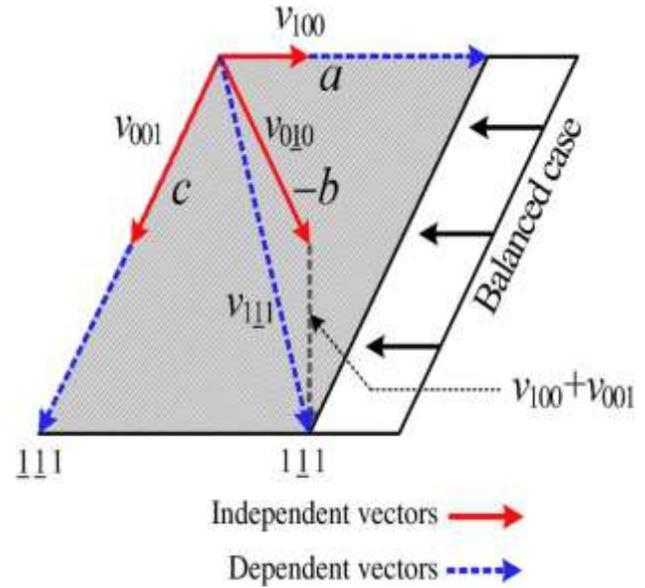


Fig. 6. Voltage vector space in an unbalanced dc-link condition.

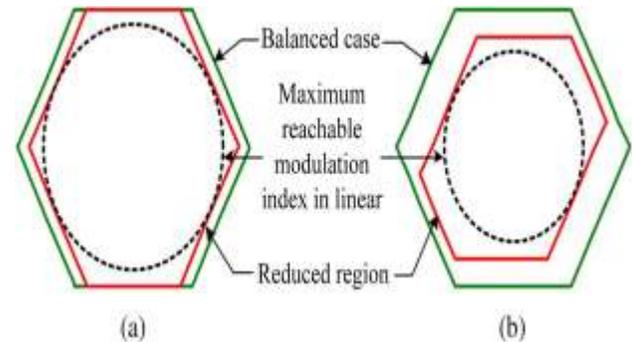


Fig. 7. Comparison of the voltage vector space under different dc-link ratios.

(a) $V_{dc_a} < V_{dc_b} = V_{dc_c}$. (b) $V_{dc_b} < V_{dc_a} < V_{dc_c}$.

and the dependent vectors. Unlike traditional three-phase half bridge inverters, the independent vectors can be fully applied in a switching period because the dc links in each of the three phases are separated in the given system. It should be noted that the maximum voltage is decided by the dependent vectors in the entire voltage vector space. Now, let us consider the case when a three-phase load is supplied by unequal dc links. Fig. 6 shows an extremely unbalanced case where V_{dc_a} is half of the others. If V_{dc_a} decreases, the magnitudes of the independent vectors in phase a are also reduced. As a result, the magnitude of v_{100} is decreased. Here, the phase angle of

v_{111} , which is the sum of v_{010} , v_{100} , and v_{001} , is no longer matched with the angle of the independent vectors in phase b from the figure. As shown in the figure, if the magnitudes of the independent vectors are reduced, the available voltage vector space is also reduced, and the angles of the dependent vectors are no longer multiples of 60° . Using these properties, the voltage vector spaces in two different cases are compared in Fig. 7. In Fig. 7(a), V_{dc_a} has a lower value than the others. In Fig. 7(b), all three dc links have different voltages. As it can be seen in Fig. 7, the original shape of the hexagon is distorted in both cases. This means that the trajectory of the maximum output voltage vector in the $\alpha-\beta$ coordinates is also distorted according to the shape of the hexagon in each. On the other hand, the magnitude of the maximum modulation index in the linear modulation range in a given hexagon corresponds to the radius of the inner circle which is inscribed in the hexagon. As shown in Fig. 7, the radius is changed as the hexagon distorts, and the achievable linear modulation range is also altered. Here, the maximum amplitude of the phase voltage V_{ph_max} in the linear modulation range is defined as

$$V_{ph_max} = V_m \left(V_{dc_max} \frac{\sqrt{3}}{2} \right)$$

$$V_m = \left(\frac{4}{3} \underbrace{\frac{2V_{dc_max} - V_{dc_mid}}{3}}_{\text{Voltage limitation from the medium dc link}} - \frac{2V_{dc_max} - V_{dc_min}}{3} \underbrace{\frac{1}{V_{dc_max}}}_{\text{Voltage limitation from the minimum dc link}} \right)$$

(6)

Where V_{dc_max} , V_{dc_mid} , and V_{dc_min} represent the maximum, medium, and minimum voltages among the dc links. In fact, (6) can be simplified as

$$V_{ph_max} = \frac{V_{dc_mid} + V_{dc_min}}{\sqrt{3}}$$

(7)

It should be noted that V_{ph_max} is the maximum synthesizable voltage in the linear modulation range in the MLCI undergoing unbalanced dc-link conditions. From (7), it can be recognized that V_{ph_max} is determined by V_{dc_mid} and V_{dc_min} . If all dc links are well balanced so that V_{dc_mid} and V_{dc_min} have identical values, (7) is rewritten as

$$V_{ph_max} = \frac{2}{\sqrt{3}} V_{dc}$$

(8)

This is exactly double the maximum synthesizable voltage in the linear modulation range of a traditional three-phase half bridge inverter. In fact, the inverter in Fig. 4 is considered as a three-phase full-bridge inverter which is fed by independent dc links. To extend the proposed approach to the multistage MLCI using PS modulation, the total dc-link voltage per phase is represented as

$$V_{dc_p} = \sum_{j=1}^N V_{dc_p(j)_{p=a,b,or c}}$$

(9)

where p represents a certain phase among phases a , b , and c , N is the number of the power stage modules in each phase, and j represents the index of a power stage module in each phase. In the multistage MLCI, (9) is utilized to obtain V_{dc_max} , V_{dc_mid} , and V_{dc_min} . After that, (7) is still applied.

III. PROPOSED MODULATION TECHNIQUE

In Section II, the maximum synthesizable voltage in the linear modulation range was evaluated under the unbalanced dc links. In this section, a method is proposed to realize the maximum modulation index in the linear modulation range under these conditions.

A. Traditional Offset Voltage Injection Method:

The offset voltage injection scheme is a popular technique in three-phase half-bridge inverter applications. The theory behind this is that an offset voltage is incorporated with phase voltage

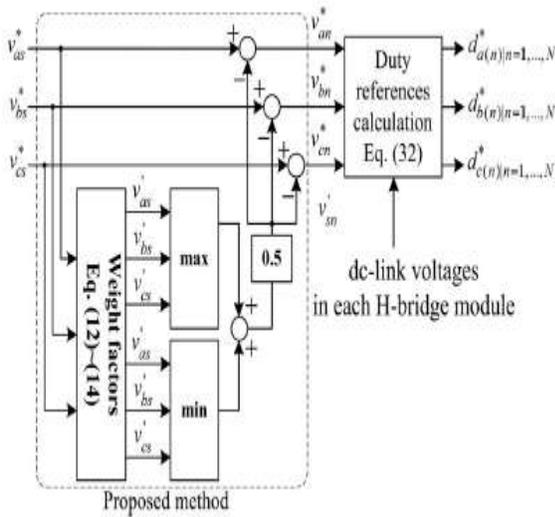


Fig. 8. Implementation of the NVM method. references to implement various PWM schemes in carrier-based PWM by using the fact that line-to-line voltages are applied to a three-phase load [43], [44]. For example, the offset voltage v^*_{sn} is injected to the phase voltage references v^*_{as} , v^*_{bs} , and v^*_{cs} to implement carrier-based SVPWM as in

$$v^*_{sn} = \frac{v^*_{\max} + v^*_{\min}}{2} \quad v^*_{\max} = \max(v^*_{as}, v^*_{bs}) \quad (10)$$

$$v^*_{\min} = \min(v^*_{as}, v^*_{bs}, v^*_{cs}).$$

Then, the pole voltage references v^*_{an} , v^*_{bn} , and v^*_{cn} , which will be converted to PWM duty references, are

$$v^*_{an} = v^*_{as} - v^*_{sn} \quad v^*_{bn} = v^*_{bs} - v^*_{sn} \quad v^*_{cn} = v^*_{cs} - v^*_{sn}. \quad (11)$$

However, the aforementioned technique may not maximize the linear modulation range in MLCI undergoing unbalanced dc-link conditions.

B. Proposed NVM Method

If the dc links in an MLCI are unbalanced and the traditional offset voltage injection methods are utilized, the three-phase output voltages may become distorted as the phase voltage reference approaches V_{ph_max} . This is because the traditional methods are not considering unbalanced dc-link conditions. Therefore, even if a phase can synthesize an

output voltage reference in the linear modulation range, the other phases can be saturated or go into the overmodulation region. In this situation, a neutral voltage can be produced by the saturated or overmodulated phase. In order to resolve this issue and to synthesize the output voltage to V_{ph_max} in the linear modulation range, the NVM technique is proposed in this paper. Fig. 8 shows the concept of the proposed NVM technique. Here, a neutral voltage between the two neutral points n and s in Fig. 4 is modulated to compensate the output voltage imbalance caused by unbalanced dc-link conditions. To do this, first, the weight constant K_w is defined as

$$K_w = \frac{V_{dc_mid} + V_{dc_min}}{2}. \quad (12)$$

By using (12), the weight factors are calculated as

$$K_{w_a} = \frac{K_w}{V_{dc_a}} \quad K_{w_b} = \frac{K_w}{V_{dc_b}} \quad K_{w_c} = \frac{K_w}{V_{dc_c}} \quad (13)$$

where K_{w_a} , K_{w_b} , and K_{w_c} represent the weight factors for phases a , b , and c , respectively. Next, the weight factors are multiplied by the phase voltage references, and the new references $v_{_as}$, $v_{_bs}$, and $v_{_cs}$ are obtained as

$$v'_{as} = K_{w_a} v^*_{as} \quad v'_{bs} = K_{w_b} v^*_{bs} \quad v'_{cs} = K_{w_c} v^*_{cs}. \quad (14)$$

It should be noted that, depending on dc-link conditions, the sum of $v_{_as}$, $v_{_bs}$, and $v_{_cs}$ may not be zero. By using these components, the injected voltage $v_{_sn}$ and the pole voltage references are given as

$$v'_{\max} = \max(v'_{as}, v'_{bs}, v'_{cs}) \quad v'_{\min} = \min(v'_{as}, v'_{bs}, v'_{cs}) \quad (15)$$

$$v'_{sn} = \frac{v'_{\max} + v'_{\min}}{2} \quad \begin{bmatrix} v^*_{an} \\ v^*_{bn} \\ v^*_{cn} \end{bmatrix} = \begin{bmatrix} v^*_{as} - v'_{sn} \\ v^*_{bs} - v'_{sn} \\ v^*_{cs} - v'_{sn} \end{bmatrix}.$$

From (15), the line-to-line voltages across each phase of the load are represented as

$$\begin{aligned} \begin{bmatrix} v_{ab}^* \\ v_{bc}^* \\ v_{ca}^* \end{bmatrix} &= \begin{bmatrix} v_{an}^* - v_{bn}^* \\ v_{bn}^* - v_{cn}^* \\ v_{cn}^* - v_{an}^* \end{bmatrix} = \begin{bmatrix} v_{as}^* - v'_{sn} - v_{bs}^* + v'_{sn} \\ v_{bs}^* - v'_{sn} - v_{cs}^* + v'_{sn} \\ v_{cs}^* - v'_{sn} - v_{as}^* + v'_{sn} \end{bmatrix} \\ &= \begin{bmatrix} v_{as}^* - v_{bs}^* \\ v_{bs}^* - v_{cs}^* \\ v_{cs}^* - v_{as}^* \end{bmatrix}. \end{aligned} \quad (16)$$

As it can be seen in (16), v_{sn} does not appear in the line-to-line voltages, and it is still considered as a hidden freedom of voltage modulation. Now, let us consider the role of the weight factors K_{w_a} , K_{w_b} , and K_{w_c} , which are inversely proportional to the corresponding dc-link voltage. For convenience, let us assume that the magnitudes of the dc-link voltage are under the following relationship:

$$V_{dc_a} < V_{dc_b} < V_{dc_c}. \quad (17)$$

Then, from (13) and (17)

$$\begin{aligned} K_{w_a} > K_{w_b} > K_{w_c} & \quad K_{w_a} > 1 \\ K_{w_b}, K_{w_c} < 1. & \quad (18) \end{aligned}$$

Equation (18) gives

$$|v'_{as}| > |v_{as}^*| \quad |v'_{bs}| < |v_{bs}^*| \quad |v'_{cs}| < |v_{cs}^*|. \quad (19)$$

From (15) and (19), it can be recognized that, if v'_{as} , whose dc-link voltage is less than the others, is corresponding to v'_{max} or v'_{min} , the absolute value of v'_{sn} is greater than v_{sn}^* in (10). On the other hand, the final pole voltage references v_{an}^* , v_{bn}^* , and v_{cn}^* are calculated by subtracting v'_{sn} from the original phase voltage references v_{as}^* , v_{bs}^* , and v_{cs}^* as in (15). From this reasoning, in this example, it is supposed that, if v'_{as} is corresponding to v'_{max} , then the final pole voltage references v_{an}^* , v_{bn}^* , and v_{cn}^* are less than the original pole voltage references

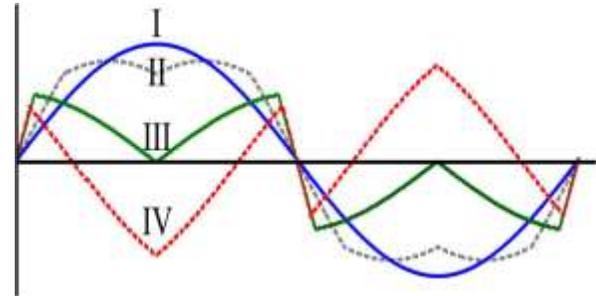


Fig. 9. Comparison of modulated waveforms. (I) Without v_{sn}^* . (II) Traditional carrier-based SVPWM. (III) Proposed NVM with $V_{dc_a} = 0.275 V_{dc}$, $V_{dc_b} = V_{dc}$, and $V_{dc_c} = V_{dc}$. (IV) Proposed NVM with $V_{dc_a} = 0.2 V_{dc}$, $V_{dc_b} = V_{dc}$, and $V_{dc_c} = V_{dc}$.

which are not considering v'_{sn} but v_{sn}^* . On the contrary, if v'_{cs} is v'_{max} , then the final pole voltage references are greater than the original pole voltage references. By using this principle, the proposed method reduces the portion of the phase whose dc-link voltage is smaller than the others and increases the utilization of the phase in which the dc-link voltage is greater than those of the other phases. However, as it can be seen in (16), v_{sn} does not affect the line-to-line voltages. Therefore, the line-to-line voltage is the same as the one derived from the original phase voltage reference. From this analysis, the proposed method enables the maximum synthesizable modulation index in the linear modulation range under the unbalanced dc-link conditions to be achieved. In addition to this, if all of the dc-link voltages are well balanced so that V_{dc_a} , V_{dc_b} , and V_{dc_c} are equal to V_{dc} .

$$V_{dc_mid} = V_{dc_min} = V_{dc}. \quad (20)$$

By substituting (20) into (12)–(14)

$$\begin{aligned} K_w &= \frac{V_{dc_mid} + V_{dc_min}}{2} = V_{dc} \\ K_{w_a} &= K_{w_b} = K_{w_c} = 1 \\ v'_{as} &= v_{as}^* \quad v'_{bs} = v_{bs}^* \quad v'_{cs} = v_{cs}^*. \end{aligned} \quad (21)$$

Equation (21) shows that the proposed method gives the same voltage references as

the traditional method under balanced dc-link conditions.

C. Constraints of the Proposed Method

In this section, the limitation of how unbalanced dc links can be while still being compensated by the proposed method is evaluated. Fig. 9 shows the modulated voltage waveforms with different modulation methods and dc-link conditions. In the figure, cases I and II show the results of traditional sinusoidal PWM (SPWM) and carrier-based SVPWM, while cases III and IV illustrate the waveforms of the proposed method with different ratios of dc-link voltages. The fundamental idea to examine the limitation of the proposed method is to evaluate what conditions bring the different polarities between the original voltage reference and the modified voltage reference by using the proposed method. In Fig. 9, the vertices at $\pi/2$ and $3\pi/2$ rad almost come in contact with, but do not cross, the zero point. However, the directions of the vertices are opposite the original phase voltage reference in case IV. This means that an excessive and unnecessary voltage is injected into the system. As a result,

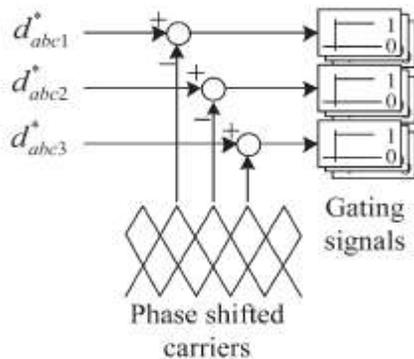


Fig. 10. Comparison of the duty references and the carriers

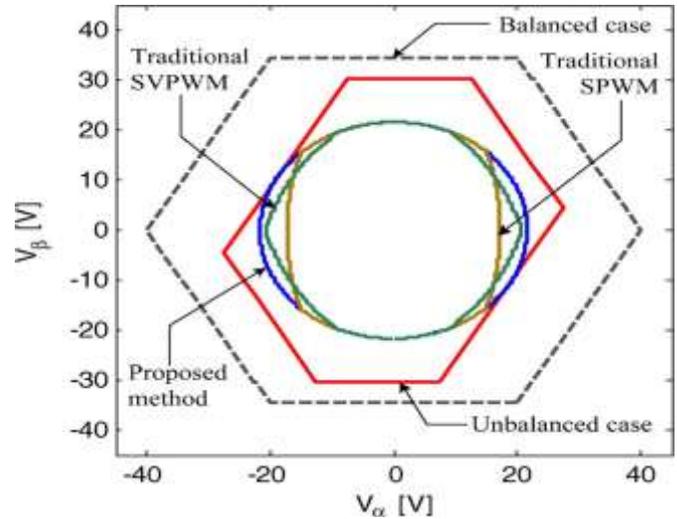


Fig. 11. Comparison of the voltage vector trajectories.

The maximum linear modulation range is reduced, and the line to line voltage may be distorted. With this basic concept, it is assumed that a phase which has the lowest dc-link voltage commands v^*_{max} and a phase which has the highest dc-link voltage commands v^*_{min} to examine a worst case situation. From (14) and (15), the following equations can be established:

$$v'_{max} = \frac{V_{dc_mid} + V_{dc_min}}{2V_{dc_min}} v^*_{max}$$

$$v'_{min} = \frac{V_{dc_mid} + V_{dc_min}}{2V_{dc_max}} v^*_{min}$$

$$v'_{sn} = \frac{v'_{max} + v'_{min}}{2} \tag{22}$$

By using (22), the pole voltage reference which is considered as the worst case is

$$v^*_{max_n} = v^*_{max} - \frac{v'_{max} + v'_{min}}{2} \tag{23}$$

By substituting (22) into (23), we have

$$v_{\max_n}^* = \left(1 - \frac{V_{dc_mid} + V_{dc_min}}{4V_{dc_min}}\right) v_{\max}^* - \frac{V_{dc_mid} + V_{dc_min}}{4V_{dc_max}} v_{\min}^* \quad (24)$$

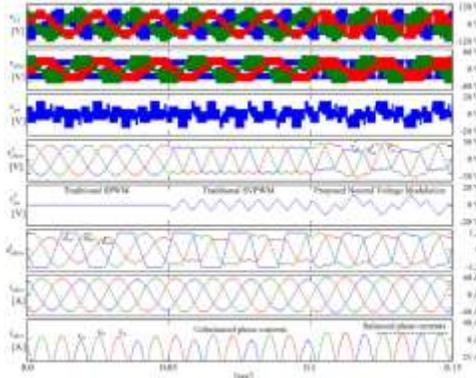


Fig. 12. Simulation result of traditional SPWM, traditional SVPWM, and the proposed method.

Unless all three-phase voltage references are not zero simultaneously, near a positive peak of the original voltage reference, the sufficient condition which guarantees the same polarity between v_{\max}^* and v_{\min}^* is established as follows:

$$v_{\max_n}^* > 0 \quad v_{\max}^* > 0 \quad v_{\min}^* < 0. \quad (25)$$

By substituting (24) into the first condition in (25), the following condition can be written:

$$k_1 v_{\max}^* > k_2 v_{\min}^* \quad k_1 = 1 - \frac{V_{dc_mid} + V_{dc_min}}{4V_{dc_min}} \\ k_2 = \frac{V_{dc_mid} + V_{dc_min}}{4V_{dc_max}} \quad (26)$$

Here, it is obvious that k_2 is always positive. Therefore, as long as k_1 is positive, the condition (26) is always satisfied, and k_1 can be rearranged as follows:

$$k_1 = \left(\frac{3V_{dc_min} - V_{dc_mid}}{4V_{dc_min}} \right). \quad (27)$$

Equation (28) is then directly obtained from (27) to ensure that k_1 will always be positive

$$V_{dc_min} > \frac{1}{3} V_{dc_mid}. \quad (28)$$

Note that (28) is a sufficient condition to meet the conditions in (25) so that the proposed method can be applied. However, even if (28) is not satisfied so that k_1 is negative, there still is a chance to apply the proposed method. To deal with this situation, let us consider the relationship between v_{\max}^* and v_{\min}^* as follows at a positive peak point:

$$v_{\max}^* = -2v_{\min}^*. \quad (29)$$

By substituting (29) into (26), we have

$$-2k_1 > k_2. \quad (30)$$

Since k_1 is negative in this case, the following condition is derived from (30);

$$|k_1| < \frac{k_2}{2}. \quad (31)$$

If the relationship between k_1 and k_2 is established as in (31), even if the provision in (28) is broken, the conditions in (25) are satisfied so that the proposed method can be still effective. Let us recall Fig. 9 again here. In the figure, the values of $|k_1|$ and $k_2/2$ for case III are evaluated as 0.1591 and 0.1593, respectively. Although the difference between the two values is very small, (31) is still true with these values. For case IV,

D. Duty Calculation

In Fig. 8, the final voltage references are entered to the duty reference calculation block. In this block, the duty references of each H-bridge module are calculated as follows:

$$d_{a1}^* = d_{a2}^* = \dots = d_{aN}^* = \frac{v_{an}^*}{V_{dc_a}}$$

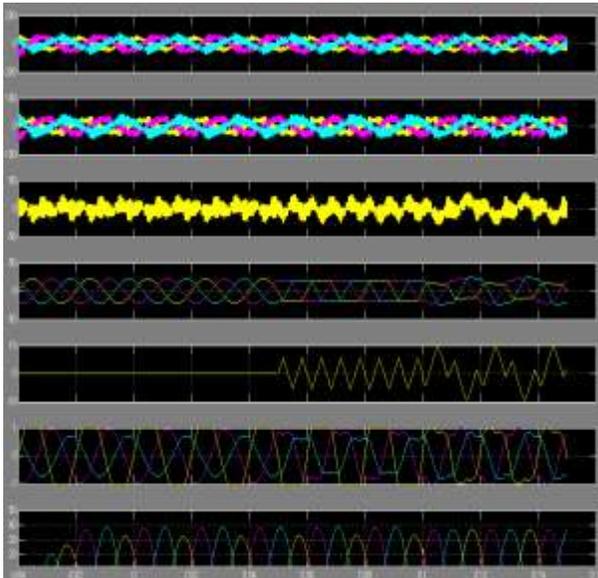
$$d_{b1}^* = d_{b2}^* = \dots = d_{bN}^* = \frac{v_{bn}^*}{V_{dc_b}}$$

$$d_{c1}^* = d_{c2}^* = \dots = d_{cN}^* = \frac{v_{cn}^*}{V_{dc_c}}.$$

(32)

The calculated duty references are compared to PS carriers to generate gating signals, as shown in Fig. 10. It should be noted that the duty references for each H-bridge in each phase are shared in the PS modulation.

IV. SIMULATION



A simple one-by-three configuration MLCI model is built in Matlab Simulink. The three-phase RL load with $R = 0.1\Omega$ and $L = 1\text{mH}$ is employed. The dc-link voltages for each phase are $V_{dc_a} = 0.5 \times 30 \text{ V}$, $V_{dc_b} = 0.75 \times 30 \text{ V}$, and $V_{dc_c} = 30 \text{ V}$. From (7), the maximum synthesizable phase voltage in linear is

$$V_{ph_max} = \frac{0.75 \times 30 + 0.5 \times 30}{\sqrt{3}} = 21.65 \text{ V}.$$

(32)

The voltage references are given by

$$v_{as}^* = V_{ph_max} \sin(100\pi t)$$

$$v_{bs}^* = V_{ph_max} \sin(100\pi t - 2\pi/3)$$

$$v_{cs}^* = V_{ph_max} \sin(100\pi t + 2\pi/3).$$

(33)

Equation (34) is applied to the modulators of the inverter in open loop. Fig. 11 compares the voltage vector spaces and the voltage trajectories in the α - β -axes of traditional SPWM, traditional SVPWM, and the proposed NVM method under the given simulation condition. Compared to the balanced dc-link case, the area of the voltage vector space is reduced under the unbalanced dc-link condition. In the figure, the traditional SPWM shows the worst voltage distortion and the minimum voltage vector space.

The traditional SVPWM gives more area than SPWM, but still, the voltage distortion is not avoidable. The proposed method shows no distortion on the output voltage and maximizes the voltage vector space compared to other methods. Fig. 12 shows the time-domain simulation results with the same simulation condition. From $t = 0.0 \text{ s}$ to $t = 0.05 \text{ s}$, traditional SPWM is used. From $t = 0.05 \text{ s}$ to $t = 0.1 \text{ s}$, traditional SVPWM is used. After $t = 0.1 \text{ s}$, the proposed method is applied. When traditional SPWM is applied, v_{sn}^* is zero, and the pole voltage references are identical to the ones in (34). With traditional SVPWM, v_{sn}^* is no longer zero, and the peak voltage of the pole voltage references is reduced compared to SPWM. However, the duty reference of phase a , where the dc-link voltage is minimum among the three phases, is saturated in both cases. Whereas with the proposed method, the fundamental frequency component of the neutral voltage is included in v_{sn}^* , and the duty references are not saturated. The benefit of the proposed method can also be observed from the peak value of the phase current in the last section of the figure. Under traditional methods, the phase currents are unbalanced. However, the phase currents are well balanced

with the proposed method. From the simulation results, it can be seen that the proposed method can synthesize the maximum available phase voltage in the linear modulation range under unbalanced dc link.

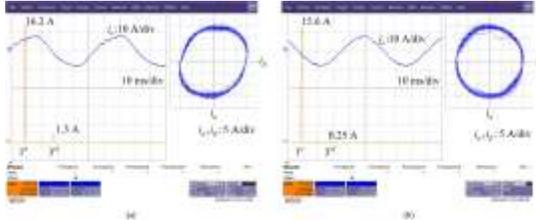


Fig. 16. Comparison of the FFT results and the current trajectories in the α - β plane. (a) Traditional carrier-based SVPWM. (b) Proposed NVM

VI. CONCLUSION

The NVM technique for MLCIs under unbalanced dc-link conditions has been proposed in this paper. In order to analyze the maximum synthesizable voltage of MLCIs, the voltage vector space has been analyzed using the switching function. From the analysis, the maximum linear modulation range was derived. The proposed NVM technique is applied to achieve the maximum modulation index in the linear modulation range under an unbalanced dc-link condition as well as to balance the output phase voltages. Compared to the previous methods, the proposed technique is easily implemented and improves the output voltage quality under unbalanced dc-link conditions. Both simulations and experimental results based on the IPM motor drive application verify the effectiveness of the proposed method.

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