International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 02
February 2017

Low-Power and Area-Efficient Shift Register Using Pulsed Latches with modified SSASPL with130nM CMOS Technology

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Abstract— This paper proposes a low-power and area-efficient shift register by using pulsed latches. The area and power consumption are reduced by replacing SSASPL (Static differential Sense Amp Shared Pulse Latch) to modified SSASPL. This method solves the timing problem between pulsed latches by replacing the usage of the conventional single pulsed clock signal to multiple non-overlap delayed pulsed clock signals. The shift register uses a small number of the pulsed clock signals by grouping the latches to N(N=4) sub shifter registers by using additional temporary storage latches. From the experiments and the results obtained it is observed that the proposed shift register is having less area and low power for an N-bit shift register. The design is implemented with 130nm technology in Tanner EDA (Electronic Design Automation) Tool. With Vdd =1.8V, Freq=200MHz.

Index Terms— Flip flop, Pulsed latch, Pulsed clock, Shift register, SSASPL.

I. INTRODUCTION

Most of the sequential circuits based devices operate without shift register unlike the digital filter, communication system, and image processing ICs. The quality of the image has increased the process of the image processor to a large with size shift register which is required. Sometimes the size of the shift register has frequently increased the power consumption. The performance of a flip-flop is based on three important timings and delays: 1) propagation delay, 2) setup time and 3) hold time. They reflect in the Flip-Flops in system level performance [2]. All SoC's(System On Chip) of digital design the flip-flop is the main stage element. These accumulate the power that is applied to the chip. So the flip-flop is one of the most power consumption element in the chip. It reduces the power consumption of the flip-flop by using the pulse signal [3].

Pulse-triggered FF (P-FF) is the popular alternative to the traditional master–slave-based FF in the applications of fast operations [4]-[7]. Besides the speed advantage, circuit simplicity is also an advantage for lowering the power consumption of the clock-based system.

Master-slave flip-flops, pulsed-triggered flip-flops, and sense amplifier based flip-flops are used in several existing microprocessors. Master-slave flip-flops consist of two stages, one is master and other is a slave and their character is classified on the hard edge trigger base [8].

The remainder of this paper is to introduce the existing system discussed in section II, problem statement discussed in section III, proposed system in section IV, simulation result in section V, and presenting the conclusion in section VI.

II. EXISTING SYSTEM

A shift register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters [9], communication receivers [10], and image processing ICs [11] - [13]. Recently, by the size of the image data continues to increase due to the high demand for high-quality image data, the word length of the shifter register increases to process large image data in image processing ICs.

An image extraction and vector generation VLSI chip uses a 4K-bit shift register [11].

A 10-bit 208 channel output LCD column driver IC uses a 2K-bit shift register [12]. A 16-megapixel CMOS image sensor uses a 45K-bit shift register [13]. As the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations.

The architecture of a shift register is quite simple. The cascaded flip-flops are to form the shift register which shares the same clock, the output of each flip-flop data is given to next flip-flop. Which a master-slave flip-flop also using two latches shares the same clock signal as shown in Fig.1 The speed of the flip-flop is less important than the area and power consumption because there is no circuit between flip-flops in the shift register. The smallest flip-flop is suitable for the shift register to reduce the area and power consumption. Recently, pulsed latches have replaced flip-flops in many applications, because a pulsed latch is much smaller than a flip-flop. But the pulsed latch cannot be used in a shift register due to the timing problem between pulsed latches.

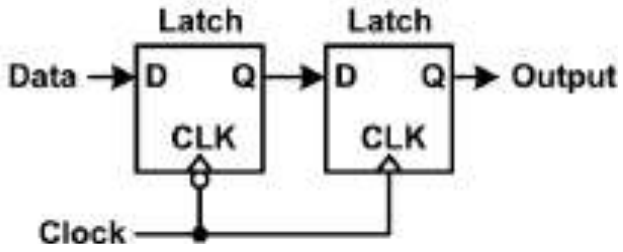

Figure 1: Master-slave flip-flop

III. PROBLEM STATEMENT

The main challenges for designing low power area efficient shift registers using latches is to optimize power & reduce the area without affecting the response or timing problem.

Solving Timing Problem**:** The pulsed latch can not be used in shift registers due to their timing problem. The shift register solves the timing problem using multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal shown in Fig.4 (a). As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches.

Reduced Area**:** Area required for Shift register using flip-flops is twice that of shift registers using latches, because a flip-flop consists of two latches.

Thus area is reduced 50% by replacing flip-flops with latches.

Reduced Power**:** Flip-flop consumes about 50% of total power because in the sequential circuit, flip-flops are replaced with latches in proposed shift register, the power is saved by using clock pulsed instead of the clock signal. Because of all these reasons, static differential sense amplifier shared pulsed latch is an attractive choice for the efficient design of shift register.

IV. PROPOSED SYSTEM

In the proposed system to change the SSASPL and reduce the power level of the shift registers. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. The pulsed latch is an attractive solution for the small area and low power consumption. The pulsed latch cannot be used in shift registers due to the timing problem, as shown in Fig. 2.

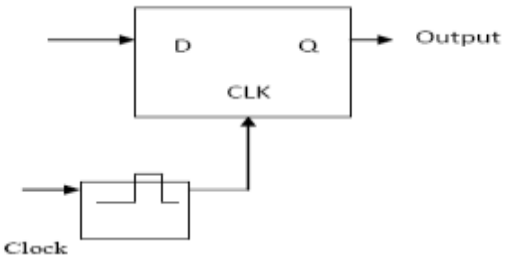

Figure 2: Pulsed latch.

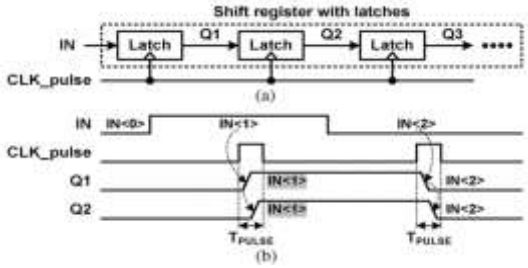

Figure 3: Shift register with latches and a pulsed clock signal.(a) Schematic.(b)Waveforms.

The shift registers in Fig. 3(a) consists of several latches and a pulsed clock signal (CLK-pulse). The operation waveforms in Fig. 3(b) show the timing problem in the shifter register. The output signal of the first latch (Q1) changes correctly because the inputs signal of the first latch (IN) is constant during the clock pulse width. But the second latch has an uncertain output signal (Q2) because its input signal (Q1) changes during the clock pulse width. One solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 4(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

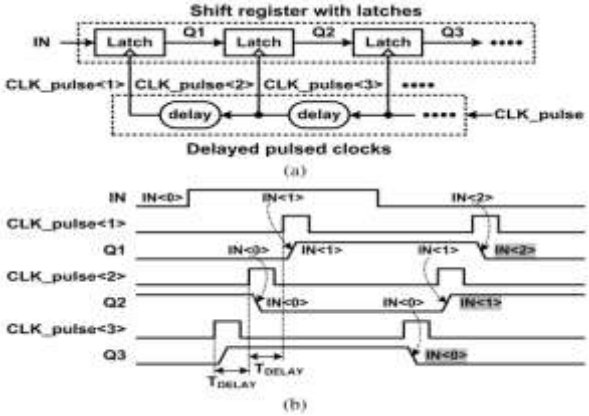

Fig. 4. Shift register with latches and delayed pulsed clock signals. (a)Schematic. (b) Waveforms.

A.CLOCK PULSE CIRCUIT

Each pulsed clock signal arrives at the sub-shift registers at different time due to the pulse skew in the wire. The pulse skew increases proportionally to the wire distance from the delayed pulsed clock generator.

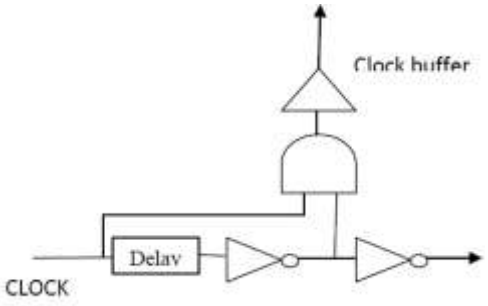

Fig.5. The clock pulse circuit

All pulsed clock signals have almost the same pulse skews when they arrive at the sub-shift register. Therefore in the sub-shift register, the pulse skew differences between the pulsed clock signals are very small. The clock pulse intervals larger than the pulse skew differences are which cancel out the effects of the pulse skew differences.

Another solution is to insert the clock buffers and clock trees to send the short clock pulse with a small wire delay. But, this increases the area and power overhead. Moreover, the multiple clock pulses make the most overhead for multiple clock buffers and clock trees. The schematic of clock pulse circuit is shown in Fig.5.

The proposed shift register reduces the number of delayed pulsed clock signals significantly, but it increases the number of latches because of the additional temporary storage latches. As shown in Fig.6 each pulsed clock signal is generated in a clock-pulse circuit consisting a delay circuit and an AND gate.

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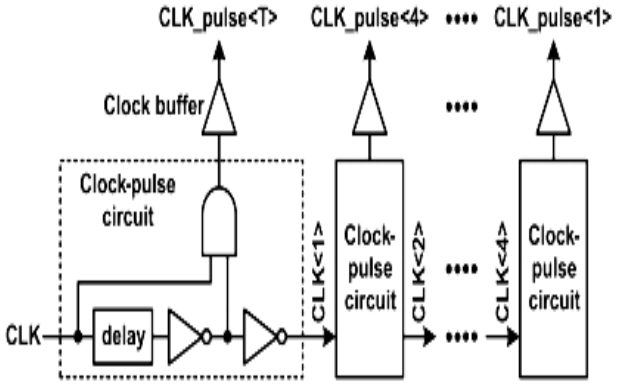


Figure 6: Delayed pulsed clock generator

In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in Fig. 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals. The numbers of latches and clock-pulse circuits change according to the word length of the sub shift register.

B. SHIFT REGISTER WITH PULSED CLOCK GENERATOR

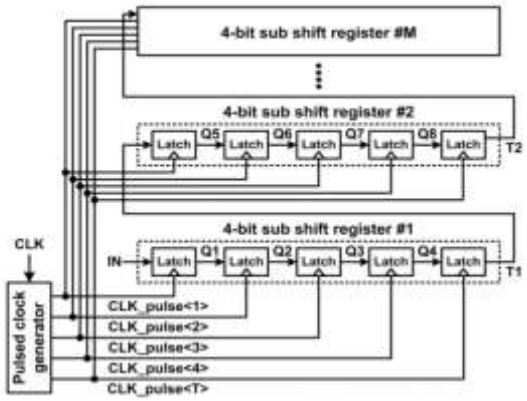


Figure 7: Proposed shift register schematic

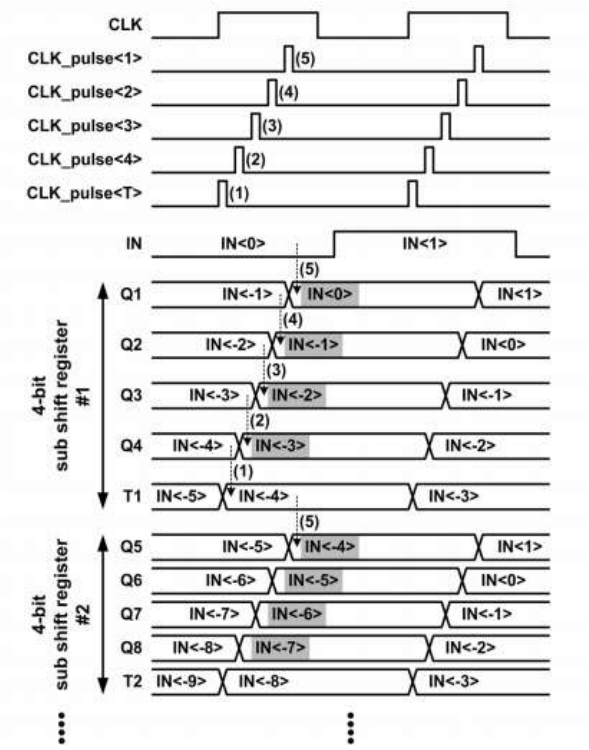


Figure 8: Proposed shift register Waveforms.

Fig. 7 shows an example of the proposed shift register. The proposed shift register is divided into N sub-shifter registers to reduce the number of delayed pulsed clock signals. A 4-bit sub-shifter register consists of five latches and it performs shift operations with five non-overlap delayed pulsed clock signals). In the 4-bit sub-shift ⟩T⟨ and CLK-pulse⟩1:4 ⟨(CLK-pulse register #1, four latches store 4-bit data (Q1-Q4) and the last latch stores 1-bit temporary data (T1) which will be stored in the first latch (Q5) of the 4-bit sub shift register #2. Fig. 8 shows the operation waveforms in the proposed shift register. Five non-overlaps delayed pulsed clock signals are generated by the delayed pulsed clock generator in Fig. 6. The sequence of the pulsed clock signals is in the opposite order of the ⟩T⟨five latches. Initially, the pulsed clock signal CLK-pulse updates the latch data T1 from Q4. And then, the pulsed clock update the four latch data from Q4 to⟩1:4⟨signals CLK-pulse Q1 sequentially. The latches Q2–Q4 receive data from their previous latches Q1–Q3 but the first latch Q1 receives data from the input of the shift register (IN). The operations of the other sub -shift registers are the same as that of the sub-shift register #1 except that the first latch receives data

from the temporary storage latch in the previous sub-shift register.

C. SSASPL-LATCH

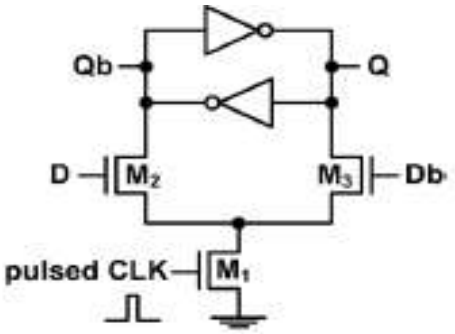


Figure 9: Schematic of the SSASPL

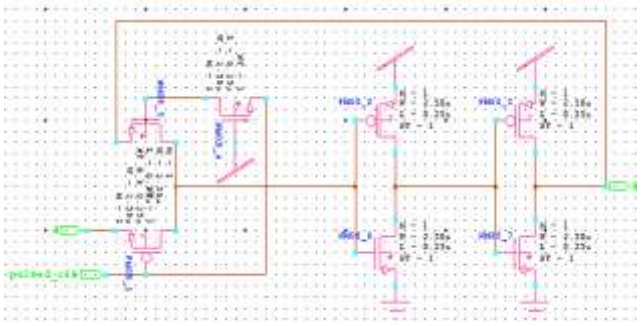


Figure 10: Schematic of the modified SSASPL

The maximum clock frequency in the conventional shift register is limited to only the delay of flip-flops because there is no delay between flip-flips. Therefore, the area and power consumption are more important than the speed for selecting the flip-flop. The proposed shift register uses latches instead of flip- flops to reduce the area and power consumption. In chip implementation, the SSASPL (static differential sense amp shared pulse latch) in Fig. 9, which is the smallest latch, is selected. The original SSASPL with 9 transistors [14] is modified to the SSASPL with 7 transistors in Fig.9 by removing an inverter to generate the complementary data input (Db) from the data input (D). In the proposed shift register, the differential data inputs (D and Db) of the latch come from the differential data outputs (Q and Qb) of the previous latch. The SSASPL uses the smallest number of transistors (7 transistors) and it consumes the lowest clock power because it has a single transistor driven by the pulsed clock signal. We are modified the SSASPL for reduction of power consumption. The modified architecture is shown in fig .10.

IV. SIMULATION RESULT

The architecture of the proposed 256bit pulse triggered shift register in 130nm CMOS technology is design and analysis the performance in the tanner EDA tools.

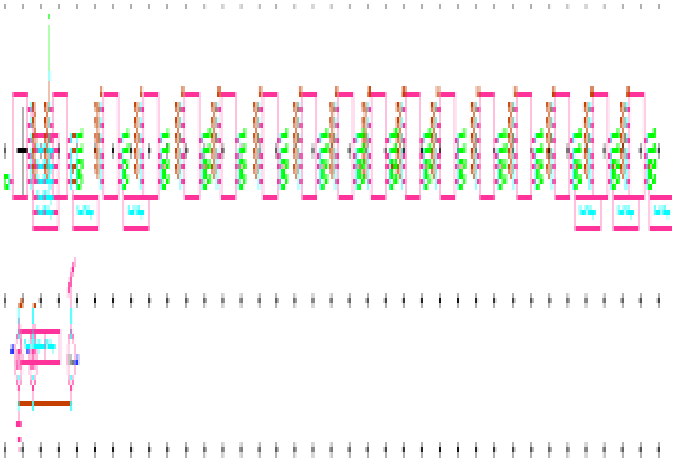


Figure11: shift register design

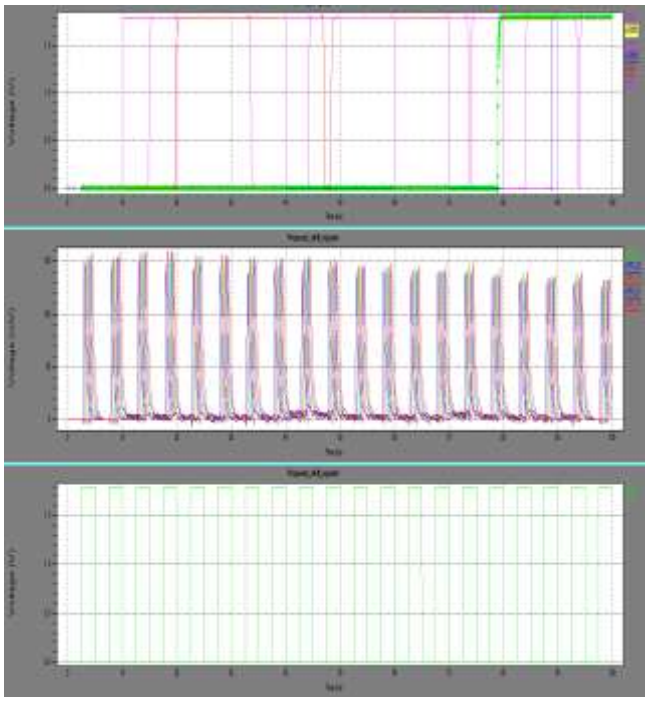
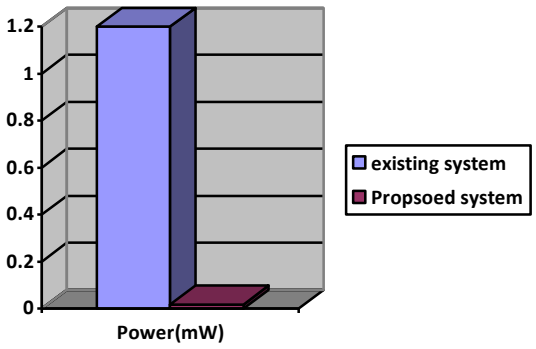


Figure12: simulation result

The architecture of the 256bit pulse triggered shift register shown in figure11.The simulation result of the 256bit pulse triggered shift register is shown in figure 12. Finally to comparison the existing system and proposed system is detailed in table 1.

Table 1: comparison

Parameters	Existing system	Proposed system
Vdd(V)	1.8	1.8
Area(nm)	180	130
power	1.2mW	0.0173mW
Type of pulsed latch	SSASPL	Modified SSASPL
Word length of shift register	256	256
Clock freq MHz	100	200
Word length of sub shift registers	4	4



GRAPH1: POWER COMPARISON BETWEEN SSASPL AND MODIFIED SSASPL

V. CONCLUSION

The proposed a low-power and area-efficient shift register using pulsed latches. The shift register reduces 27.7% area and saves 98.5% power by replacing flip-flops with pulsed latches. The timing problem between pulsed latches is solved by using multiple non-overlap delayed pulsed clock signals instead of a single pulsed clock signal.

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