Systematic Cell Design of Three-Input XOR/XNOR with Energy Efficiency

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Abstract: *In this paper, a Systematic Cell Design Methodology (SCDM) based on transmission gate in the category of hybrid-CMOS Logic style is proposed. (SCDM), which is an extension of Cell Design methodology (CDM), plays the essential role in designing efficient circuits. In this methodology, designer utilize various basic cells, including three independent inputs and two complementary outputs. XOR/XNOR circuits are proposed with high driving capability, full-balanced full-swing outputs and low number transistors of basic structure, high performance, operating at low voltages and excellent signal integrity. As an especial feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay. All simulations have been performed with TSMC 0.125-μm technology, in optimum state of the circuits from viewpoint to achieve the minimum power and delay. They also outperform their counterparts exhibiting 17%–53% reduction in power and 22%-77% reduction in delay.The simulation results demonstrate the delay, power consumption) at different supply voltages ranging from 0.8V to 1.6V.*

Index Terms: Systematic cell design methodology,three input XOR/XNOR,energy efficiency,Binary Decision Diagram

I. INTRODUCTION

Building low-power VLSI system has emerged as significant performance goal because of the fast technology in mobile communication and computation. So the designers are faced with more constraint; high speed, high throughput and at the same time, consumption of power as minimal as possible.[3]The exclusive-OR (XOR) and exclusiveNOR (XNOR) gates are the essential parts of several digital systems and are highly used in very large scale integration (VLSI) systems such as parity checkers, comparators, crypto processors

,arithmetic and logic circuits, test pattern generators, especially in Full adder module as Sum output that is 3-input XOR and so forth. In most of these systems , XOR and XNOR gates constitute a part of the critical path of the system, which significantly affects the worst-case delay and the overall performance of the system.[4].A formal design method for balanced 3-input XOR–XNOR circuits in the hybrid-CMOS logic style. Inour approach, we start with selecting a basic cell including 3-input and two outputs. Next and if necessary we apply various correction mechanisms and optimization methods to obtain balanced 3-input XOR–XNOR circuits. Accordingly and by using four basic cells, we come up with six balanced 3-input XOR–XNOR circuits. Full swing outputs impact multi-stage structured arithmetic circuit performance. Therefore, designers consider achieving full swing output operations as an important factor in the basic block design of arithmetic circuits. In addition, all of the proposed circuits whose critical path contains only two transistors have low average power consumption and delay[1]. As a consequence, most of them suffer from some different disadvantages[3].

1. They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to static power dissipation.

2. Most of them suffer from severe output signal degradation and cannot sustain low-voltage operation.

3. They predominantly have dynamic power consumption for non- balanced propagation delay inside and outside circuits, which results in glitches at the outputs

Design proposed in literature so far concentrate on creative design ideas but do not follow a systematic approach.SCDM (Systematic Cell Design Methodology), which is an extension of CDM, plays the essential role in designing efficient circuits. As an especial feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay, low VDD operations, low static power dissipation, avoids any degradation on the on the output voltage, increased the driving capability. After the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms;

and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. The rest of this report is organized as follows. The details of SCDM and the three-input XOR/XNORs as the outcome of findings are discussed in Section II. Simulation results areanalyzed in Section III. Finally, the conclusions are drawn in Section IV.

II. ELEMENTARY BASIC CELL

In this section, the methodology for three-input XOR/XNORs is presented according to the flowchart Fig.1. The design path is started by EBC systematic generation. In this step, general design goals are considered that the most distinctive ones are generating fairly balanced outputs, symmetric and power-ground-free structure, fewer transistors in the critical path, as well as sharing common sub circuit. In the remaining steps, the methodology offers opportunity to strive toward an assigned design target. Two of these steps include wisely selection of mechanisms and basic cells from PDP point of view.
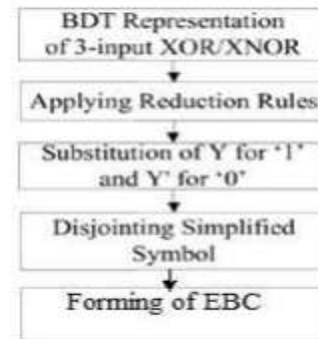

Fig 1 Flowchart for EBC

Elementary Basic Cell Systematic Generation:

In order to generate the EBC of three-input XOR/XNOR circuits,four steps are taken. Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) [8] in order to share common sub circuits. The BDT is achieved by some cascaded 2×1 MUX blocks,[10] which are denoted by simplified symbol controlled with input variables at each correspondent level. The step is followed by applying reduction rules to simplify the BDT representation. These include elimination, merging and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. Afterward, as the inputs into the first level are 0's and 1's of the

function's truth table, the 0 and 1 can be replaced by the Y and Y′ , respectively. In the process of designing balanced 3- input XOR–XNOR circuits, we face three independent inputs and two complementary outputs. The result of applying the reduction rules and the substitution and disjoining to the trees.
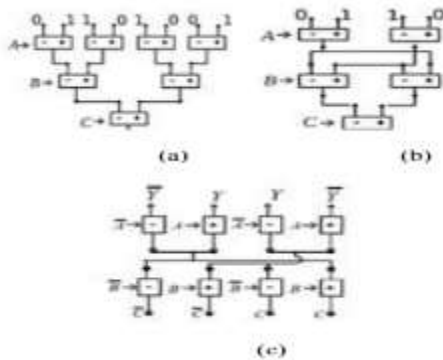

Fig 2 (a) BDT representation of three-input XOR/XNOR function.(b) Applying reduction rules. (c) substitution and disjointing.

The elementary basic cell which is extracted of minimum sum of product form of 3-input XOR– XNOR has been presented.[11] This cell has eight elements, deciding two outputs. Each element is a pass transistor or transition gate and has two input controls, i.e.,the gate and either the drain or the source. This construction simply implements

the min terms of the three-input XOR/XNOR function as shown below

$$A \oplus B \oplus C = B'. (AC' + A'C) + B. (A'C' + AC)$$

$$A \odot B \odot C = B. (AC' + A'C) + B' (A'C' + AC)$$

The input signals (applied to the two input terminals of these transistors) and the selection of pMOS, nMOS transistors This cell has eight elements, deciding two outputs.[8]We refer to the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also assume that pins of the external section G5–G8 can also be B or its complement [12].This form of the circuit (as the elementary basic cell) is power-less and ground-less (P-/G-).
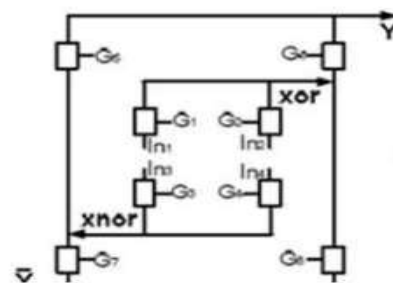

Fig 3 Representation of EBC

The EBC is formed by the above steps. This structure of EBC fig 3 is used to implement the following designs

III. SIMULATION RESULTS:

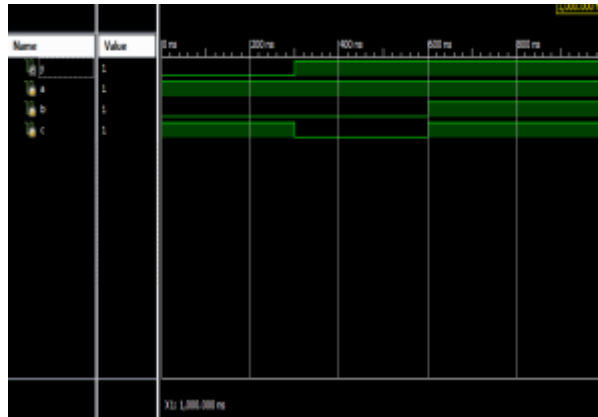The simulated output for xo4 should be shown in the below waveform.

Fig 4 Waveform of xor/xnor

IV. CONCLUSION

In the end, new high performance three-input XOR/XNOR circuits with less power consumption and delay during SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature,the critical path of the presented designs consists of only two transistors, which causes low propagation delay. On average, these circuits outperform their counterparts with 17%–53% reduction in power and 22%-77% reduction in delay respectively, in tanner simulation based on the TSMC 0.125-μm technology. Simulation results show that the proposed circuits exhibit better performances compared to previously suggested circuits. Finally, we also classify the basic cells and the mechanisms based on performances and applications.

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