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Fast Detection of Open-Switch Fault in Cascaded H-Bridge Multilevel Converter

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Abstract: Fell H-Bridge converter has as of late been used in various high-control applications because of its particular furthermore, basic structure. So as to have an adjusted many an issue event in this converter, it is important to recognize the switch issue and its area. In this paper, a quick power switch shortcoming discovery strategy is introduced to recognize the flaw and its area. One and only voltage estimation per stage is required by this technique, and the shortcoming identification is speedier contrasted with the existing techniques. In addition, it is simple for execution on an FPGA gadget, because of the utilization of basic math, social and state machine pieces. The proposed technique is confirmed by PC recreation.

Keywords: H-Bridge Converter, FPGA, PC Recreation.

I. INTRODUCTION

Multilevel converters have been used in recent years in a large number of power electronics applications. They have lots of benefits over the conventional two-level converters that make them interesting choices especially in high-power applications. In these converters, each switching device has to withstand only a portion of the total voltage. Therefore by using several devices, the converter can work with higher voltages compared to the conventional ones. Also these converters produce lower harmonics. Several types of multilevel converters are proposed and used. The most popular structures are the diode clamped, flying capacitor and the Cascaded H-Bridge (CHB) converters. However, having a large number of devices increases significantly the risk of a failure in one of the power converter switches. Therefore it is important to detect and compensate faults occurrence in these converters. Several methods are proposed for the post-fault operation of multilevel converter providing the possibility of balanced operation of the converter even after a fault. The faster the fault is detected; the smaller will be its effect on the system performances. Also using a large number of additional sensors for fault detection will in turn increase the cost and reduce the system reliability; therefore it is desired to lower the number of additional sensors as much as possible. In this paper, the cascaded H-bridge converter and open-circuit power switch fault detection are concerned. The studied converter is consisted of the cascaded connection of H-bridges in each phase. A diagram of a CHB converter is given in Fig 1.

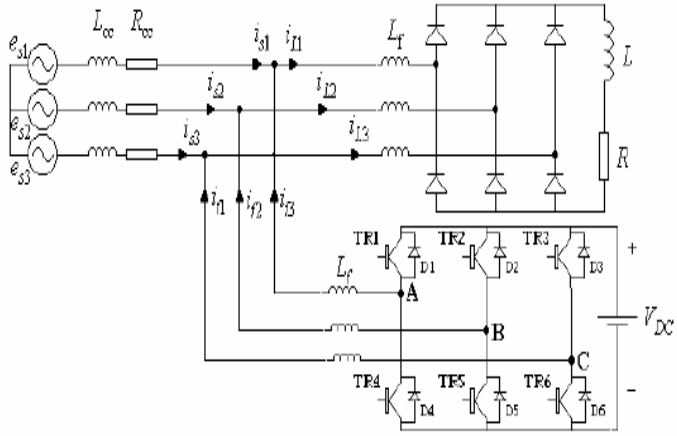

Fig.1. Classical three-leg shunt active filter topology.

II. PROPOSED MULTILEVEL CHB CONVERTER

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel converter system for a high power application. This chapter reviews state of the art of multilevel power converter technology. Fundamental multilevel converter structures and modulation paradigms are discussed including the pros and cons of each technique. Particular concentration is addressed in modern and more practical industrial applications of multilevel converters. A procedure for calculating the required ratings for the active switches, clamping diodes, and dc link capacitors including a design example are described. Finally, the possible future developments of multilevel converter technology are noted.

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A. Multilevel Power Converter Structures

As previously mentioned, three different major multilevel converter structures have been applied in industrial applications: cascaded H-bridges converter with separate dc sources, diode clamped, and flying capacitors. Before continuing discussion in this topic, it should be noted that the term multilevel converter is utilized to refer to a power electronic circuit that could operate in an inverter or rectifier mode. The multilevel inverter structures are the focus of in this chapter; however, the illustrated structures can be implemented for rectifying operation as well.

B. Cascaded H-Bridges

A single-phase structure of an m-level cascaded inverter is illustrated in Fig3. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by connecting the dc source to the ac output by different combinations of the four switches, S_1, S_2, S_3, and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_3. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by m = 2s+1, where s is the number of separate dc sources. An example phase voltage waveform for an 11-level cascaded H-bridge inverter with 5 SDCSs and 5 full bridges is shown in Figure 31.2. The phase voltage

$$v_{an} = v_{a1} + v_{a2} + v_{a3} + v_{a4} + v_{a5}.$$

$$V(\omega t) = \frac{4V_{dc}}{\pi}\sum_{n}\left[\cos(n\theta_1)+\cos(n\theta_2)+\ldots+\cos(n\theta_s)\right]\frac{\sin(n\omega t)}{n}, \quad \text{where } n = 1, 3, 5, 7, \ldots$$

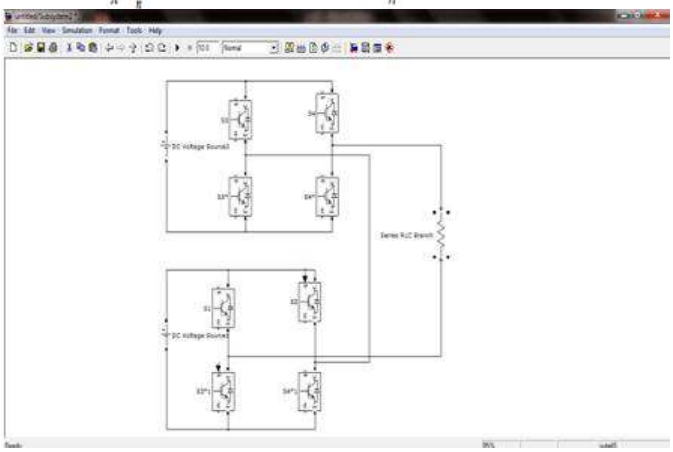

Fig.2. Proposed structure of a multilevel cascaded H-bridges inverter.

The magnitudes of the Fourier coefficients when normalized with respect to V_{dc}. Cascaded inverters have also been proposed for use as the main traction drive in electric vehicles, where several batteries or ultra capacitors are well suited to serve as SDCSs. The cascaded inverter could also serve as a rectifier/charger for the batteries of an electric vehicle while the vehicle was connected to an ac supply as shown in Fig3. Additionally, the cascade inverter can act as a rectifier in a vehicle that uses regenerative braking.

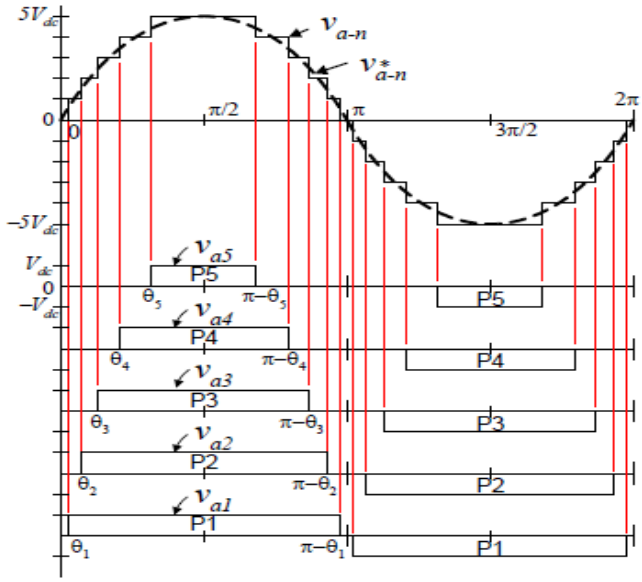

Fig3. Output phase voltage waveform of an 11-level cascade inverter with 5 separate dc sources.

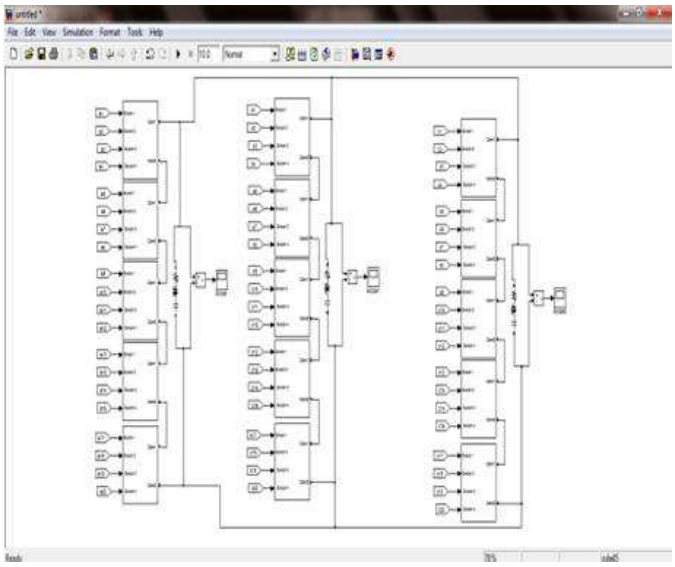

Fig4. Three-phase wye-connection structure for electric vehicle motor drive and battery charging.

Manjrekar has proposed a cascade topology that uses multiple dc levels, which instead of being identical in value are multiples of each other. He also uses a combination of fundamental frequency switching for some of the levels and PWM switching for part of the levels to achieve the output voltage waveform. This approach enables a wider diversity of output voltage magnitudes; however, it also results in unequal voltage and current ratings for each of the levels and loses the advantage of being able to use identical, modular units for each level.

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III.FAULT DETECTION ALGORITHM

Fast fault detection is mandatory in power electronics converters in order to minimize the undesirable behavior of the converter by changing the converter topology or the control method after fault detection. For DC-DC and conventional two-level converters, fast detection methods are proposed in [4, 5]. In this paper, a generalized version of those method is proposed for the CHB converter that not only detects the fault, but also can detect the faulty cell, which is necessary for the reconfiguration of the converter in order to be capable of using any of the post-fault control methods proposed in[12]. In this paper, open-circuit faults are considered. For short-circuit switch faults, normally using fast acting fuses the converter topology will become similar to that after an open-switch fault [24], or special supplementary hardware is needed to detect the fault, as the software methods are not fast enough to detect the short-circuit switch faults. Nonetheless, this is not in the scope of this paper.

A. Fault Detection

In ideal condition, an open switch fault can be easily detected by comparing the measured and estimated phase voltages of the converter. Considering a single cell (cell C) in one phase of a CHB converter as shown in Fig2, let us assume that the fault is in 51 switch. Clearly, the observations can be generalized to other swithches as well. Gate command for switch k is shown with Tk E {0, 1}, and commands for two switches in each leg are complementary. For a fault in 51, when T1T 3 = 10 and icell < 0, Dz diode will conduct instead of the 51, therefore while estimated output voltage is VDC the measured voltage will be equal to 0. If icell > ° however, the D1 diode will conduct and the converter will behave normally, so there will be no fault in the system and it cannot be detected as well. For the fault in 51, estimated and measured voltages of the cell and the error between them are resumed in Table II. It is assumed that icell < 0, therefore the fault in 51 will affect the output voltage of the cell.

Table 1. Estimated and Measured Voltages in Case of An Open Switch Fault In 51 In Cell C

T_1T_3	$V_{es,C}$	$V_{m,C}$	Error $V_{es,C}-V_{m,C}$
00	0	0	0
01	$-V_{DC}$	$-V_{DC}$	0
10	$+V_{DC}$	0	$+V_{DC}$
11	0	$-V_{DC}$	$+V_{DC}$

Since in other cells the measured and estimated voltages are equal in normal operation, the total error between measured and estimated voltages can be written as:

$$V_{es} - V_m = V_{es,C} - V_{m,C} = +V_{DC} \quad (1)$$

Therefore the fault in any of the switches can be effectively detected. However in practice, the estimated and measured voltages are always different, mostly due to measurement and discretizing errors, and more importantly because of non-ideal behaviors of the switches and the drivers, such as turn-off and turn-on delay times and dead time generated by the controllers or drivers. Therefore, to avoid false detection, separate time and voltage criteria must be adopted to account for the probable time and voltage mismatches. On the other hand, in order to make the fault tolerant control possible, not only the occurrence of a fault but also its location must be detected, Generally, it is necessary to detect the faulty cell, and bypass it to continue the operation of the converter. The proposed method is designed to account for voltage mismatches, and detect the fault and its location very quickly. First the estimated voltage is produced using the gate commands of the switches and DC voltages of the cells. Then, error between estimated and measured voltages is calculated, Fault is detected by evaluating this error, using two levels of mismatch compensation for voltage and time, as discussed before, First, two comparators check if the voltage error amplitude is large enough. If the voltage error is larger than Cv or smaller than -Cv, output of these comparators become' I', As it is previously seen, a fault will induce a voltage error equal to ±Voc , therefore choosing Cv = VoelZ seems very reasonable for voltage mismatch compensation.

Assuming that the fault detection algorithm operates with a 500 kHz clock, a moving sum is then performed for 15 sampling periods (equal to a window length of 30 J-ls) on these outputs to see on how many samples the voltage error has been considerable. Moving sum, also known as the running sum, is the simplest form of a Finite Impulse Response (FIR) filter, and is defmed as the sum of element over a moving window of values with length N, as shown in equation (2).

$$y(n) = x(n) + x(n-1) + \cdots + x(n-N+1) \quad (2)$$

Here, the moving sum shows in how many of the last observed samples (the observation window), the input has been equal to one. The outputs of the moving sum blocks then are investigated and if they are larger than Ct then one can be sure that a fault has occurred somewhere in the circuit. Since the observation window considers 15 values, Ct is chosen equal to 12.

B. Fault Location Identification

After fault detection, it is necessary to detect the fault location as well. Here, a simple yet effective method is used based on the fact that when the command of the faulty switch goes back to zero, the voltage error will also disappear, because the converter will act normally again, The third comparison and moving sum unit detect the fault removal, and signal it to the fault detection state machine (FDSM). As it is visible in Fig. 4, when the error voltage is less than Cv and larger than -Cv for at least Ct samples, one can be sure that there is no fault in the system, and the Fault Jemoved input of the FDSM wi II become equal to l. The FDSM is shown in Fig5. If a fault is already detected, one of the Fault""positive or Fault negative states in FDSM are active, and the SM is waitU;-g for the Fault removal signal (FaultJemoved) to arrive, When this signal arrives, it is only necessary to investigate in which cell(s) a switching is occurred in the previous Ct samples. This is done with the help of DiP and

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Din signals, 1 for each cell, these signals basically show if that in the last Ct sampling a switching is commanded that increase or decrease the cell's output voltage. Fig, 6 shows the DiP and Din generation for one cell. Basically a switching in S1 or S4 will tend to increase the output voltage by VDC while a switching in S2 or S3 will decrease it by VDC' If the error has been positive and the fault removal signal arrives, it can be concluded that a decreasing switching has been occurred, which corresponds to one Din signal going high.

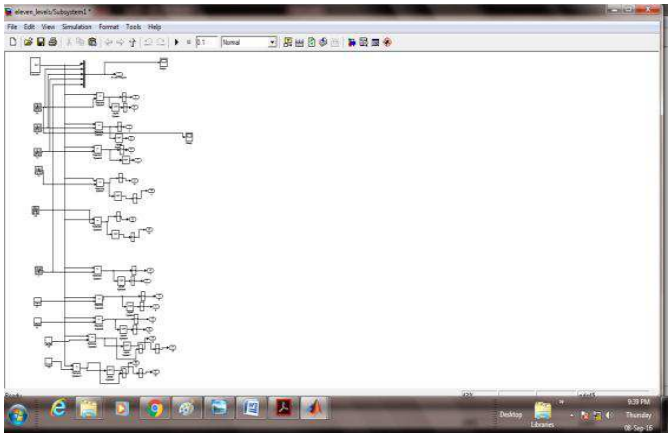

Fig5. Proposed fault detection scheme for CHB converter.

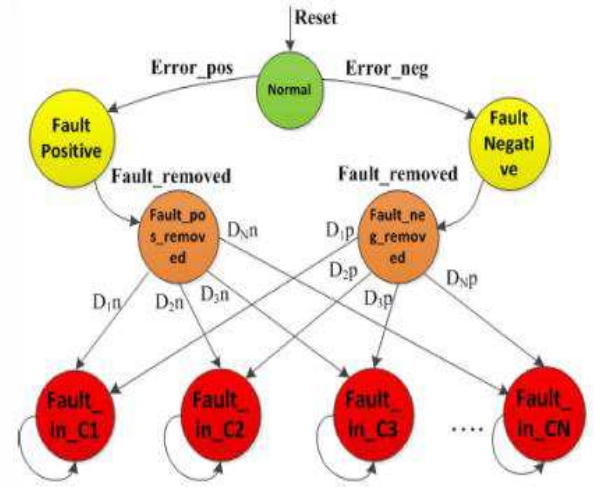

Fig6. Fault detection State machine.

Based on the Din signals, the next state in the FDSM can be detected. For a negative error similar reasoning applies. The FDSM stays in the faulty states (FauIUn_Ci , i E {1: N}) upon entering them, as long as a reset signal is not applied output voltage by VDC while a switching in S2 or S3 will decrease it by VDC' If the error has been positive and the fault removal signal arrives, it can be concluded that a decreasing switching has been occurred, which corresponds to one Din signal going high. Based on the Din signals, the next state in the FDSM can be detected. For a negative error similar reasoning applies. The FDSM stays in the faulty states (FauIUn_Ci , i E {1: N}) upon entering them, as long as a reset signal is not applied. Finally, the FaulUn_Ci outputs go high when the corresponding state is active. These outputs may be used in the fault tolerant scheme, to reconfigure the structure and control appropriately. In Fig. 4, their information is combined to determine the faulty cell's number. It is worth mentioning that after reconfiguration, the FDSM can be reset, and fault detection will be again possible for other switches, as long as the necessary changes in the calculation of the estimated voltage are applied. One special condition is particularly interesting, when two switchings have occurred in two legs during the last Ct sampling periods, because it is important to detect which one has been responsible for fault removal.

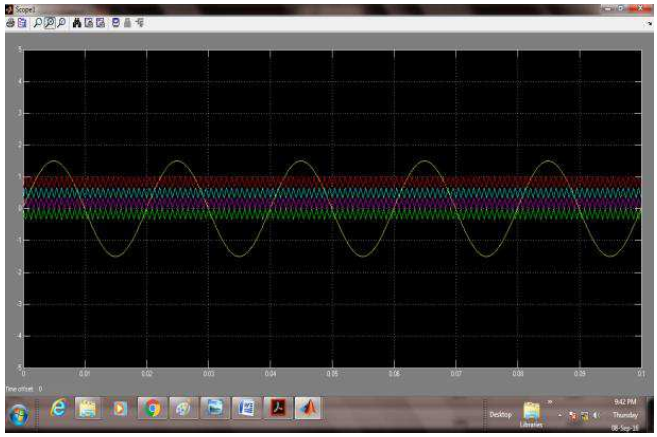

Fig7. Generation of 3 phase fault detection voltages.

In another words, it is important that in the observation window, only one DiP and Din are present, otherwise the FDST cannot decide between two DiP or Din signals. Fig. 7 shows an example of such condition for a Phase Shifted PWM (PSPWM). Referring to Fig. 3, it can be verified that when a carrier becomes larger than the modulation signal, voltage of the corresponding cell will experience a +VDC change (rising level) and vice versa. The modulation signal frequency is several times smaller than the carrier frequency, therefore it can be visually confirmed in Fig. 7 that the minimum time between two +VDC or two –VDc transitions it equal to

$$T_{min} \cong 1/2Nf_s$$

If this minimum time is a larger than the sampling window, the fault detection algorithm can will see only one positive or negative transition, and therefore it can detect the fault effectively. Normally, this minimum time is at least several times larger than the length of sampling window. Here, a conservatively large window time of Twindow = 30/-ls is used, in accordance with the value for experimental setups reported in [25], therefore if T min> 30/-lS the FDA can work correctly. For a 5-cell converter, this translates to switching frequency calculated as below:

$$f_s < \frac{1}{2*5*30\mu s} = 3333\ Hz$$

Normally the switching frequency is well beyond this limit, even with the conservative choice of Twindow in this study.

IV.SIMULATION RESULTS

Simulations are carried out to evaluate the effectiveness of the proposed method. Simulations are performed in the MATLAB/Simulink environment. A five-cell (II-level) three-phase CHB converter is simulated. DC-link voltages of the

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cells are equal to 1/00 V. The fundamental switching frequency is equal to 1000 Hz, resulting in a 2 * n * i = 2 * 5 * 1000 = 10 (kHz) equivalent switching frequency. We consider an open-loop control of the converter and using PSPWM, it generates a sinusoidal voltage at the converter's output. A fault is introduced in switch Sl of cell 2 at t=O.035s. The fault detection algorithm operates with a 500 kHz clock. As soon as the estimated and measured voltages are different, based on the sign of the voltage error, the MS positive or MS negative (ref. Fig. 4) signals will start to increase, and when one of them becomes greater than 12, the fault is detected and one of the Faulty Positive or Faulty negative states will become active.

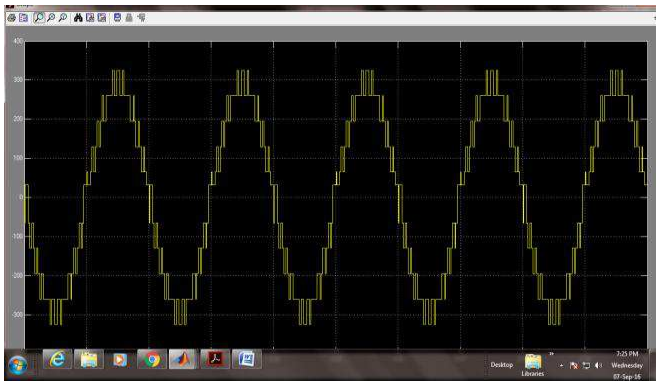

Fig8. Estimated and measured phase voltages.

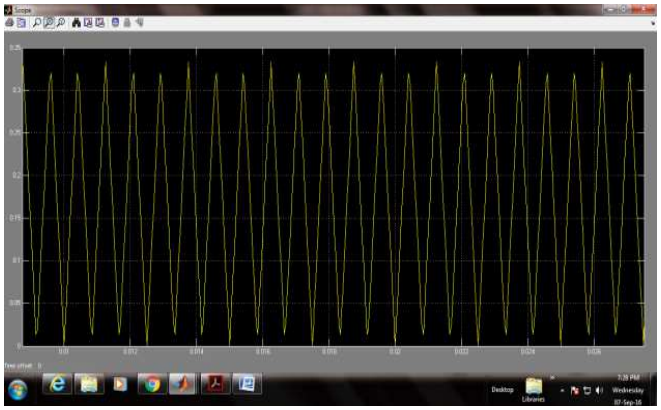

Fig9. Output of the gating pulses CHB converter.

Here, the estimated and measured voltages of the faulty phase are shown in Fig. 8. The voltage error is shown in Fig. 9. As it was expected, a fault in Sl has resulted in a +VDC error in phase voltage. It is also shown in this figure that in certain periods of time, the voltage error disappears. This is due to a decreasing switching command, and is used for identification of the fault's location. Outputs of the Moving Sum I and Moving Sum 3 blocks are shown in Fig. 10. MS Positive signal starts to increase when a large enough positive voltage error exists. When it passes Ct = 12, a fault can be declared, and the FDSM goes to the Fault positive state. MS Fault removed signal starts to increase when the converter is acting normal or when the voltage error is smaller than its limits. It can be seen that during normal operation of the converter, this signal has a usually high value, but immediately after the fault occurrence at t=0.035, it goes down to zero. However, when the fault is removed due to switching in the faulty cell, this signal goes high again. Fig. 11 shows the moment that the FDSM has reached its final stage, as well as the fmal result. Fault location is correctly detected. Also the fault detection has been very fast. The fault is detected in less than 2001lS.

Fig10. Detection of fault location in CHB (current wave forms).

V.CONCLUSION

In this paper, a very fast method for detection of open-switch faults in cascaded H-bridge converters is proposed. This method only needs one voltage measurement per phase, and is fast and robust for the detection of semiconductor open-switch fault and its location. The proposed method detects the fault by comparing the estimated and measured phase voltages of the converter. Fault location is found based on the fact that when the faulty switch command is equal to zero, converter will act normal again. Only simple math, relational and state machine blocks are used and therefore the implementation of this approach on a digital target like FPGA will be easy. The detection time will be at maximum equal to one switching period and can be as low as a few tens of microseconds. Simulation results show the high performance of the proposed method.

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