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Design and Implementing of combinational circuits using BIST for FPGAs

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Abstract— *Very Large Scale Integration (VLSI) has made an extraordinary effect on the development of integrated circuit technology. It has not only decreased the dimension and the price but also improved the complexness of the circuits. There are, however, prospective issues which may slow down the efficient use and development of upcoming VLSI technology. Among these is the issue of circuit testing, which becomes progressively challenging as the range of integration grows. Because of the high device counts and restricted input/output accessibility that define VLSI circuit, conventional testing techniques are often worthless and inadequate for VLSI circuit. Built-in self-test (BIST) is a commonly used design technique that allows a circuit to test itself. In this paper BIST architecture is implemented for testing of various faulty circuits.*

Keywords— VLSI, BIST, Faulty Circuits

I. INTRODUCTION

BIST (Built-In Self-Test) for random logic is becoming an eye-catching substitute in IC testing, although logic BIST is a recent subject which is under research over more than 3 decades. This paper provides the use of a deterministic logic BIST structure upon state-of-the-art industrial circuits. Nevertheless, new innovations throughout deep-submicron IC process engineering as well as core-based IC design and design engineering will surely lead to more popular using logical BIST due to the fact outer assessment is actually becoming a lot more difficult as well as high-priced. Logic built-in self-test (BIST) depend on the fundamental design for test methodology.

For any testing methodology, the following factors should be considered- high and easily verifiable fault coverage, minimum test pattern generation, minimum performance degradation, at-speed testing, short testing time, and reasonable hardware overhead [1]. Logic Built-In Self-Test

(BIST) provides a feasible solution to the above demands. First, BIST significantly reduces off-chip communication to overcome the bottleneck caused by the limited input/output access. Further, it eliminates much of the test pattern generation and simulation process [1]. Testing time can be shortened by testing multiple units simultaneously through test scheduling. Hardware overhead can be minimized by careful design and through the sharing of test hardware. In the modern System-on-Chip (SoC) design, many cores are integrated into a single chip. Some of them are embedded, and cannot be accessed directly from the outside of the chip. Such SoC designs make the test of these embedded cores a great challenge [2]. BIST is one of the most popular test solutions to test the embedded cores. Since more and more transistors are integrated on a single IC, the amount of test vectors to test such large ICs is increasing. This requires large memories in external test equipment. In addition, a significant increase is predicted.

Originally, the predominant compelling purpose for the adopting of BIST was the need to execute in-field examining. Just lately, there have been developing desires for BIST as it may lower the price of manufacturing test together with strengthen the standard of the particular test by providing at-speed testing ability. In BIST, pseudorandomstyles tend to be generated on chip; the actual replies tend to be compacted about chip, as well as the handle impulses tend to be pushed simply by an on-chip controller. The amount of examination files exchanged with the tester is consequently considerably lowered. In addition, the scan cells are configured into a large number of relatively short scan chains, thus reducing the time required to apply a single test pattern. The low memory and performance requirements on the tester allow the usage of very low cost testers for manufacturing test of designs with logic BIST.

II. METHODOLOGY:

Linear Feedback Shift Register:

LFSR is an n-bit shift register which pseudo randomly scrolls between 2n-1 values, but does it very quickly because there is minimal combinational logic involve [1]. The all zeros case is not possible in this type of LFSR, but the probability of any bit being "1" or "0" is 50% except for that. Therefore, the sequence is pseudorandom in the sense that the probability of a "1" or "0" is approximately 50%, but the sequence is repeatable. Like a binary counter, all 2n - 1 states are generated, but in a “random” order that is repeatable. The exclusive-OR gates and shift register act to produce a pseudorandom binary sequence (PRBS) at each of the flip-flop outputs. By correctly choosing the points at which we take the feedback from an n -bit shift register we can produce a PRBS of length 2n – 1, a

maximal-length sequence that includes all possible patterns (or vectors) of n bits, excluding the allzeros pattern. In an LFSR, the bits contained in selected positions in the shift register are combined in some sort of function and the result is fed back into the register's input bit. Fig.1 shows a 3bit LFSR.

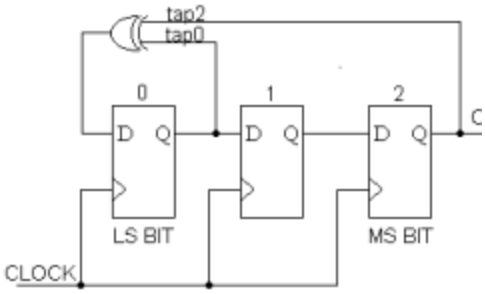

Fig.1: 3 bit maximal-length LFSR

The feedback is done so as to make the system more stable and free from errors. Specific taps are taken from the tapping points and then by using the XOR operation on them they are feedback into the registers.

Signature Analysis:

Signature Analysis is a compression technique based on the concept of cyclic redundancy checking [2]. The good and faulty circuits produce different signatures. Test Patterns for BIST can be generated at-speed by an LFSR with only a clock input. The outputs of the circuit under-test must be compared to the known good response. In general, collecting each output response and off-loading it from the circuit under test for comparison is too inefficient to be practical. The general solution is to compress the entire output stream into a single signature value

SISR - Single-Input Signature Register:

A serial-input signature register can only be used to test logic with a single output. There are several ways to connect the inputs of LFSRs to form an SISR. Since the XOR operation is linear and associative, $(A \oplus B) \oplus C = A \oplus (B \oplus C)$, as long as the result of the additions are the same then the different representations are equivalent. If we have an n -bit long SISR we can accommodate up to n inputs to form the signature. If we use $m < n$ inputs we do not need the extra XOR gates in the last $n - m$ positions of the SISR. SISR reduce the amount of hardware required to compress a multiple bit stream. LFSR and/or SISR circuit is implemented using a memory already existing in a circuit to be tested. If we apply a binary input sequence to LFSR, the shift register will perform data compaction (or compression) on the input sequence. At the end of the input sequence the shift-register contents, Q0, Q1, and Q2, will form a pattern that we call a signature. If the input sequence and the serial-input signature register (SISR) are long enough, it is unlikely (though possible) that two different input sequences will produce the same signature. If the input sequence comes from logic that we wish to test, a fault in the logic will cause the input sequence to change. This causes the signature to change from a known good value and we shall then

know that the circuit under test is bad. This technique, called signature analysis, was developed by Hewlett-Packard to test equipment in the field in the late 1970s. The simplest form of this technique is based on a single input LFSR.

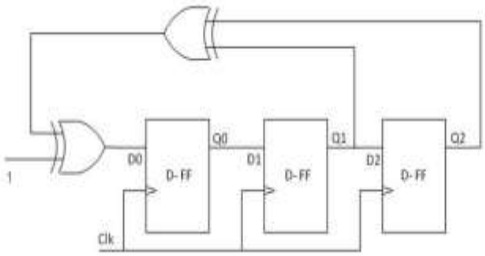

Fig3: 3 bit Single-input signature register (SISR)

Every LFSR has a characteristic polynomial that describes its behavior. Degree of polynomial is given by the number of shift registers.

III. PROPOSED DESIGN METHODOLOGY

In this paper circuit under test is a combinational circuit show in the figure 3. The different types of test carried are with respect to Stuck-at fault. It means that the fault is modeled by assigning a fixed (0 or 1) value to a single line in the circuit (in this case 1st NAND gate). A single line is an input or an output of a logic gate or a flip-flop. Stuck-at fault can be derived into two parts one is single stuck-at fault another one is multiple stuck-at faults, a stuck-at fault is assumed to affect only the interconnection between gates. However, multiple fault diagnosis becomes increasing difficulty and time-consuming as the size of integrated circuit increases. Many of methods have been introduced for diagnosing and deducing fault locations multiple faults in combinational circuit such as effect-cause analysis, guided probing, analysis by forward propagation and backward implication using randomly generated input-pairs[8], analysis and diagnosis using both electron beam and LSI tester. We have proposed methods to deduce suspected faults by algorithmically-generated sensitizing input-pairs without probing internal lines. To reduce the number of suspected faults, single and multiple fault simulation with diagnostic tests that lead to fault-free responses are used to identify non existent faults. To avoid missing actual faults in a fault circuit the proposed method uses the result of multiple fault simulation to diagnose multiple stuck-at faults. On the assumption that all suspected faults are equally likely in the faulty circuit, multiple faults simulations are performed.

A Single-Input Signature Register (SISR) has been designed for this project. There are several ways to connect the inputs of LFSRs to form an SISR. Since the XOR operation is linear and associative, (A Xor B) Xor C = A Xor (B Xor C), as long as the result of the additions are the same then the different representations are equivalent. If we have an n -bit long SISR we can accommodate up to n inputs to form the signature. If we use m < n inputs we do not need the extra XOR gates in the last n – m positions of the SISR. SISR

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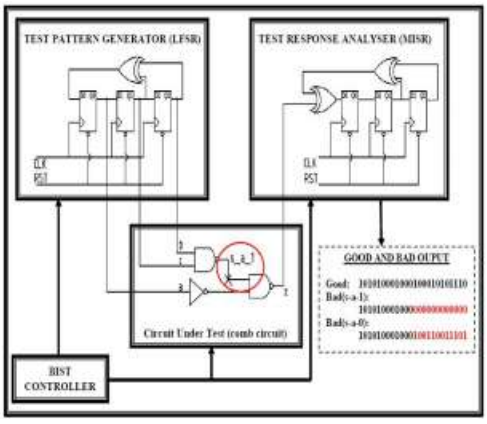

Fig4:Circuit diagram of proposed BIST Architecture

IV. RESULTS AND DISCUSSION

In this paper BIST architecture has been designed for combinational circuit using Xilinx ISE 14.2 tool and vivado 2015.2 and implemented on zynq board.

First the 3-bit LFSR simulation result using XILINX 14.2 tool and vivado 2015.2 tool is observed by applying input signals Clock and Reset. 23 random pattern sequences are generated at the output signal. Then MISR simulation result using XILINX 14.2 tool is evaluated by inputting signals Clock, Reset and data_in (output signal from CUT for BIST design). 23 random pattern sequences are generated at the output signal.

Simulation Results of vivado :

Interpretation : For input clk = 0 and en = 1

and the output y = 010

Fig.5: Top Module Simulation

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Design	PARAMETERS	
	Slices(LUTs)(Area)	Power
Conventional (Xilinx)	6	0.839w
Proposed (vivado)	3	1.042w

Top Module RTL Schematic:

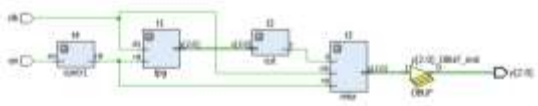

Fig.6: RTL Schematic of Top Module

Synthesis Design:

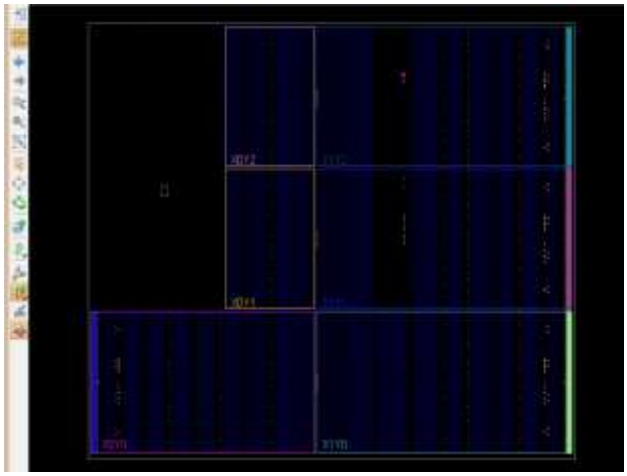

Fig.7: Synthesis Design of Top Module

Vivado output :

Fig.8: Implementation of Top Module on a Zynq Board

Utilization Report :

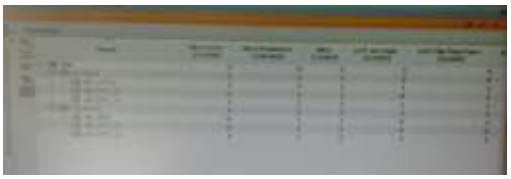

Fig.9: LUTs Report

Fig.10: Power Report

CONCLUSION:

In this paper BIST architecture has been designed for combinational circuit using an Xilinx ISE 14.2 tool and vivado 2015.2 tool and implemented on a zynq board.. Memory usage, Delay time reductions because of BIST design into CUT with fault and without fault are designed. Memory usage with BIST consumes lesser area when we compare with CUT with/without fault. Delay time without BIST takes longer time to complete execution of required result. By seeing these little variations in parameters justifies the BIST technique for combinational circuit will not affect the area overhead, memory issues and power consumption.

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