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Hybrid Multicarrier Modulation to Reduce Leakage Current in a Transformerless Cascaded Multilevel Inverter for Photovoltaic Systems

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***Abstract*—This letter proposes a hybrid multicarrier pulse width modulation (H-MCPWM) technique to reduce leakage current in a transformerless cascaded multilevel inverter for photovoltaic (PV) systems. The transformerless PV inverter topology has the advantages of simple structure, low weight and provides higher efficiency. However, the topology makes a path for leakage current to flow through parasitic capacitance formed between the PV module and the ground. A modulation technique has significant impact to reduce the leakage current without adding any extra component. The proposed H-MCPWM technique ensures low leakage current in the transformerless PV inverter system with simplicity in implementation of the modulation technique using lesser number of carriers. Experimental prototype developed in the laboratory demonstrates the performance of the proposed modulation technique in reducing the leakage current.**

***Index Terms*—Cascaded H-bridge multilevel inverter, hybrid multicarrier pulse width modulation (H-MCPWM), leakage current reduction, transformerless photovoltaic (PV) system.**

I. INTRODUCTION

THE total power generation from the photovoltaic (PV) system is relatively small as compared to other common energy resources due to its high installation cost. Reducing the PV system cost and increasing its efficiency have attained greater research interest. One of the solutions to reduce the cost of the PV power system is to remove transformer required in the output of the PV inverter [1]–[3]. Most of the national elec- tricity regulatory authority made it compulsory to use trans- former above certain threshold power in the system because it ensures galvanic isolation. However, the use of transform- ers increases weight, size,

The commercial transformerless centralized PV inverter has been successfully connected in roof-top projects with ratings above 10 MW and it is recognized by IEEE 1547 and other standards. This encourages the possibility to use transformer- less inverter topology for high-power applications [13]. Next- generation PV inverter has reached higher power ratings with modularity, and redundant topologies will be adopted in the design for reliability of the inverter. This use of cascaded H-bridge multilevel inverter opens up the option to eliminate the transformer from the PV system. In general, following two well-established modulation techniques are available for the multilevel inverter topologies which provide constant common mode voltage: space vector modulation (SVM) and multicarrier pulse width modulation (MCPWM). The SVM technique is more constructive from the view of switching timings. The switching sequence and modula- tion can be decided by the users, but it requires regress effort for implementation [15]–[18]. In [19], the author has demonstrated the use of SVM to reduce the leakage current in transformer- less PV inverter topology by placing zero active vectors at ap- propriate switching instants. However, selection of switching states is not easy for practical implementation.

In [21], the authors have reported the effect of common mode voltage using bipolar and unipolar modulation schemes on the neutral point clamped multilevel inverter and cascaded H-bridge multilevel inverter. As the level of cascaded H-bridge multilevel inverter increases, it is expected to get reduction in leakage current, and further studies are required to know the relation

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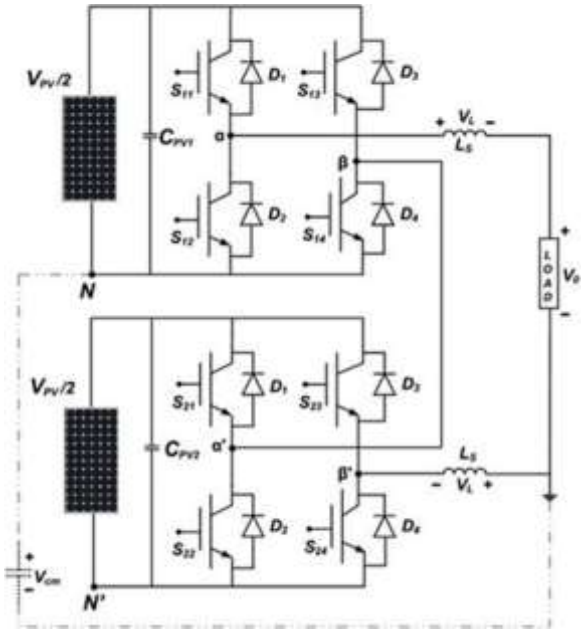


Fig. 1. PV-supported transformerless single-phase five-level cascaded multilevel inverter.

between the modulation strategy and the leakage current. The cascaded H-bridge multilevel inverter has the advantages of less leakage current as compared to the conventional single H-bridge inverter due to reduced value of dc-link voltage per bridge. The common multicarrier modulation techniques used in the transformerless cascaded H-bridge multilevel PV inverter topologies introduce common mode voltage.

II. be written from Fig. 1:

$$V_{cm} + V_{\alpha N} - V_L - V_O = 0 \quad (2)$$

COMMON MODE VOLTAGE

Fig. 1 shows the PV-supported single-phase five-level cascaded H-bridge inverter topology, where two H-bridges are connected in cascade and provides a common output. The configuration of two cascaded H-bridges adds the output voltage of the upper and lower bridges to generate five-level stepped output voltage at the ac side, i.e., V_{PV} , $V_{PV}/2$, 0, $-V_{PV}/2$, and $-V_{PV}$. It is assumed that the grid does not contribute common mode voltage in the system [9]. The converter topology and modulation method have significant contribution in leakage current generation. Therefore, the transformerless cascaded multilevel inverter shown in Fig. 1 is connected to a simple resistive load for evaluation of the proposed modulation technique. The leakage current is generated in the parasitic capacitance formed between the PV module and the ground, where common mode voltage is also induced at the same point as shown in Fig. 1. The common mode voltage of any electrical circuit is the mean value of voltage between the outputs and a common reference point.

The negative terminal of the dc bus, i.e., terminal *N* is called here as common reference point for upper H-bridge inverter. Similarly, for lower H-bridge inverter, N' is the common reference point. The parasitic capacitance formed for the lower H-bridge and upper H-bridge is assumed to be the same, because both the H-bridges are supplied from the similar rated PV modules [11]. The common mode voltage (CMV) and leakage current in the two H-bridges are also same; hence, the capacitive currents flow from point *N* to ground and N' to ground is considered equal. The common mode voltage V_{cm} for the upper full-bridge (H-bridge) inverter is defined as follows [3]:

$$V_{cm} = \frac{V_{\alpha N} + V_{\beta N}}{2} \quad (1)$$

$$V_{cm} + V_{\beta N} + V_L - V_{\alpha'\beta'} = 0. \quad (3)$$

The output voltage V_o has little effect on parasitic capacitance and hence it is neglected. It is assumed that the filter inductance L_s is considered the same in the two H-bridges for simplicity of the analysis and hence the voltage drop V_L due to the inductance L_s in the two H-bridges is also assumed equal [3]. The expression of the common mode voltage can be obtained in (4) by adding (2) and (3) as follows:

$$2V_{cm} + V_{\beta N} + V_{\alpha N} - V_{\alpha'\beta'} = 0. \quad (4)$$

Using (4), the common mode voltage can be expressed as follows:

$$V_{cm} = \frac{V_{\alpha'\beta'} - V_{\alpha N} - V_{\beta N}}{2}. \quad (5)$$

Now considering convention that the leakage current will flow from PV module to ground or vice versa as per the standards IEEE 80 [22], the sign of common mode voltage can be reversed as $V'_{cm} = -V_{cm}$ and abbreviated now onward as CMV in this paper. Equation (5) is useful for determining the common mode voltage in various intervals of the reference period.

To minimize the leakage current flow through the parasitic capacitance, the common mode voltage is required to be maintained minimum during the switching instances. The minimum step value of the common mode voltage is defined by $V_{PV}/(n-1)$ in the MCPWM technique [18]. In phase

TABLE I
SWITCHING INSTANTS OF THE H-MCPWM TECHNIQUE FOR CONSTANT COMMON MODE VOLTAGE

Logic conditions	*Switches on upper H-bridge*				*Switches on lower H-bridge*				*Common mode voltage*
Mode-1: (0 to *T*/2)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	V'_{cm}
$V_{c1} > V_{ref} < V_{c2}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c1} > V_{ref} > V_{c2}$	0	1	0	1	0	0	1	1	$V_{PV}/4$
$V_{c1} < V_{ref} > V_{c2}$	0	0	1	1	0	0	1	1	$2V_{PV}/4$
Mode-2: (*T*/2 to *T*)	S_{11}	S_{14}	S_{13}	S_{12}	S_{21}	S_{24}	S_{23}	S_{22}	–
$V_{c2} > V_{ref} < V_{c1}$	1	1	0	0	0	0	1	1	$2V_{PV}/4$
$V_{c2} > V_{ref} > V_{c1}$	1	1	0	0	1	0	1	0	$V_{PV}/4$
$V_{c2} < V_{ref} > V_{c1}$	1	1	0	0	1	1	0	0	0

disposition multicarrier pulse width modulation (PD-MCPWM), the common mode V'_{cm} varies in the band range of $\pm V_{PV}/2$. However, in this modulation method, total $(n-1)$ number of carrier signals are used, where n is the inverter level. The proposed H-MCPWM is the modified version of the phase opposite disposition (POD) pulse width modulation technique, where the number of carriers required is half of that required in POD PWM and therefore computational burden is reduced. In this modulation method, the carrier signals used are in-phase with each other. The phase of all the carriers is shifted by 180° after each half-cycle. Table I shows the different switching instants and their corresponding magnitude of CMV. It has six switching instants, in which one instant has zero CMV, three instants have $2V_{PV}/4$, and two instants have $V_{PV}/4$, CMV. There is no voltage transition in zero CMV. The CMV may take the values depending upon the inverter switch states selected since the voltage-source inverter cannot provide pure sinusoidal voltages and has discrete output voltage levels synthesized from the output voltage of the PV [10], [23]. The voltage transition depends upon the direction of the current in the inverter; hence, the proposed H-MCPWM modulation technique ensures the reduced common mode voltage generation in the band limit of maximum $\pm V_{PV}/4$. The switching pattern of the proposed H-MCPWM technique for five-level cascaded multilevel inverter is illustrated in Fig. 2. The operation of the proposed H-MCPWM is divided into two modes of operation, i.e., mode-1 and mode-2, as explained next.

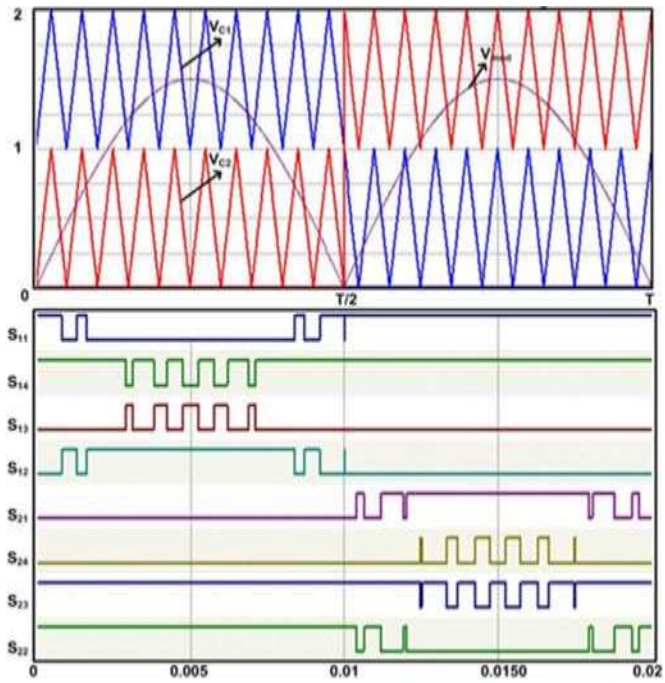


Fig. 2. Switching pattern of the proposed H-MCPWM technique for the five- level cascaded multilevel inverter.

A. Mode-1 (0 to T/2)

In this mode, all the carrier signals are in-phase with each other, the three-level voltages, i.e., 0, $-V_{PV}/2$, and $-V_{PV}$, are generated using following switching scheme:

1) When the reference signal V_{ref} is smaller than the carrier signals V_{c1} and V_{c2}, then the switches S_{11}, S_{14}, S_{23}, and S_{22} are turned ON and the complimentary switches, S_{13}, S_{12}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{aN} = V_{PV}/2$, $V_{\beta N} = 0$, and the output voltage is $V_{a\beta} = +V_{PV}/2$.
2) When the reference signal V_{ref} is greater the carrier signal V_{c2}, and lesser than the carrier signal V_{c1}, then the switches S_{14}, S_{12}, S_{23}, and S_{22} are turned ON and the
1) When both the carrier signals, V_{c1} and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned ON and the complimentary switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned OFF. In this situation $V_{aN} = 0$, $V_{\beta N} = V_{PV}/2$, and the output voltage is $V_{a\beta} = -V_{PV}/2$.

B. Mode-2 (T/2 to T)

In this mode, all the carrier signals are phase shifted by 180°, the three-level voltages, i.e., 0, $+V_{PV}/2$, and $+V_{PV}$, are gener- ated using following switching scheme.

1) When the reference signal V_{ref} is smaller than the carrier signals V_{c1} and V_{c2}, then the switches, S_{11}, S_{14}, S_{23}, and S_{22}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{21}, and S_{24},

the switches, S_{11}, S_{14}, S_{21}, and S_{23}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{22}, and S_{24}, are turned OFF. In this situation $V_{a'N'} = +V_{PV}/2$, $V_{\beta'N'} = +V_{PV}/2$, and the output voltage is $V_{a'\beta'} = 0$.

3) When both the carrier signals, V_{c1} and V_{c2}, are smaller than the reference signal V_{ref}, then the switches, S_{11}, S_{14}, S_{21}, and S_{24}, are turned ON and the complimentary switches, S_{13}, S_{12}, S_{23}, and S_{22}, are turned OFF. In this situation $V_{a'N'} = V_{PV}/2$, $V_{\beta'N'} = 0$, and the output voltage is $V_{a'\beta'} = +V_{PV}/2$.

The summary of the switching instants employed in two modes of operation is presented in Table I. It is clearly visible from the previous discussion that the proposed H-MCPWM technique is able to generate five-level inverter output voltage and attain reduced common mode voltage in the band of maximum $\pm V_{PV}/4$, which is superior to the conventional MCPWM technique.

III. Results and Discussions

To validate the proposed H-MCPWM technique, a prototype model is developed in the laboratory. The system parameters used for the experimental studies consist of four AKSHAYA ASP-1250 solar PV modules (each module is rated for 50 W), dc-link capacitance (2200 μF), ground resistance (10 Ω), parasitic capacitance (100 nF), switching frequency (3 kHz), and inductance (5 mH). The Mitsubishi make intelligent power modules (IPM), PM50RSD120 having IGBT switches is chosen for the H-bridge inverter. The multicarrier modulation techniques are implemented on XILINX XC3S1400A, field-programmable gate array (FPGA), which generates the gating signals for the switches of the IPM.

Fig. 3(a)–(c) shows the inverter output voltage, common mode voltage, output current and leakage current, respectively, for the PD-MCPWM, POD-MCPWM, and proposed H-MCPWM techniques, for the five-level inverter. It can be seen from the figure that the output voltages of the inverter have five voltage steps, i.e., +40 V, +20 V, 0, −20 V, and −40 V. It can be observed from Fig. 3(a) and (b), respectively, that the CMV is 35.2 V (peak) in the PD-MCPWM technique and 26.0 V (peak) in the POD-MCPWM technique. The proposed H-MCPWM technique produces CMV of 24.5 V (peak) as observed from Fig. 3(c). It is in good agreement with the theoretical aspects explained in the previous section that the PD-MCPWM technique varies in the band range of $\pm V_{PV}/2$ and hence, further reduction of CMV is not possible due to uncontrollable switching states. The H-MCPWM offers reduced magnitude of CMV to the band limit of maximum $\pm V_{PV}/4$. The proposed H-MCPWM provides reduced CMV during all the switching instants; hence, it renders low leakage current flow through the parasitic capacitance.

The simulation results comparison of different multicarrier PWM techniques, PD and POD-MCPWM [24], and the proposed H- MCPWM, regarding total harmonic distortion of the inverter output voltage and current, common mode voltage, leak-

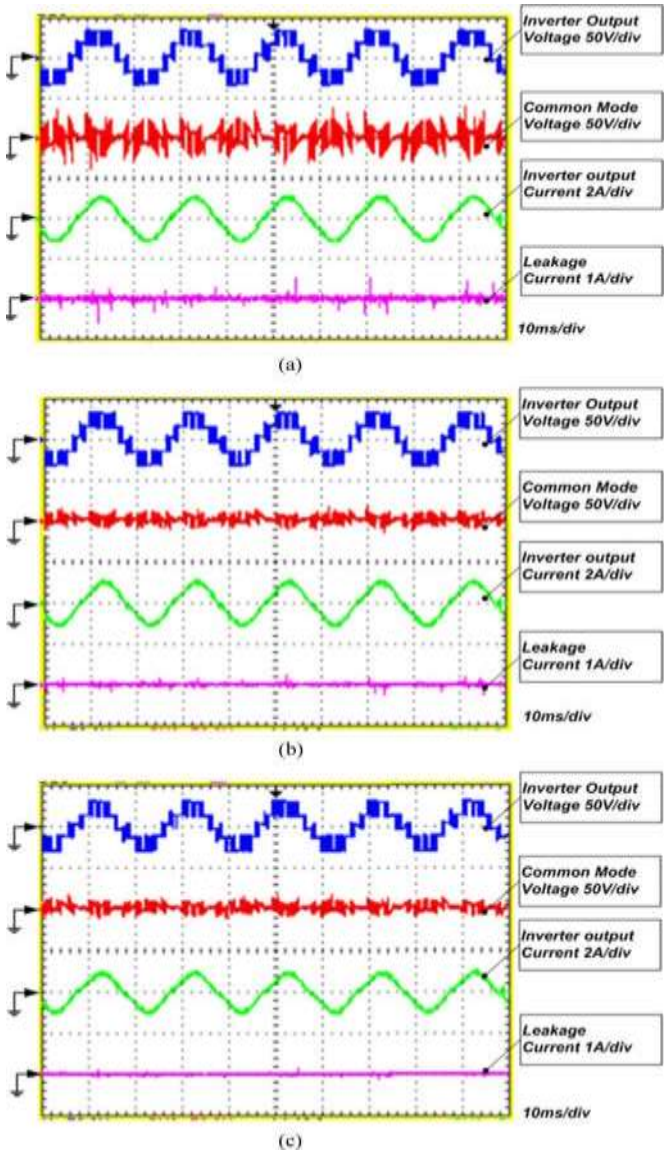
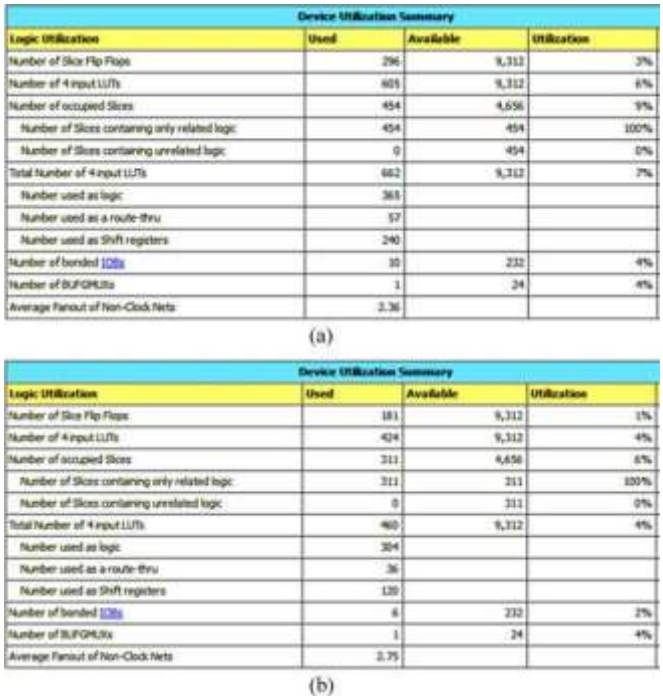


Fig. 3. Inverter output voltage, common mode voltage, inverter output current, and leakage current for (a) PD-MCPWM, (b) POD-MCPWM, and (c) proposed H-MCPWM techniques.

TABLE II
Comparison of Different Multicarrier PWM Techniques

Content	*PD-MCPWM*	*POD-MCPWM*	*H-MCPWM*
Total harmonic distortion% (voltage)	30.29%	30.96%	27.41%
Total harmonic distortion% (current)	4.71%	5.12%	4.25%
Common mode voltage	High	Low	Low
Leakage current (peak)	0.3 A	0.24 A	0.24 A
Leakage current (rms)	0.098 A	0.078 A	0.070 A



Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	296	9,312	3%
Number of 4 input LUTs	605	9,312	6%
Number of occupied Slices	454	4,656	9%
Number of Slices containing only related logic	454	454	100%
Number of Slices containing unrelated logic	0	454	0%
Total Number of 4 input LUTs	662	9,312	7%
Number used as logic	365		
Number used as a route-thru	57		
Number used as Shift registers	240		
Number of bonded IOBs	10	232	4%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.36		

(a)

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	181	9,312	1%
Number of 4 input LUTs	424	9,312	4%
Number of occupied Slices	311	4,656	6%
Number of Slices containing only related logic	311	311	100%
Number of Slices containing unrelated logic	0	311	0%
Total Number of 4 input LUTs	460	9,312	4%
Number used as logic	304		
Number used as a route-thru	36		
Number used as Shift registers	120		
Number of bonded IOBs	6	232	2%
Number of BUFGMUXs	1	24	4%
Average Fanout of Non-Clock Nets	2.75		

(b)

Fig. 4. FPGA device utilization summary report: (a) MCPWM (both PD and POD) techniques, and (b) proposed H-MCPWM technique.

output voltage of 120 V across the dc link of each H-bridge, parasitic capacitance (0.1 μF), modulation index (0.9), filter inductance (1.8 mH), and load (20 Ω). The table clearly shows the advantage of the proposed H-MCPWM as compared to the other multicarrier PWM techniques. Also the proposed H-MCPWM has less computational burden, as compared to the conventional MCPWM. To show this, the digital processor utilization summary report for XILINX XC3S1400A FPGA is shown in Fig. 4(a) and (b), respectively, for the MCPWM (same for both PD and POD) and for the proposed H-MCPWM techniques.

IV. Conclusion

This letter proposes H-MCPWM technique employed in transformerless cascaded multilevel inverter for the PV systems. The proposed modulation technique attains reduced common mode voltage with simplicity in implementation of the modulation technique. It has been illustrated that the proposed modulation technique has less leakage current as compared to the two- and three-level inverters. It is also observed that the proposed H-MCPWM offers less total harmonic distortion as compared to the conventional modulation methods. It uses only two carrier signals to generate the five-level inverter output which otherwise is four in other multicarrier modulation techniques.

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