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Review on Implementation of Optimized Digital Filter

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Abstract

Due to the explosive growth of multimedia application, the demand for high performance and low power DSP is getting higher and higher. Most widely used fundamental device performed in DSP system is FIR digital filter. Being the critical part of the theoretical advancement and implementation, FIR filter design continues to be a critical area of on-going research activities. for better performance it is good direction to optimize power consumption ,reduction in computational complexity as well as area optimization of FIR digital filter.

Key Words:

area optimization, low power, MAC, multiplier free, Pipelining.

Paper

I.INTRODUCTION

The speed of developments in electronic technology is taking place tremendously. Now a days, Digital Signal Processing (DSP) is used in various applications such as speech processing, digital versatile disk, portable video systems/computers, digital audio, multimedia and wireless communications, video compression, digital set-top box, cable modems, digital radio, transmission systems, radar imaging, acoustic beam formers, global positioning systems, and biomedical signal processing. The field of DSP has always been driven by the advances in DSP applications and in scaled very-large-scale integrated (VLSI) technologies. Therefore, at any given time, several challenges are imposed on the implementations of the DSP systems. These implementations must satisfy the enforced sampling rate constraints of the real-time DSP applications and must require less space and power consumption. DSP computation is different from general-purpose computation in the sense that the DSP programs are non terminating programs. In DSP computation, the same program is executed repetitively on an infinite time series. The non terminating nature can be exploited to design more proficient DSP systems by exploiting the dependency of tasks both within iteration and among multiple iterations. in addition, long critical paths in DSP algorithms limit the performance of DSP systems. Digital filters are essential elements of DSP systems. Digital filters are classified into two categories as: Finite Impulse Response (FIR) filter and Infinite Impulse Response (IIR) filter. Though FIR filters have linear phase property, low coefficient sensitivity and stability compare to IIR filter they have power consumption more than IIR filter . In many applications it is often advantageous to employ finite impulse response (FIR) filters, since they can be designed with exact linear phase and reveal no stability problems

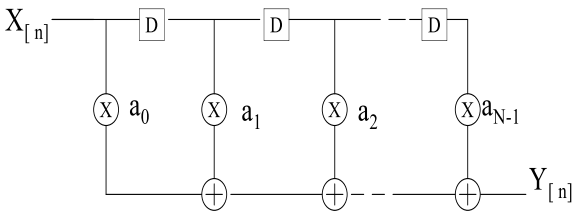
(Mitra, 2006). However FIR filters have a computationally more intensive complexity compared to infinite impulse response (IIR) filters with correspondent magnitude responses. During the past several years, many design methods have been proposed to reduce the complexity of the FIR filters.

II. DIGITAL FILTER

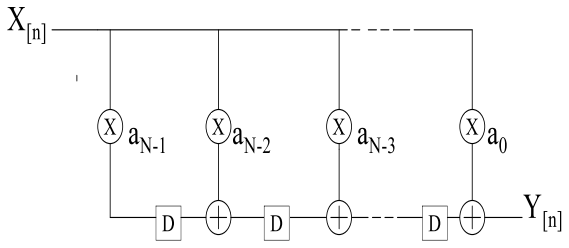
The output of a FIR filter is described by the following equation:

$$y[n] = a_0 x[n] + a_1 x[n-1] + \dots + a_{N-1} x[n-N]$$

x[n] is the input signal.y[n] is the output signal. a_i are the filter coefficients, also known as tap weights, that make up the impulse response.The output y of a FIR system is determined by convolving its input signal x with its impulse response a.



(a)Direct form



(b)Transposed form

Fig. 1 Various Realizations of FIR Filters

In general, there are two popular forms to realize FIR filters: direct and transposed shown in Fig. 2. In the direct form, there are delay units between multipliers. At a time, the present filter input, x(n), and N-1 previous samples of the input are fed to each multiplier input, and the filter output y(n) is the sum of product of every multiplier. In the transposed form, however, delay units are placed between adders so that the multipliers can be fed simultaneously. For the computation of FIR filter, we have to convolve the input data with filter coefficient, convolution process contains number of multiplication and addition.

III. LITERATURE REVIEW

Area optimization

Computational complexity of Digital Filter structures is given by total number of multipliers and total number of two input adders required for it's implementation, which indicates cost of implementation. For the applications demanding low power and high speed Digital Filters, various approaches developed so far to reduce the number of multiplications and additions are discussed below.

Strength reduction at algorithmic level can be used to reduce the number of additions and multiplications. Applications involving multiplication by constant are common in digital signal processing. A first solution proposed to optimize multiplication by constant was the use of constant recoding, such as Booth's. This solution just avoids long strings of consecutive ones in the binary representation of the constant.

In the paper titled "Low-Complexity Constant Coefficient Matrix Multiplication Using a Minimum Spanning Tree Approach", Oscar Gustafsson, Henrik Ohlsson, and Lars Wanhammar proposed an algorithm for low complexity constant coefficient matrix multiplication based on differences. It uses a minimum spanning tree (MST) to select the coefficients, which warrants low execution time as an MST can be found in polynomial time

In general, optimization techniques usually used for multiplier less filter design are complex, can require long run times, and provide no performance guarantees (Koter at al., 2003). Gordana Jovanovic Dolecek and Sanjit K. Mitra in their paper titled "Computationally Efficient Multiplier-Free Fir Filter Design", proposed simple efficient method for the design of multiplier-free.FIR filters without optimization. The method uses the rounding to the nearest integer of the coefficients of the equiripple filter which satisfies the desired specification. Considering that the integer coefficient multiplications can be accomplished with only shift-and-add operations, the rounded impulse response filter is multiplier-free.

Power optimization

In a FIR context, a MAC is the operation of multiplying a coefficient by the corresponding delayed data sample and accumulating the result. FIR usually requires one MAC per tap. high speed and high throughput Multiplier-Accumulator (MAC) unit that consumes low power, whi is always a key to achieve a high performance digital signal Processing system. A low power MAC unit can be designed and implemented using block enabling technique to save power. In any MAC unit, data flows from the input register to the output register through multiple stages such as, multiplier stage, adder stage and the accumulator stage. Within the multiplier stage, further, there are multiple stages of addition. During each operation of multiplication and addition, the blocks in the pipeline may not be required to be on or enabled until the actual data gets in from the previous stage. In block enabling technique, the delay of each stage is obtained. Every block gets enabled only after the expected delay. For the entire duration until the inputs are available, the successive blocks are disabled, thus saving power.

Pipelining is another method which reduces power consumption. It is a transformation leads to a reduction in the critical path, which can be exploited to either increase the clock speed or sample speed or to reduce power consumption at same speed. Critical path is defined as the path with longest computation time among all the paths that contain zero delays, and the computation time of the critical path is the lower bound on the clock period of the circuit. In parallel processing, multiple outputs are computed in parallel in a clock period. Therefore the effective sampling speed is increased by the level of parallelism.

Conclusion.

Low power, high speed and area optimization techniques for digital filter implementations are reviewed in this paper. A significant drop up to 40 percent in the total number of additions/subtractions is obtained by using Lefevre's modified approach for optimization of hardware multiplication by constant matrices. Design of MAC using block enabling technique results in low power consumption. also Pipelining is another method which reduces power consumption.The method for the design of multiplier-free FIR filters without optimization technique has proven less complexity which results in high speed digital filter.

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