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Design of a Reversible ALU with Novel Reversible Logic Gate Structures

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ABSTRACT: In digital computer system a major problem has been found that the Power dissipation which leads to bring some research on the methods to decrease this power dissipation. This is the main cause to give birth to reversible computing systems for digital computers and designs. The main aim of this reversible computing is to lower the power dissipation and some other advantages like security of data and prevention of errors etc... Reversible logic has so many applications low power CMOS, nanotechnology, DNA computing and quantum computing. There are two primary design implementations in this study which are the major spotlights. The first one is reversible design gate and the second one is multiplier design using reversible gates. In this manuscript we have implemented a 8 * 8 reversible design called "NSG". The total project is implemented in Xilinx 14.7 ISE with Spartan 3E family.

Keywords: Reversibility, NSG, Constant Input, Garbage Output, ALU.

I. INTRODUCTION

Energy loss is a very important factor in modern VLSI design. Irreversible hardware computation results in energy dissipation due to information loss. R.Landauer [1] has shown that for irreversible logic computations, each bit of information lost generated KTln2 joules of heat energy, where K is Boltzmann's constant and T is the temperature at which computation performed.

Reversible logic circuit does not have loss of information and reversible computation in a system can be performed only when the system consists of reversible gates. C.H.Bennet [2] showed that KTln2 energy dissipation would not occur if the computation is carried out in a reversible way.

Reversible logic is very crucial for the construction of low power, low loss computational designs which are very essential for the design process of arithmetic circuits used in quantum computation, Nano-technology and other low power digital circuits.

Lately, quite a few researchers have been paying their attention on the design, simulation and synthesis of proficient reversible logic circuits. The vital reversible gates [3] used for reversible logic synthesis are Feynman Gate and Fredkin gate [3, 4].

Reversible logic is emergent and drawing attention in the recent past due to its uniqueness i.e. less heat dissipating characteristics. It has been proved that any Boolean function can be implemented using reversible gates. The NS Gate [5] i.e. "NSG" can singly be implemented in all logical Boolean operations. Reversible logic has publicized possibilities to have widespread purpose in upcoming emerging promising technologies such as quantum computing, optical computing, quantum dot cellular automata in addition to ultra-low power VLSI circuits, DNA computing to generate zero power rakishness under ideal conditions.

In Proposed system, there exists a design of multiplier and adder units by number of reversible gates. In This design, we are using only

one reversible gate called NSG gate. By using this gate number of operations will be performed by only single gate and the garbage outputs also minimized. In this paper, we are also proposed a 8-bit Multiplier unit.

Multiplier unit is an inevitable component in many digital signal processing (DSP) applications involving multiplications. Multiplier unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT).

Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation. The multiplier and adder unit will be designed by NSG gate.

The simulation output is verified using Xilinx ISE 14.7.

II.8-BIT MULTIPLIER UNIT USING CONVENTIONAL MULTIPLIER

A Multiplier unit having the sum of the earlier consecutive products. The inputs from the Multiplier will be obtained from the memory location and it will be given to the multiplier block. The design contains 8 bit modified multiplier, 16 bit ripple carry adder and a shift register. In multimedia information processing, DSP applications and various other applications, the Multiplier operation is the key operation.

We are using the conventional Multiplier in the above Multiplier unit. The conventional multiplier of width N x N bits will generate the N number of partial products. The partial products are generated by bit wise AND in one multiplier bit with another multiplier. Hence, the N x N bit multiplier uses 2N multiplications and N-Adders in the architecture of Conventional multiplier.

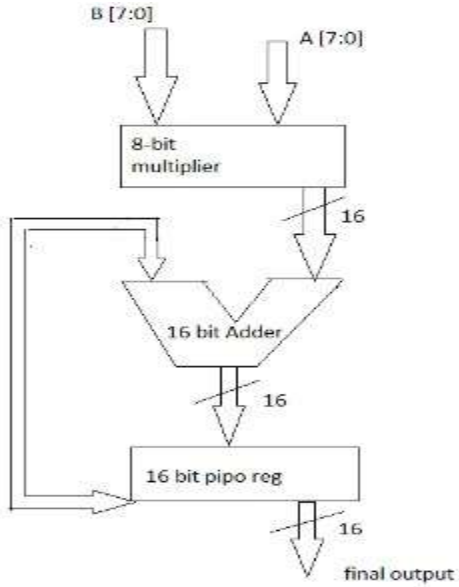

Fig 2.1 Multiplier Block Diagram

III. PROPOSED DESIGN

We have projected the reversible gate called NS gate "NSG" in this paper, which is a 4 * 4 one. The projected reversible NSG gate is shown in Figure.3.1. The analogous truth table of the gate is shown in Table I. It can be recognized from the Truth Table that the input pattern analogous to a particular output pattern can be completely resolute [5]. The NSG gate which is invented can perceive all Boolean logical operators. The input d, c, b and a are termed as input terminal 1, 2, 3 and 4 respectively and the output are termed as output 1, output 2, output3 and output 4 correspondingly from first to last of the paper.

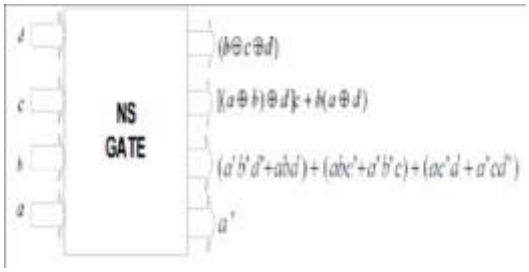

Fig 3.1 Proposed Reversible NS Gate

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Multiplier unit contains a multiplier, adder and register as mentioned above. In this paper, 8 bit modified Reversible NS multiplier has been used. The inputs of the Multiplier are obtained from the memory location and it will be given to the multiplier block. This will be very useful in the digital signal processor of the 8 bit. The input which is being fed from the memory location is 8 bit.

Since the bits are vast and also ripple carry adder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The register is taken out or fed back as one of the input to the ripple carry adder. The above figure 2.1 shows [8] the basic architecture of Multiplier unit. The figures 3.2 shows the 8X8 NS multiplier.

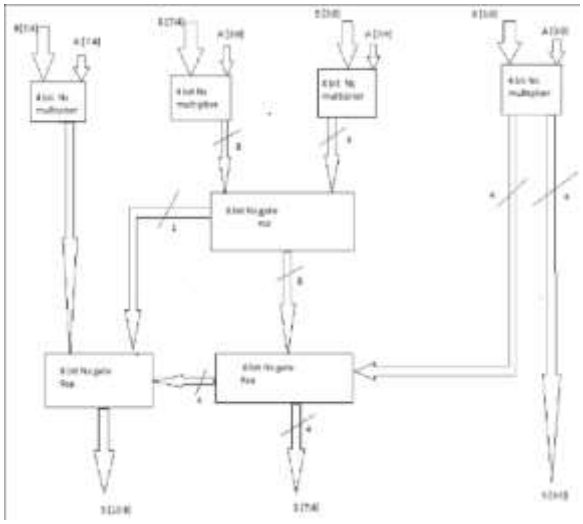

Fig 3.2 Multiplier Architecture

IV. RESULTS

The Reversible Multiplier unit simulated and synthesized using the Xilinx Design Suit13.2 with device family as spartan3E and device Xc3s100e5vq100. The simulation Results are verified by using Model sim simulator i.e. given the input values are multiplier of a = 00110011 (51) and b = 00011110 (30) and get the final output is final out = 0000101111110100 (3060). The Figure 4.1 shows the model graph of Reversible Multiplier unit and Table I shows the comparison of conventional and Reversible Multiplier units.

In the below table-I observe the number of (Look Up Tables) LUT's used in the general Multiplier unit is 214 which is higher than that of Reversible Multiplier unit. Here area occupied by the General Multiplier unit is higher than that of Reversible Multiplier unit. In reversible Mac unit, the multiplier we used was designed by using only one reversible gate called as NS gate. So area occupied by reversible multiplier is low when comparing with normal multiplier used in general Multiplier unit. And also the delay produced by general Mac unit is very high when comparing with Reversible Multiplier unit.

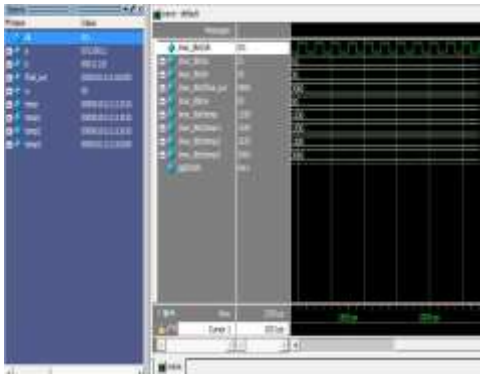

Fig 4.1 Simulation Results of Reversible MAC Unit

Architecture	LUT's	Area (%)	Delay (ns)
EXISTED SYSTEM	214	11	36.286
PROPOSED SYSTEM	207	10	27.288

TABLE I Comparison of Delay and Area For Conventional and Reversible Mac Units

V. CONCLUSION

Reversible multiplier can be designed with the different logical designs purposed in conventional combinational and sequential logic with the aim to improve the performance of computational units.

Number of gates, Number of garbage outputs, Number of ancillary inputs, are to be efficient to improve the performance of the reversible logic multiplier. Finally reversible logic gates are occupied less area and delay because it has a many to many input and output relations. So by using of these gates we can design any large circuits with less components and it is the main advantage of reversible logic gates.

VI.REFERENCES

[1] J R.Landauer, "Irreversibility and Heat Generation in the Computational Process", IBM Journal of Research and Development, 5,pp. 183-191,1961.

[2] C.H. Bennett, "Logical Reversibility of Computation", IBM 1. Research and Development, pp.525-532, Novemberl973.

[3] Bennett, C.H., 1988. "Notes on the history of reversible computation". IBM 1. Res. Develop., 32: 16-23.

[4] E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theor. Physics, 21(1982), pp.219-253.

[5]Neeraj kumarmisra, subodh wairya, vinod kumar singh, "An inventive design of 4*4 bit reversible NS gate", proceedings of IEEE international conference, 2014.

[6] T.nagapavani, V.rajmohan, p.rajendran "Optimized shift register design using reversible logic", proceedings of IEEE international conference, 2011.

[7] NM Nayeem, Md A Hossian, L Jamal and Hafiz Md. HasanBabu, "Efficient design of Shift Registers using Reversible Logic," Proceedings of International Conference on Signal Processing Systems, 2009.

[8] Samir palnitkar, "verilog HDL", second edition, IEEE 1364-2001 compliant.

[9] J. E. Rice, "A New Look at Reversible Memory Elements," Proceedings of IEEE International Symposium on Circuits and Systems, 2006.

[10] H. Thapliyal and M. B. Srinivas, "A Beginning in the Reversible Logic Synthesis of Sequential Circuits," Proceedings of Military and Aerospace Programmable Logic Devices International Conference, 2005.

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