International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 05
April 2017

Power Efficient Fixed Width Replica Redundancy Multiplier

K Revathi #1, SK Sahir *2
P.G. Scholar in VLSI, * Associate Professor & HOD, Department of ECE
Priyadarshini Institute of Technology & Sciences for Women, Tenali, Andhra Pradesh

Abstract

Most DSP applications runs on approximate values where as if u use normal elements which increases the area and the power, channel utilization also increases when we are dealing with the large bit length. Hence most architectural are turning towards fixed width multiplication. The present fixed with multipliers major problems are either lack of accuracy, replica blocks or improper compensation circuits. All drawbacks of earlier designs can be overcome by our proposed methods by designing fixed width multiplier without replica blocks and appropriate error compensation circuit. Replica blocks are removed from our design hence the overall area and the power of the system can be reduced drastically compare to that of the earlier designs.

I. INTRODUCTION

The rising of transportable and remote processing frameworks as of late drives the necessity for ultralow control frameworks. To bring down the office scattering, offer voltage scaling is wide utilized as a proficient low-control strategy since the office utilization in CMOS circuits is corresponding to the sq. of offer voltage. Be that as it may, in profound sub micrometer prepare advancements, clamor impedance issues have raised issue to style the dependable and sparing gadgets frameworks; in this way, the arranging strategies to fortify commotion resistance are wide created. Relate forceful low-control system, raised as voltage over scaling (VOS), was anticipated into lower offer voltage on the far side fundamental offer voltage while not yielding the yield. Be that as it may, VOS winds up in serious debasement in signal to noise (SNR). A totally exceptional recursive noise tolerant (ANT) strategy consolidated VOS primary piece with reduced precision reproduction (RPR) that battles delicate blunders successfully while accomplishing indispensable vitality sparing. Some hymenopteran distortion styles range unit given in and along these lines the hymenopterans style origination is more reached out to framework level. In any case, the RPR styles inside the hymenopterous creepy crawly styles of are composed in an extremely altered way, that aren't just received and lasting. The RPR styles inside the hymenopterous creepy crawly style will work in an exceptionally in the blink of an eye way, however their equipment many-sided quality is basically excessively progressed. Accordingly, the RPR style inside the hymenopterous creepy crawly style of remains the chief regular style because of its straightforwardness. Be that as it may, embracing with RPR in should in any case pay additionally space overhead and power utilization. In this paper, we tend to extra anticipated a clear means exploitation the settled width RPR to switch the full-width RPR piece. exploitation the settled width RPR, the calculation mistake will be rectified with lower control utilization and lower space overhead. we tend to take utilization of risk, insights, and halfway item weight investigation to search out the inexact remuneration vector for a considerable measure of exact RPR style. in order to not expand the significant way delay, we tend to restrict the pay circuit in RPR ought not be set inside the urgent way. Therefore, we will see the hymenopterous bug style with littler circuit space, bring down power utilization, and lower significant give voltage.

II. EXISTING ANT DESIGN

The ANT technique includes both main digital signal processor (MDSP) and error correction (EC) block, as shown in Fig. 1. To meet ultralow power demand, VOS is used in MDSP. However, under the VOS, once the critical path delay *T*cp of the system becomes greater than the sampling period *T*samp, the

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 05
April 2017

soft errors will occur. It leads to severe degradation in signal precision.

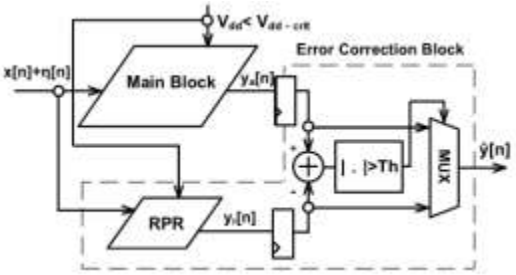

Fig.1. ANT architecture

In the ANT technique, a replica of the MDSP but with reduced precision operands and shorter computation delay is used as EC block. Under VOS, there are a number of input dependent soft errors in its output *ya*[*n*]; however, RPR output *yr*[*n*] is still correct since the critical path delay of the replica is smaller than *T*samp. Therefore, *yr*[*n*] is applied to detect errors in the MDSP output *ya*[*n*]. Error detection is accomplished by comparing the difference | *ya*[*n*] − *yr*[*n*]| against a threshold *Th*. Once the difference between *ya*[*n*] and *yr*[*n*] is larger than *Th*, the output *y*^[*n*] is *yr*[*n*] instead of *ya*[*n*]. As a result, *y*^[*n*] can be expressed as

$$\hat{y}[n] = \begin{cases} y_a[n], & \text{if } |y_a[n] - y_r[n]| \le Th \\ y_r[n], & \text{if } |y_a[n] - y_r[n]| > Th. \end{cases}$$

Th is determined by

$$Th = \max_{\forall \text{input}} |y_o[n] - y_r[n]|$$

Where *yo*[*n*] is error free output signal. In this way, the power consumption can be greatly lowered while the SNR can still be maintained without severe degradation.

III. PROPOSED ANT MULTIPLIER

In this paper, we tend to more arranged the settled width RPR to interchange the full-width RPR hinder inside the hymenopter style, as appeared in Fig. 2, which may not exclusively give higher calculation precision, bring down power utilization, and lower space overhead in RPR, however conjointly perform with higher SNR, a considerable measure of space temperate, bring down agent offer voltage, and lower control utilization in understanding the hymenopter outline. We tend to show our settled width RPR based hymenopter style in Associate in nursing hymenopter number. The settled width styles are some of the time connected in DSP applications to keep away from boundless development of bit broadness. Disconnecting n-bit least significant bit (LSB) yield might be an across the board reply to build a settled width DSP with n-bit input and n-bit yield. The equipment multifaceted nature and power utilization of a fixed width DSP is normally concerning 1/2 the full length one. Nonetheless, truncation of LSB half winds up in adjusting, that must be paid precisely. A few literary works are presented to decrease the misreckoning with steady redress cost or with variable rectification cost. The circuit many-sided quality to remunerate with consistent remedied cost might be less muddled than that of variable rectification esteem; at the same time, the variable amendment approaches at in some cases a great deal of exact.

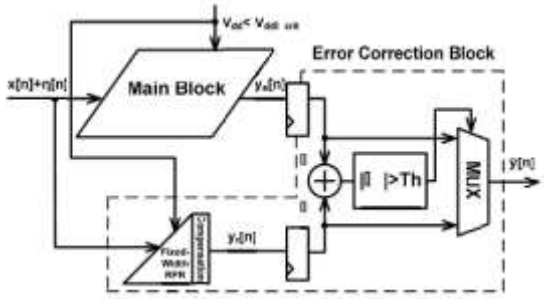

Fig.2. Proposed ANT architecture with fixed-width RPR

In their remuneration strategy is to repay the erroneous conclusion between the full length multiplier consider and furthermore the settled width multiplier figure. In any case, inside the settled width RPR of partner emmet multiplier calculate, the pay mistake we'd get a kick out of the chance to right is that the general erroneous conclusion of MDSP square. Dissimilar to, our pay system is to remunerate the erroneous conclusion between the full-length MDSP multiplier figure and furthermore the settled width RPR multiplier calculate. In today, there are a few fixed width multiplier consider styles connected to the full width multipliers. Be that as it may, there's still no fixed width RPR style connected to the emmet multiplier figure styles. to accomplish a great deal of exact blunder pay, we tend to remunerate the erroneous conclusion with variable adjustment worth. we tend to develop the blunder remuneration circuit

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 05
April 2017

in the principle misuse the incomplete item terms with the greatest weight inside the slightest essential segment. The blunder pay recipe makes utilization of possibility, insights, and relapse investigation to look out the rough remuneration worth. to abstain from squandering equipment quality, the pay vector inside the incomplete item terms with the greatest weight inside the minimum essential area is specifically infuse into the settled width RPR, that doesn't need promote remuneration logic gates. To any lower the pay mistake, we tend to conjointly consider the effect of truncated stock with the second most essential bits on the blunder remuneration. We have a tendency to propose a mistake pay circuit utilizing a basic minor input amendment vector to pay the blunder remained. All together not to build the basic way delay, we find the remuneration circuit in the noncritical way of the settled width RPR. As contrasted and the full-width RPR outline in, the proposed settled width RPR multiplier performs with higher SNR as well as with lower circuitry zone and lower control utilization.

A. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

In the hymenopter style, the perform of RPR is to rectify the blunders happening inside the yield of MDSP and keep up the SNR of entire framework while bringing down give voltage. Inside the instance of misuse settled width RPR to understand hymenopter plan, we have a tendency to not exclusively bring down circuit space and power utilization, however conjointly quicken the calculation speed as contrasted and the standard full-length RPR. Nonetheless, we need to remunerate tremendous misestimating inferable from pruning a few equipment segments inside the LSB a piece of MDSP. In the MDSP of n-bit ANT Baugh Wooley exhibit multiplier, its two unsigned n-bit inputs of X and Y can be communicated as

$$X = \sum_{i=0}^{n-1} x_i \cdot 2^i, \qquad Y = \sum_{j=0}^{n-1} y_j \cdot 2^j.$$

The multiplication result P is the summation of partial products of $xi\ y\ j$, which is expressed as

$$P = \sum_{k=0}^{2n-1} p_k \cdot 2^k = \sum_{j=0}^{n-1} \sum_{i=0}^{n-1} x_i y_j \cdot 2^{i+j}.$$

The $(n/2)$-bit unsigned full-width Baugh–Wooley partial product array can be divided into four subsets, which are most significant part (MSP), input correction vector [ICV(β)], minor ICV [MICV(α)], and LSP, as shown in Fig. 3. In the RPR, only MSP part is kept and the other parts are removed. Therefore, the other three parts of ICV(β), MICV(α), and LSP are called as truncated part. The truncated ICV(β) and MICV(α) are the most important parts because of their highest weighting. Therefore, they can be applied to construct the truncation error compensation algorithm. To evaluate the accuracy of a fixed-width RPR, we can exploit the difference between the $(n/2)$-bit fixed-width RPR output and the $2n$-bit full-length MDSP output, which is expressed as

$$\varepsilon = P - P_t$$

Where P is the output of the complete multiplier in MDSP and Pt is the output of the fixed-width multiplier in RPR. Pt can be expressed as

$$\begin{aligned} P_t &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i \\ &\quad + f\left(x_{n-1} y_{\frac{n}{2}}, x_{n-2} y_{\frac{n}{2}+1}, x_{n-3} y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}} y_{\frac{n}{2}+2}\right) \\ &\quad + f\left(x_{n-2} y_{\frac{n}{2}}, x_{n-3} y_{\frac{n}{2}+1}, x_{n-4} y_{\frac{n}{2}+2}, \ldots, x_{\frac{n}{2}} y_{n-2}\right) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(\mathrm{ICV}) + f(\mathrm{MICV}) \\ &= \sum_{j=\frac{n}{2}+1}^{n-1} y_j 2^j \sum_{i=\frac{3n}{2}-j}^{n-1} x_i 2^i + f(\mathrm{EC}) \end{aligned}$$

Where f(EC) is the error compensation function, f(ICV) is the error compensation function contributed by the input correction vector ICV(β), and f(MICV) is the error compensation function contributed by minor input correction vector MICV(α). The source of errors generated in the fixed-width RPR is dominated by the bit products of ICV since they have the largest weight. It is reported that a low-cost EC circuit can be designed easily if a simple relationship between f(EC) and β is found. It is noted that β is the summation of all partial products of ICV. By statistically analyzing the truncated difference between MDSP and fixed width RPR with uniform input distribution.

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 05
April 2017

B. Proposed Precise Error Compensation Vector for Fixed-Width RPR Design

To realize the fixed-width RPR, we construct one directly injecting ICV(β) to basically meet the statistic distribution and one minor compensation The term Cm1 is used to judge whether $\beta = 0$ or not. The judgment function is realized by one NOR gate, while its inputs are $Xn-1$ $Yn/2$, vector MICV(α) to amend the insufficient error compensation cases. The compensation vector ICV(β) is realized by directly injecting the partial terms ($Xn-1$ $Yn/2$,$Xn-2$ $Y(n/2)+1$,$Xn-3$ $Y(n/2)+2$,..... ... $X(n/2)+2$ $Yn-2$). These directly injecting compensation terms are labeled as $C1$, $C2$, $C3$,. . ., $C(n/2)-1$ in Fig. 3.The other compensation vector used to mend the insufficient error compensation case is constructed by one conditional controlled OR gate. One input of OR gate is injected by $X(n/2)Yn-1$, which is designed to realize the function of compensation vector β. The other input is conditional controlled by the judgment formula used to judge whether $\beta = 0$ and $\beta 1 = 0$ as well.

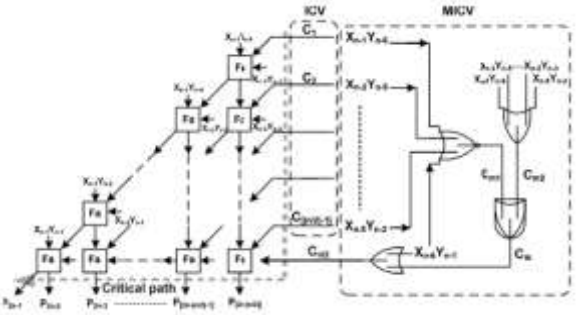

Fig. 3 Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation EC vectors combined ICV together with MICV.

The term Cm1 is used to judge whether $\beta = 0$ or not. The judgment function is realized by one NOR gate, while its inputs are $Xn-1$ $Yn/2$, $Xn-2$ $Y(n/2)+1$, $Xn-3$ $Y(n/2)+2$,. . ., $X(n/2)+2$ $Yn-2$. The term $Cm2$ is used to judge whether $\beta 1 = 0$. The judgment function is realized by one OR gate, while its inputs are $Xn-2$ $Yn/2$, $Xn-3$ $Y(n/2)+1$, $Xn-4$ $Y(n/2)+2$,. . ., $X(n/2)+1$ $Yn-2$. If both of these two judgments are true, a compensation term Cm is generated via a two-input AND gate. Then, Cm is injected together with $X(n/2)Yn-1$ into a two input OR gate to correct the insufficient error compensation. Accordingly, in the case of $\beta = 0$ and $\beta 1 = 0$ as well, one additional carry-in signal $C(n/2)$ is injected into the compensation vector to modify the compensation value as $\beta + 1$ instead of β. Moreover, the carry-in signal $C(n/2)$ is injected in the bottom of error compensation vector, which is the farthest location away from the critical path. Therefore, not only the error compensation precision in the fixed-width RPR can be enhanced, the computation delay will also not be postponed. Since the critical supply voltage is dominated by the critical delay time of the RPR circuit, preserving the critical path of RPR not be postponed is very important. Finally, the proposed high-precision fixed-width RPR multiplier circuit is shown in Fig. 3. In our presented fixed-width RPR design, the adder cells can be saved by half as compared with the conventional full-width RPR. Moreover, the proposed high-precision fixed-width RPR design can even provide higher precision as compared with the full-width RPR design.

IV. RESULTS

The essential multiplication rule is two-fold i.e. assessment of halfway items and amassing of the shifted incomplete items. It is performed by the progressive increments of the segments of the shifted halfway item lattice. The "multiplier" is effectively shifted and gates the fitting piece of the 'multiplicand'. The postponed, gated occurrence of the multiplicand should all be in a similar segment of the shifted halfway item framework. They are then added to frame the item bit for the specific shape. Multiplication is in this manner a multi operand operation. To extend the multiplication to both marked and unsigned numbers, an advantageous number framework would be the reintroduction of numbers in two's supplement arrange.

The program is composed and furthermore best level record is reproduced and diverse inputs are given to check the usefulness and contrasted and the manual estimations. The input record is spared and stacked here.

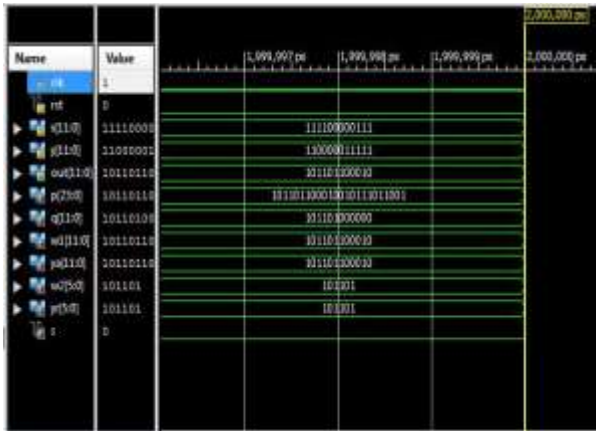

Fig.4 Simulation results

The above fig shows the fixed with multiplier with proposed compensation circuit result. By this the partial products can be reduced and as well as the operation time also will be reduced.

V. CONCLUSION

In this paper, a low-error and area-efficient fixed-width RPR-based ANT multiplier design is presented. The proposed 12-bit ANT multiplier circuit is implemented in TSMC 90-nm process and its silicon area is 4616.5 μm2. Under 0.6 V supply voltage and 200-MHz operating frequency, the power consumption is 0.393 mw. In the presented 12-bit by 12-bit ANT multiplier, the circuitry area in our fixed-width RPR can be saved by 45%, the lowest reliable operating supply voltage in our ANT design can be lowered to 0.623 *V*DD, and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

REFERENCES

[1] *The International Technology Roadmap for Semiconductor, 2009*

[2] Shim, S. Sridhara, and N. R. Shanbhag, "Reliable low-power digital signal processing via reduced precision redundancy," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 497–510, May 2004.

[3] B. Shim and N. R. Shanbhag, "Energyefficient soft-error tolerant digital signal processing," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 4, pp. 336–348,Apr.2006.

[4] R. Hedge and N. R. Shanbhag, "Energyefficient signal processing via algorithmic noisetolerance," in *Proc. IEEE Int. Symp. Low Power Electron. Des.*, Aug. 1999, pp.

[5] Gupta, D. Mohapatra, A. Raghunathan, and K. Roy, "Low-power digital signal processing using approximate adders," *IEEE Trans. Comput. Added Des. Integr. Circuits Syst.*, vol. 32, no. 1, pp. 124–137, Jan. 2013.

[6] Y. Liu, T. Zhang, and K. K. Parhi, "Computation error analysis in digital signal processing systems with overscaled supply voltage," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 18, no. 4, pp. 517–526, Apr. 2010.

[7] J. N. Chen, J. H. Hu, and S. Y. Li, "Low power digital signal processing scheme via stochastic logic protection," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2012, pp. 3077–3080.