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Design of High Speed Brent Kung Carry Select Adder

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ABSTRACT- *In this paper, Carry Select Adder (CSA) architectures are proposed using parallel prefix adders. Instead of using dual Ripple Carry Adders (RCA), parallel prefix adder i.e., Brent Kung (BK) adder is used to design Regular Linear CSA. Adders are the basic building blocks in digital integrated circuit based designs. Ripple Carry Adder (RCA) gives the most compact design but takes longer computation time. The time critical applications use Carry Look-ahead scheme (CLA) to derive fast results but they lead to increase in area. Carry Select Adder is a compromise between RCA and CLA in term of area and delay. Delay of RCA is large therefore we have replaced it with parallel prefix adder which gives fast results. In this paper, structures of 16-Bit Regular Linear Brent Kung CSA, Modified Linear BK CSA are designed. Memory used and delay of all these adder architectures are calculated at different input voltages.*

Keywords - Brent Kung (BK) adder, Ripple Carry Adder (RCA), Modified Linear BK Carry Select Adder.

I. INTRODUCTION

An adder is a digital circuit that performs addition of numbers. In many computers and other kinds of processors, adders are used not only in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices, and similar operations. Addition usually impacts widely the overall performance of digital systems and an arithmetic function. Adders are used in multipliers, in DSP to execute various algorithms like FFT, FIR and IlR.

Millions of instructions per second are performed in microprocessors using adders. So, speed of operation is the most important constraint. Design of low power, high speed data path logic systems are one of the most essential areas of research in VLSI. In CSA, all possible values of the input carry i.e. 0 and 1 are defined and the result is evaluated in advance. Once the real value of the carry is known the result can be easily selected with the help of a multiplexer stage. Conventional Carry Select Adder [1] is designed using dual Ripple Carry Adders (RCAs) and then there is a multiplexer stage. Here, one RCA (Cin=l) is replaced by Brent Kung adder. As, RCA (for Cin=O) and Brent Kung adder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary to Excess-l converter is introduced. Also the CSA [2] are designed using Brent Kung adder in order to reduce the power and delay of adder. In this paper, Modified Carry select Adder using Brent Kung adder is proposed using single BK and BEC instead of dual RCAs in order to reduce the power consumption with small penalty in speed.

II. PARALLEL PREFIX ADDERS

Parallel prefix adders [3] are used to speed up the binary additions as they are very flexible. The structure of Carry Look Ahead Adder (CLA) is used to obtain parallel prefix adders [4]. Tree structures are used to increase the speed [5] of arithmetic operation. Parallel prefix adders are used for high performance arithmetic circuits in industries as they increase the speed of operation. The construction of parallel prefix adder [6] involves three stages:

1. Pre- processing stage
2. Carry generation network
3. Post processing stage

PRE-POSSESSING STAGE

Generate and propagate signals to each pair of inputs A and B are computed in this stage. These signals are given by the following equations:

$$P_i = A_i \text{ xor } B_i \text{ ---- (1)}$$

$$G_i = A_i \text{ and } B_i \text{---- (2)}$$

CARRY GENERATION NETWORK

In this stage, we compute carries equivalent to each bit. Implementation of these operations is carried out in parallel. After the computation of carries in parallel they are segmented into smaller pieces. Carry propagate and

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generate are used as intermediate signals which are given by the logic equations3& 4

$$CP_{i:j} = P_{i:k+1} \text{ and } P_{k:j} \text{ -------- (3)}$$

$$CG_{i:j} = G_{i:k+1} \text{ or } (P_{i:k+1} \text{ and } G_{k:j})$$

The Operations involved in fig: 1 is given as:

$$CP_o = P_i \text{ and } P_j \quad \text{----------3(i)}$$

$$CG_o = (P_i \text{ and } G_j) \text{ or } G_i \text{-------3(ii)}$$

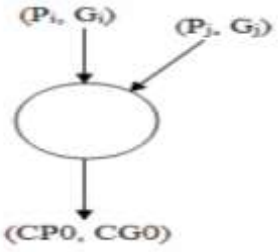

Fig 1: Carry Network

POST PROCESSING STAGE

This is the concluding step to compute the summation of input bits. It is common for all the adders and the sum bits are computed by logic equation 5& 6:

$$C_{i-1} = (P_i \text{ and } C_{in}) \text{ or } G_i \quad \text{--- (4)}$$

$$S_i = P_i \text{ xor } C_{i-1} \quad \text{--- (5)}$$

III. BRENT-KUNG ADDER

Brent-Kung adder [7] is a very well-known logarithmic adder architecture that gives an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent Kung adders. But the gate level depth of Brent-Kung adders [8] is 0 (log2 (n)), so the speed is lower.

Regular Linear Brent Kung Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin=1 and Brent Kung adder for Cin=0 and so it consumes more area. To solve this problem add-one schemes like gray cell have been introduced. Using gray cell, Regular Linear BK CSA is modified in order to obtain a reduced area and power consumption.

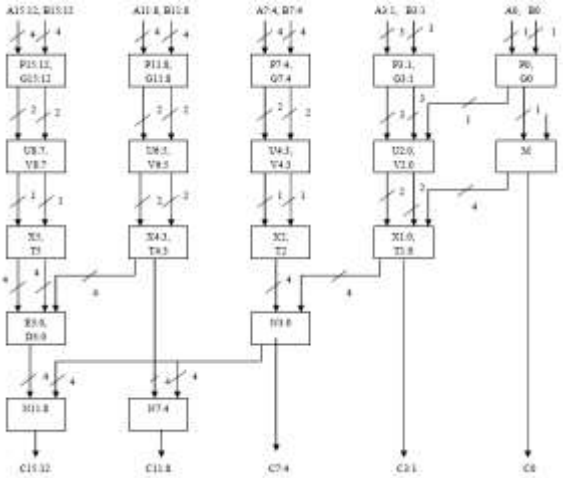

Fig. 2 16-Proposed System

IV. RESULTS

The output waveform is shown in below figure for proposed system.

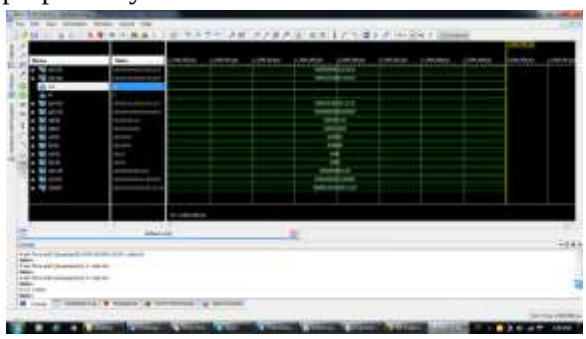

Fig. 3 Simulated Waveform of Brent Kung Adder

COMPARISON TABLE:

	DELAY (ns)	MEMORY (KB)
EXISTED SYSTEM	17.343	209
PROPOSED SYSTEM	11.764	205

	Existed	Proposed
No. of Slices	75	57
No. of 4input LUTs	130	99
No. of bonded IOBs	163	149

V. CONCLUSION

In this work, a Modified BK Carry Select Adder is proposed which is designed using single Brent Kung adder and Binary to Excess-l Converter instead of using single Brent kung adder for Cin=O and Ripple Carry Adder for Cin=l in order to reduce the delay and power consumption of the circuit. Here, the adder architectures like Regular Linear BK CSA, Modified Linear BK CSA, and Regular BK CSA and Modified BK CSA are designed for 16-Bit word size only. This work can be extended for higher number of bits also. By using parallel prefix adder, delay and power consumption of different adder architectures is reduced. As, parallel prefix adders derive fast results therefore Brent Kung adder is used. The synthesized results show that power consumption of Modified BK CSA is reduced in comparison to Regular Linear CSA but with small speed penalty. The calculated results conclude that Modified BK Carry Select Adder is better in terms of power consumption when compared with other adder architectures and can be used in different applications of adders like in multipliers, to execute different algorithms of Digital Signal Processing like Finite Impulse Response, Infinite Impulse Response etc.

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