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Programmable Generator Producing Virtual Arbitrary Test Patterns

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ABSTRACT:

The suggested hybrid plan efficiently combines test compression with LBIST, where both techniques could work synergistically to provide top quality tests. It is composed of a straight line finite condition machine driving a suitable phase shifter, and it arrives with numerous features permitting this product to create binary sequences with preselected toggling (PRESTO) activity. We introduce a means to instantly select several controls from the generator offering simple and easy, precise tuning. This paper describes a minimal-power (LP) generator able to creating pseudorandom test designs with preferred toggling levels that has been enhanced fault coverage gradient in comparison using the best-to-date built-in self-test (BIST)-based pseudorandom test pattern machines. Exactly the same strategy is subsequently used to deterministically advice the generator toward test sequences with enhanced fault-coverage-to pattern-count ratios. In addition, this paper proposes an LP test compression way in which enables shaping the exam power envelope inside a fully foreseeable, accurate, and versatile fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. Experimental results acquired for industrial designs illustrate the practicality from the suggested test schemes and therefore are reported herein.

Keywords: Built-in self-test (BIST), low-power (LP) test, pseudorandom test pattern generators (PRPGs.

I. INTRODUCTION

The semiconductor technology, design qualities, and also the design process are some of the important aspects which will impact this evolution. With new kinds of defects that certain will need to envisage to supply the preferred test quality for the following technology nodes for example 3-D. Test compression, introduced about ten years ago, has rapidly end up being the primary stream DFT methodology. This hybrid approach appears is the next logical transformative part of DFT. Its possibility of enhanced test quality it might augment the capabilities to operate at-speed power aware tests; also it can reduce the price of manufacturing test while protecting all LBIST and scan compression advantages. However, it's unclear whether test compression will manage to dealing with the rapid rate of technological changes within the next decade [1]. Curiously, logic built-in self-test (LBIST), initially produced for board, system, as well as in-field test, has become attaining acceptance for production test because it provides very robust DFT and it is used more and more frequently with test compression. Tries to overcome the bottleneck of test data bandwidth between your tester and also the nick make the idea of mixing LBIST and test data compression an important development and research area. Particularly, several hybrid BIST schemes store deterministic top-up designs around the tester inside a compressed form, after which make use of the existing BIST hardware to decompress these test designs. Just like conventional scan-based test, hybrid schemes, because of the high data activity connected with scan-based test procedures, may consume a lot more power than the usual circuit under- test is built to function under. With overstressing products past the mission mode, reductions within the operating power ICs inside a test mode happen to be of interest for a long time. Full-toggle scan designs may draw several occasions the normal functional mode power, which trend keeps growing, particularly within the mission mode's peak power. This power induced over-test may lead to thermal issues, current noise, power droop, or excessive peak control of multiple cycles which, consequently, result in a yield loss because of instant device damage, severe reduction in nick reliability, shorter product lifetime, or perhaps a device malfunction due to timing failures carrying out a significant circuit delay increase, for instance. This really is accomplished by

placing gating logic between scan cell outputs and logic they drive. Because the BIST power consumption can certainly exceed the utmost ratings when testing as fast as possible, scan designs should be moved in a low speed, and just the final couple of cycles and also the capture cycle are applied at its peak frequency. The very first four cycles serve shifting reasons, whereas the final the first is designated for capture. The aim would be to stabilize the ability supply prior to the last shifts and capture pulses are applied, that are crucial for at-speed tests. To lessen the current droop associated with a greater circuit activity, a burst clock controller slows lower a few of the shift cycles. It enables a gentle increase from the circuit activity, therefore lowering the di/dt effect. The controller can gate the shift clocks, with respect to the needs for progressively starting to warm up from the circuit. Within this paper, we advise a PRPG for LP BIST programs. The generator mainly is aimed at lowering the switching activity during scan loading because of its preselected toggling (PRESTO) levels. It may assume a number of designs that permit confirmed scan chain to become driven either with a PRPG itself or with a constant value fixed for any given time period [2]. Not just the PRESTO generator enables loading scan chains with designs getting low transition counts, and therefore considerably reduced power dissipation, it allows fully automated choice of its controls so that the resultant test designs feature preferred, user-defined toggling rates. We'll show this flexible programming could be further accustomed to produce tests better than conventional pseudorandom vectors regarding a resultant fault-coverage-to-test-pattern-count ratio. This paper culminates in showing the PRESTO generator may also effectively behave as an evaluation data decompress or, thus permitting someone to implement a hybrid test methodology that mixes LBIST and ATPG-based embedded test compression. This is actually the first LP test compression plan that's integrated in each and every way using the BIST atmosphere and allows designers shape the ability envelope inside a fully foreseeable, accurate, and versatile fashion. Consequently, it produces an atmosphere you can use to reach a competent hybrid solution mixing benefits of scan compression and logic BIST. Additionally, both techniques can complement one another to deal with, for instance, a current

drop the result of a high switching activity during scan testing, constraints of at-speed ATPG-created test designs, or new fault models.

II. EXISTED STRUCTURE

An n-bit PRPG of a phase shifter feeding scan chains forms a kernel from the generator creating the particular pseudorandom test designs. A straight line feedback shift register or perhaps a ring generator can use a PRPG. More to the point, however, n hold latches are put between your PRPG and also the phase shifter. Each hold latch is individually controlled using a corresponding stage of the n-bit toggle control register. As lengthy since its enable input is asserted, the given latch is transparent for data going in the PRPG towards the phase shifter, which is stated to stay in the toggle mode. Once the latch is disabled, it captures and saves, for several clock cycles, the related little bit of PRPG, thus feeding the phase shifter having a constant value. It's now within the hold mode. It's worth observing that every phase shifter output is acquired by XOR-in outputs of three different hold latches. Therefore, every scan chain remains inside a low-power mode provided only disabled hold latches drive the related phase shifter output [3]. As pointed out formerly, the toggle control register supervises the hold latches. Its content comprises 0s and 1s, where 1s indicate latches within the toggle mode, thus transparent for data coming in the PRPG. Their fraction determines a scan switching activity. The control register is reloaded once per pattern using the content of the additional shift register. The enable signals injected in to the shift register are created inside a probabilistic fashion using the original PRPG having a group of weights.

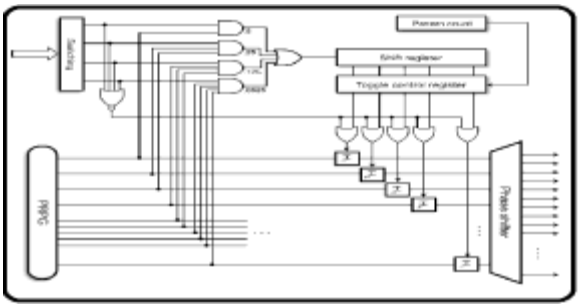

Fig.1. Block diagram of the PRESTO

III. PROPOSED MODEL

Much greater versatility in developing low-toggling test designs could be accomplished by implementing a plan presented. Basically, while protecting the operational concepts from the fundamental solution, this method splits up a shifting duration of every test pattern right into a sequence of alternating hold and toggle times. To

maneuver the generator backwards and forwards between both of these states, we make use of a T-type switch-flop that switches whenever there's single on its data input. If it's set to, the generator makes its way into the hold period with all of latches temporarily disabled whatever the control register content. This is achieved by putting AND gates around the control register outputs to permit freezing of phase shifter inputs. This property could be essential in SC designs where merely a single scan chain crosses confirmed core, and it is abnormal toggling could cause in your area unacceptable heat dissipation that may simply be reduced because of temporary hold periods. Two additional parameters stored in 4-bit Hold and Toggle registers figure out how lengthy the whole generator remains in both the hold mode or perhaps in the toggle mode, correspondingly. To terminate either mode, single must occur around the T switch-flop input. With the aid of shadow registers, values remain unchanged during capture. Clearly, it suits LBIST programs, in which the shift speeds are very high. The LP registers will also be added during embedded deterministic test (EDT) IP generation and insertion [4]. The connected logic is built-into the look combined with the EDT logic. Because the EDT logic (including LP) is just put in the scan pathways, there's no effect on the running mode of operation. performance from the PRESTO generator is dependent mainly around the following three factors: i) the switching code ii) the hold duty cycle (HC) iii) the toggle duty cycle (TC). A mission to attain greater BIST fault coverage with shorter test application time produced an enormous quantity of research previously. Typically, LFSR-based pseudorandom test sequences were modified either by putting a mapping logic between your PRPG outputs and inputs of the circuit. To be able to facilitate test data decompression while protecting its original functionality. It partitions confirmed test pattern into several blocks corresponding alternately to carry and toggle periods. Recall that within the hold mode, all phase shifter inputs are frozen because of disabled hold latches, whereas the toggle mode enables certain inputs from the phase shifter to get data in the ring generator provided the related items of the toggle control register are asserted. Because this register is up-to-date once per pattern, scan chains driven only by disabled hold latches consist of

constant values, and therefore stay in the LP mode for the whole pattern.

SIMULATION RESULTS:

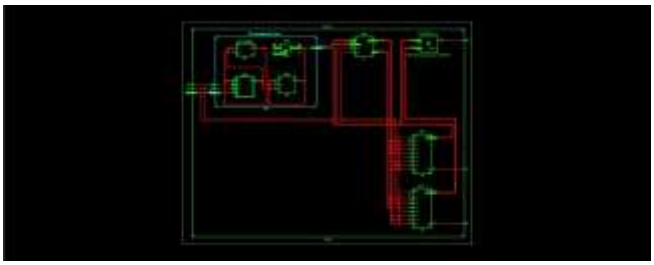

Fig: RTL Schematic

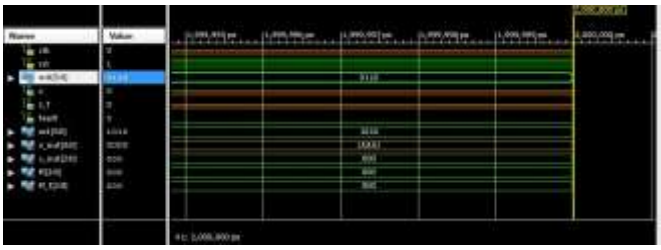

Fig: Simulation Form

IV. CONCLUSION

The suggested hybrid solution enables someone to efficiently combine test compression with logic BIST, where both techniques could work synergistically to provide top quality test. Exactly the same features may be used to control the generator, so the resultant test vectors may either yield preferred fault coverage quicker than the traditional pseudorandom designs while still reducing toggling rates lower to preferred levels, or they are able to offer noticeably greater coverage figures if run for comparable test occasions. As proven within the paper, PRESTO-the LP generator-can establish pseudorandom test designs with scan shift-in switching activity precisely selected through automated programming. This LP PRPG can also be able to serving as a completely functional test data decompress or having the ability to control scan shift-in switching activity through the entire process of encoding. Therefore, it is a really attractive LP test plan that enables for buying and selling-off test coverage, pattern counts, and toggling rates in an exceedingly flexible manner.

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