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Advanced Effective Risc Processor Design Using Built-In Self-Test Repair

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ABSTRACT: Built-in self-test repair (BISTR) technique has been most widely used to test repair embedded RISC processor. This paper proposes a reconfigurable BISTR (ReBISTR) scheme totest repairing RISC processor with different sizes and redundancy organizations. An efficient redundancy BIST algorithm is proposed to allocate redundancies of defective RISC processor. In the ReBISTR, a reconfigurable built-in self-test and test repairredundancy analysis is (ReBIRA) design circuit is to perform the redundancy algorithm for various RISC. Also, an adaptive reconfigurable methodology is proposed to reduce the test repair setup time when the RISC are operated in normal mode. Due to the complexity of memory architectures, the possibility of occurring manufacturing defects is high. Hence memory testing is necessary. Built inSelf-Testrepair (BISTR) has been proven to be most cost-effective and widely used solutions for memory testing. BISTR technique is used to reduce test repair time. The design architecture is simulatedin Xilinx ISE 14.7 tools.

KEYWORDS: SOC, BIST, BISTR, Test Pattern Generator, FPGA

I.INTRODUCTION

Very Large Scale Integration (VLSI) has a dramatic technology impact on the growth of digital technology. VLSI has not only reduced the size and the cost but also increased the complexity size of the circuits.

These improvements have resulted in significant performance. But it creates some potential problems, which may retard the effective use and growth of future VLSI technology.

Fast Development of VLSI technology results in continuously increasing density of Memory chips. The exponential increase in density makes yield improvement and testing issues.

As the feature size of component shrinks, the sensitivity to faults is also increases. Built inSelf-Testrepair (BIST) can solve the memory testing problems, which increases the comfort predictability. Test patterns generated by a BIST controller can be either deterministic or pseudo random generation. Built inSelf-test and repair (BISTR) is the most efficient technique that is used to faults to be test repair and to improve the yield of memory. To increase memory yield the most of manufactures use incorporated redundancy to replace faulty cells.

Embedded RISC processoris one of the key component in modern complex system-on-chip (SOC) designs. Typically, RISC processor consists of many RAMs having with various sizes are included in SOC which they occupy a portion of the chip area. Further, RAMs are subject to elude design rules, such that they are more chance to manufacturing defects. That is, RAMs have more serious problems of design yield and reliability than any other embedded cores in to an SOC.

To make the RAM cores at a reasonable perfect yield level is the very vital for product SOC. Built-in self-test repair (BISTR) technique has been shown to improve the RAM yield most efficiently. Built-in redundancy-analysis (BIRA) algorithm is one of the key component of a BISTR scheme, and it is responsible for allocating redundancies of memory under test. Thus, the BIRA circuit is to have heavily influence on the test repair efficiency of the BISTR scheme.

II.LITERATURE SURVEY

The MIPS processor is compilation of a lot manystructures which are used as blocks of interconnection. Theutilization of all these blocks is explained here.

1. Instruction Memory: This can simply be replaced by a

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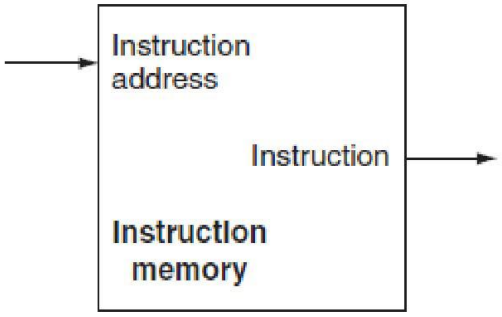

Figure 1: Instruction Memory

Read Only Memory (ROM). The instruction address is theaddress of particular instruction Stored in the Memory. For theparticular address respective instruction is saved in the ROM.It just reads the particular instructions from the required address. Hence this part in this work is replaced by an ROM.

2. Instruction Decoder Unit: This unit generally takesinput as a 32-bit instruction and outputs all the required instructions and these specified values are input to next part of circuit. The block diagram of Instruction Decoder unit is shown here.

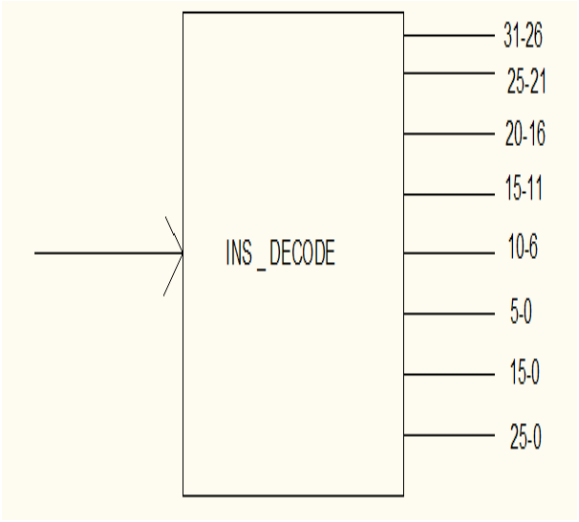

Figure 2: Instruction Decoder

3. Data Memory: This is the second memory of the MIPS.This memory can be used for both Read and Write applications. Hence this circuit can be replaced by a Random Access Memory. The input is the address and if read signal is enable it reads the data from the inputs memory location. If write signal is enable it writes the data into the input's memorylocation.

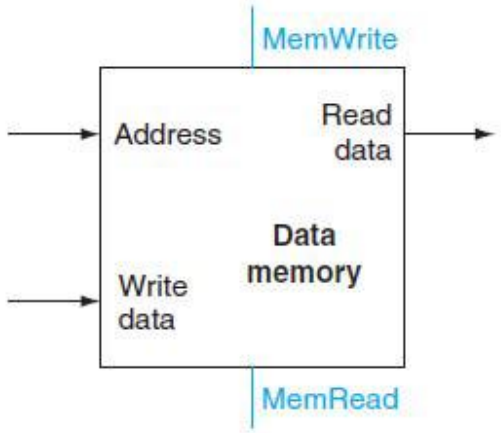

Figure 3: Data Memory

4.Sign Extend Unit:This unit is sign extension unit which inputs a 16 bit instruction as input and which gives 32 bit instruction as output. It is used for extending the immediate value.

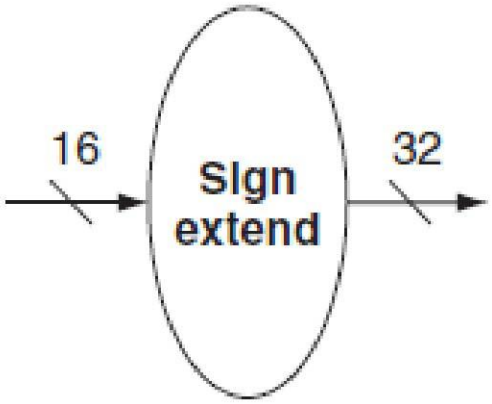

Figure 4: Sign Extend Unit

5. Registers:This is the next block presiding theInstruction Decoder. It is useful for reading the Instruction andperforming the reading or writing operations on the particular memorylocation.

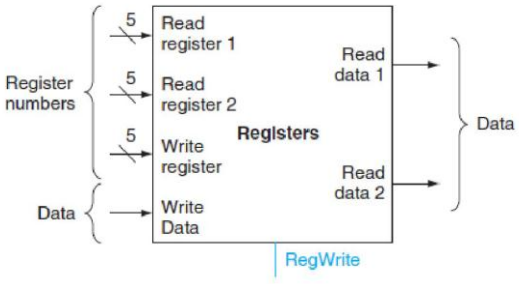

Figure 5: Registers

III.PROPOSED SYSTEM

ECC includes special test circuitry to detect and/or correct random faults (memory errors) in the stored data, using parity bits or error correction code.

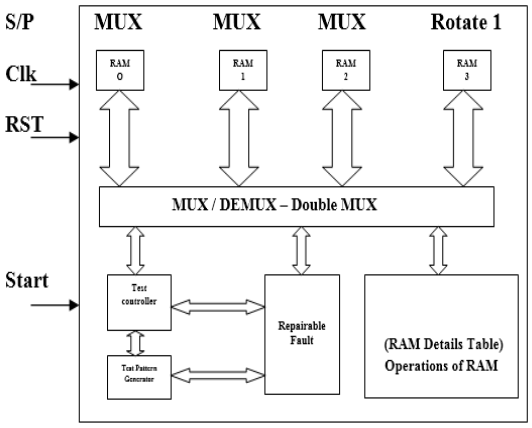

Figure 6 Block Diagram

Embedded memory testing isn't new and because memory is used as a test vehicle for technology development, testing of memory has been well studied fairly. Nevertheless, such testing remains a major problem in embedded-core-based RISC processors of complex as well as in SOC. In so many cases, built-in self-tests are used to test embedded memory. However, several methods of testing are used in the designs of SOC. Repaired memory is also a key issue in SOC for large embedded memories.

There is diversity of internal faults can be occurred in semiconductor memories, causing various types of failures in the function of the memory. These faults to be detected necessarily to test the procedures can be classified as in any digital circuit test into three more classes i.e., parametric testing of DC, parametric testing of AC and testing of function.

Multiplexers, or MUX's, can be either circuit of digitals made up of switch digital used to logic gates which are high speed or binary data.

The rams are used to store data and reconfigurable rams are used to restore the correct data. First the operation is done with respective of their application and testing patterns are generated to test their operation.

Test controller will control the circuit with pattern generations and total details are stored in ram detail table in RISC.

The fault pulse acts as an activation signal for programming the array. The FA (fault asserted) indicates that a fault has been detected. The field of a word contains the faulty operation, here as the data field is programmed to contain the correct data which is compared with the memory output.

In this mode the input multiplexer connects test collar input for memory under test as generated by the BIST circuitry of controller. While detecting the memory locations as fault by the fault diagnosis module of BIST Controller, the redundancy array is programmed in the figure 6

Memory is used as a unit under test. Fault Diagnosis is used to compare the data that expected with the data in original. If any change is there, it gives that location address and actual data to the Redundant Logic Array as input. This Redundant Logic Array acts as the redundant memory. In this we will store the data and the address of the faulty locations of memory. In normal mode it compares normal input address with the existing faulty locations; for read and write operations redundant logic memory will be used if it matches. If it doesn't match it will use the memory which is in original for the operations of read and write. Output multiplexer is used to select one value from the Redundant memory and Memory depending whether it is faulty or not.

The total slices, LUTs, IOBs used is shown in below table 1.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	12	960	1%
Number of 4 input LUTs	21	1920	1%
Number of bonded IOBs	43	108	39%

TABLE 1 Slices, LUT's & IOB's

The output waveform is shown in below figure 7, the four faulty rams are undergoes BIST test and then it produces faultless output of RISC processor.

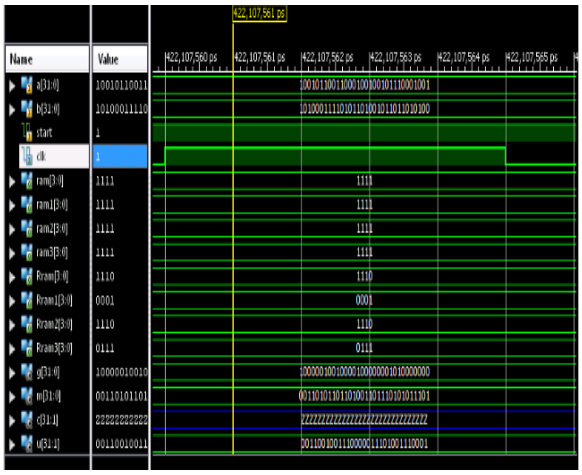

Figure 7 Output Waveform

The delay and memory used reports are shown in below.

```
Timing Detail:
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All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default path analysis
  Total number of paths / destination ports: 258 / 32
-------------------------------------------------------------------------
Delay:               11.883ns (Levels of Logic = 7)
  Source:            b<0> (PAD)
  Destination:       ram2<3> (PAD)

  Data Path: b<0> to ram2<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             1   1.218   0.595  b_0_IBUF (b_0_IBUF)
     LUT3:I0->O            7   0.704   0.743  ge1/G1 (u<1>)
     LUT3:I2->O            2   0.704   0.482  ge2/G_SW0 (N6)
     LUT3:I2->O            6   0.704   0.844  ge2/G (u<2>)
     LUT3:I0->O            4   0.704   0.762  ge18/G1 (u<18>)
     LUT3:I0->O            2   0.704   0.447  ram2_3_and00001 (ram3_2_OBUF)
     OBUF:I->O                 3.272          ram2_3_OBUF (ram2<3>)
    ----------------------------------------
    Total                     11.883ns (8.010ns logic, 3.873ns route)
                                       (67.4% logic, 32.6% route)

=========================================================================


Total REAL time to Xst completion: 9.00 secs
Total CPU time to Xst completion: 8.63 secs

-->

Total memory usage is 239520 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :   91 (   0 filtered)
Number of infos    :    0 (   0 filtered)
```

IV.CONCLUSION

The simulation results have shown that the ReBISR architecture is successfully able to implement new test algorithms. Implementation of a single test operation in one micro word ensures that any future test algorithms with any number of test operations per test element are successfully implemented using the current ReBISR architecture. Moreover, it provides a flexible approach as any new algorithm, other implemented using the same ReBIST hardware by changing the instructions in the RISC storage unit, without the need to redesign the entire circuitry. The Synthesis Report, Map Report, RTL Schematics are generated using Xilinx 14.7 i. The simulation results are generated and verified

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