International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 06
May 2017

DESIGN OF AN ACCURATEHIGH SPEED CARRY SELECT ADDER USING ENCODER

[1]SHAIK SHAKEELABI
M.TECH – SCHOLAR – E.C.E
Dept. of E.C.E
SRI CHUNDI RANGANAYAKULU ENGINEERING COLLEGE, GANAPAVARAM
GUNTUR DT.

[2]P.G.PUNITHA M.E
ASSISTANT PROFESSOR
Dept. of E.C.E
SRI CHUNDI RANGANAYAKULU ENGINEERING COLLEGE, GANAPAVARAM
GUNTUR DT.

ABSTRACT- In this paper, Carry Select Adder (CSA)architectures are proposed using parallel adders. Insteadof using dual Ripple Carry Adders (RCA) we design Regular LinearCSA. Adders are the basic building blocks in digital integratedcircuit based designs. Ripple Carry Adder (RCA) gives the mostcompact design but takes longer computation time. The timecritical applications use Carry Look-ahead scheme (CLA) toderive fast results but they lead to increase in area. Carry SelectAdder is a compromise between RCA and CLA in term of areaand delay. Delay of RCA is large therefore we have replaced itwith parallel prefix adder which gives fast results. In this paper,structures of 16-Bit modified LinearCSA are designed. Memory used and delay of allthese adder architectures are calculated at different input.

Keywords- Ripple Carry Adder(RCA), Regular Linear Carry Select Adder,Modified Linear Carry Select Adder.

I. INTRODUCTION

An adder is a digital circuit that performs addition ofnumbers. In many computers and other kinds of processors,adders are used not only in the arithmetic logic unit, but alsoin other parts of the processor, where they are used tocalculate addresses, table indices, and similar operations.Addition usually impacts widely the overall performance ofdigital systems and anarithmetic function. Adders are used inmultipliers, in DSP to execute various algorithms like FFT,FIR and IlR. Millions of instructions per second are performedin microprocessors using adders. So, speed of operation is themost important constraint.

Design of low power, high speeddata path logic systems are one of the most essential areas ofresearch in VLSI. In CSA, all possible values of the inputcarry i.e. 0 and 1 are defined and the result is evaluated inadvance. Once the real value of the carry is known the resultcan be easily selected with the help of a multiplexer stage.Conventional Carry Select Adder [1] is designed using dualRipple Carry Adders (RCAs) and then there is a multiplexerstage. Here, one RCA (Cin=l) is replaced by Decoder.As, RCA (for Cin= 0) and Decoder (for Cin=l) consume more chip area, so an add-one scheme i.e., Binary toExcess-l converter is introduced. Also the CSA [2] are designed using Decoderin order to reduce the power and delay of adder.In this paper, Modified Carry select Adderusing Decoder is proposed using single Decoder and BECinstead of dual RCAs in order to reduce the powerconsumption with small penalty in speed.

II. EXISTING SYSTEM

The structure is based on combining the concatenation and the incrementation schemes with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic replaces 2:1 multiplexers by AOI/OAI

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 06
May 2017

compound gates. The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. Note that, in this structure, as the carry propagates through the skip logics, it becomes complemented.

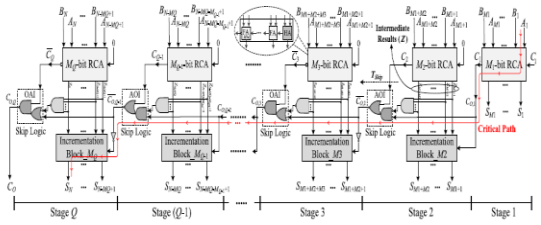

FIG. 1 EXISTED SYSTEM

Therefore, at the output of the skip logic of even stages, the complement of the carry is generated. The structure has a considerable lower propagation delay with a slightly smaller area compared with those of the conventional one. Note that while the power consumptions of the AOI (or OAI) gate are smaller than that of the multiplexer, the power consumption of the proposed CI-CSKA is a little more than that of the conventional one. This is due to the increase in the number of the gates, which imposes a higher wiring capacitance (in the noncritical paths).

Now, we describe the internal structure of the proposed CI-CSKA shown in Fig. 1 in more detail. The adder contains two N bits inputs, A and B, and Q stages. Each stage consists of an RCA block with the size of $Mj(j= 1, \ldots, Q)$. In this structure, the carry input of all the RCA blocks, except for the first block which is Ci is zero (concatenation of the RCA blocks). Therefore, all the blocks execute their jobs simultaneously.

III. PROPOSED SYSTEM

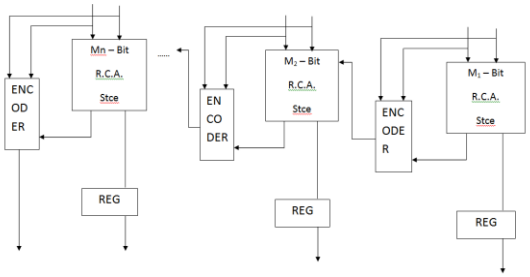

Fig. 2 PROPOSED SYSTEM

The total proposed system is depends on R.C.A Slice and encoder blocks. The register block is used to store the output. The R.C.A slide done the operations of generator and propagator along with sum generation. The encoder is used for carry generation and it is given to next RCA slice.

MUX based Register: A register consists of cascading a negative latch (master stage) with a positive one (slave stage). Fig. 1 shows a multiplexer-latch based implementation of register. On the low phase of the clock, the master stage is transperent, and the D input is passed to the master stage output, Q_M.

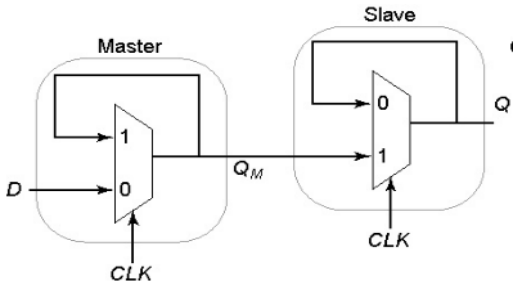

FIG 3 REGISTER BASED ON CONDITION

During this period, the slave stage is in the hold mode, keeping its previous value by using feedback. On the rising edge of the clock, the master stage stops sampling the input, and the slave stage starts sampling. During the high phase of the clock, the slave stage samples the output of the master stage (Q_M), while the master

International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 06
May 2017

stage remains in a hold mode. Since Q_M is constant during the high phase of the clock, the output Q makes only one transistion per cycle. The value of Q is the value of D right before the rising edge of the clock, achieving the *positive edge-triggered* effect.

IV. RESULTS

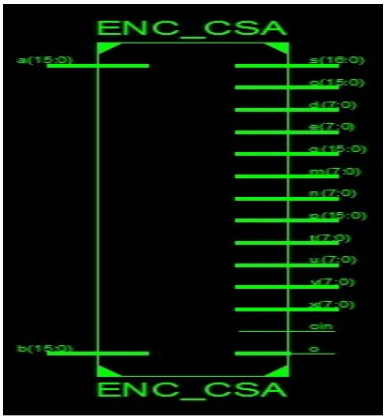

FIG 4 RTL SCHEMATIC

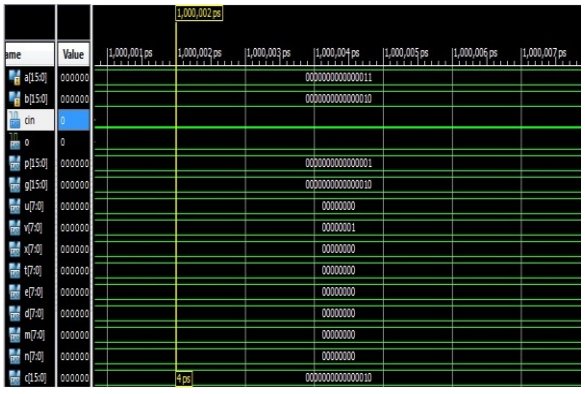

FIG 5 OUTPUT WAVEFORM

V. CONCLUSION

In this work, a Modified Carry SelectAdder is proposed which is designed using single Decoder for Cin=O and Ripple Carry Adder forCin=l in order to reduce the delay and power consumption ofthe circuit. Here, the adder architectures like Regular Linear CSA, Modified Linear CSA, and RegularCSAand Modified CSA are designed for 16-Bit wordsize only. This work can be extended for higher number of bitsalso. By using parallel prefix adder, delay and powerconsumption of different adder architectures is reduced. As,parallel prefix adders derive fast results therefore Decoder is used. The synthesized results show that powerconsumption of Modified CSA is reduced incomparison to Regular Linear CSA but with small speedpenalty. The calculated results conclude that Modified Carry Select Adder is better in terms of powerconsumption when compared with other adder architectures and can be used in different applications of adders like inmultipliers, to execute different algorithms of Digital SignalProcessing like Finite Impulse Response, Infinite ImpulseResponse etc.

VI. REFERENCES

[I] ShivaniParmar and Kirat Pal Singh," Design of High Speed Hybrid CarrySelect Adder", IEEE's 3rd International Advance Computing Conference(IACC) Ghaziabad, ISBN: 978-1-4673-4527-9,22-23 February 2013.

[2] Yajaun He, Chip-Hong Chang, and JiangminGu, "An area efficient 32-Bit carry-select adder for low power Applications, " in Proc.IEEE International Symposium Circuits and Systems, vol. 4, pp. 4082-4085,2005.

[3] M. Snir, "Depth-Size Trade-Offs for Parallel Prefix Computation",Journal of Algorithms, Vo!.7, Issue-2, pp.185-201, June 1986.

[4] David Jeff Jackson and Sidney Joel Hannah, "Modelling and Comparisonof Adder Designs with Verilog HDL", 25th South-eastern Symposium on

System Theory, pp.406-4tO, March 1993.[5] Belle W.Y. Wei and Clark D. Thompson, "Area-Time Optimal AdderDesign", IEEE transactions on Computers, vo!.39, pp. 666-675,May1990.
[6] Y. Choi, "Parallel Prefix Adder Design", Proc. 17th IEEE Symposium onComputer Arithmetic, pp. 90-98, 27th June 2005.
[7] J. M. Rabaey, "Digital Integrated Circuits- A Design Perspective", NewJersey,Prentice-Hall, 2001.
[8] R. Brent and H. Kung, "A regular layout for parallel adders", IEEETransaction on Computers, vol. C-31,n o.3,p p. 260-264,M arch 1982.
[9] AdilakshmiSiliveru, M. Bharathi, "Design of Kogge-Stone and Decoders using Degenerate Pass Transistor Logic", InternationalJournal of Emerging Science and Engineering, Vol.-I, Issue-4, February2013.
[10] K. Saranya, "Low Power and Area-Efficient Carry Select Adder",International Journal of Soft Computing and Engineering, Vol.-2, Issue-6,January 2013.
[11] DeepthiObul Reddy and P. Ramesh Yadav, "Carry Select Adder withLow Power and Area Efficiency", lnlernalional Journal of EngineeringResearch and Developmenl, Vol. 3, Issue 3, pp. 29-35, August 2012.

SHAIK SHAKILABI studied Btech-ECE in srichundiranganayakulu engineering college and MTECH-ECE in Sri ChundiRanganayakulu Engineering College.

P.G. PUNITHA studied B.E - ECE in University College of Engineering Villupuram (Constituent College of Anna University) and M.E - VLSI Design in Saveetha Engineering College, Chennai. She worked as an VLSI verification engineer in Aceic Design Technologies, Bangalore for 6 monthsand currently working as an Assistant Professor in S.C.R. Engineering College, Guntur Dt.