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Design Aging Awaredual Logic Level Multiplier

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ABSTRACT: This paper presents the design aDual logic level [D.L.L] multiplierfor 32*32bit number multiplication. Modern computer system is a dedicated and very high speed unique multiplier. Therefore, this paper presents the design aDuallogic level multiplier. The proposed systemconsists of two stages preprocessing and post processing interconnected blocks. By extending bit of the operands and generating an additional product the Duallogic level multiplier is obtained. Multiplication operation is performed by the Duallogic levelis efficient with the less area anditreduces delay i.e., speed is increased.

Keywords: D.L.L, partial products, Dual level logic unit.

I.INTRODUCTION

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low-power multiplier design has been an important part in low-power VLSI system design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally determined by the multiplier is generally the slowest element in the system.

Furthermore, it is generally the most area consuming.Hence, optimizing the speed and area of the multiplier is a major design issue. However, area and speed are usually conflicting constraints so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel.

The high speed multipliers and pipelined multipliers are used for digital signal processing (DSP) applications such as for multimedia and communication systems. High speed DSP computation applications such as Fast Fourier transform (FFT) require additions and multiplications.

II.LITERATURE SURVEY

The conventional modified Booth encoding (MBE) generates an irregular partial product array because of the extra partial product bit at the least significant bit position of each partial product row. Therefore papers [4] presents a simple approach to generate a regular partial product array with fewer partial product rows and negligible overhead, thereby lowering the complexity of partial product reduction and reducing the

area, delay, and power of MBE multipliers. But the drawback of this multiplier is that it function only for signed number operands.

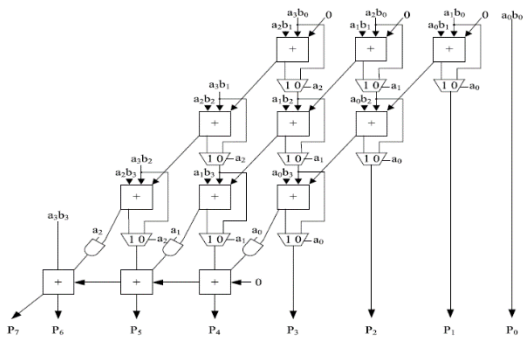

FIG. 1: EXISTED SYSTEM

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The multiplier array consists of (n−1)rows of carry save adder (CSA), in which each row contains(n − 1) full adder (FA) cells. Each FA in the CSA array hastwo outputs: 1) the sum bit goes down and 2) the carry bitgoes to the lower left FA. The last row is a ripple adder forcarry propagation.

III.PROPOSED SYSTEM

The gates in the Dual logic level [D.L.L] multiplier are always active regard of input logics. In,Dual logic level [D.L.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 2 shows a 4*4Dual logic level [D.L.L] multiplier, it can be seen that done their operations and the outputs are passed to interconnect Blocks simultaneously.

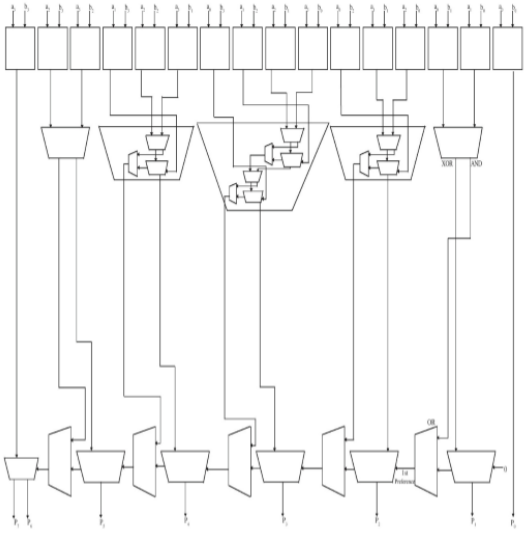

FIG. 2 PROPOSED SYSTEM [4*4 D.L.L]

Therefore, the output of the adders in both diagonals is 0, and the outputsum bit is simply equal to the third bit.The above fig. 2 shows the 4*4 high performance Dual logic level multiplierreduced the timing waste occurring in traditionalcircuits that use the critical path cycle as an execution cycleperiod. The basic concept is to execute a shorter path using Dual logic. Since mostpaths execute in a cycle period that is much smaller thanthe critical path delay.The same architecture is extended up to 32*32 bits.

IV.RESULTS

Dual logic level widely been adopted in multipliers since it can reduce the number of partial product rows to be added, thus reducing the size and enhancing the speed of the reduction tree. The least significant bit position of each partial product rowencoding, leading to an irregular partial

product array and a complex reduction tree. Therefore, the Dual logic level multipliers with partial product array produce a very highspeed.

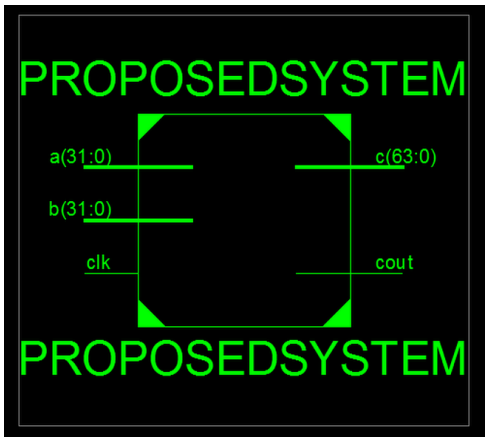

FIG. 3R.T.L SCHEMATIC

The above fig. 3 shows the R.T.L schematic of high performance Dual logic level multiplier and fig. 4 shows the technical schematic one of theLUT block of high performance Dual logic level multiplier.

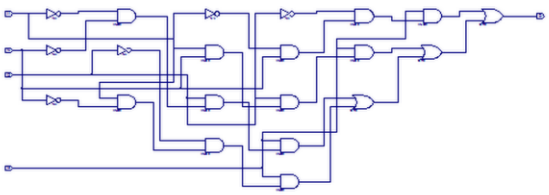

FIG. 4 LUT IN TECHNICAL SCHEMATIC

The below figure 5 shows the output waveform of 32*32 bitDual logic level multiplier.

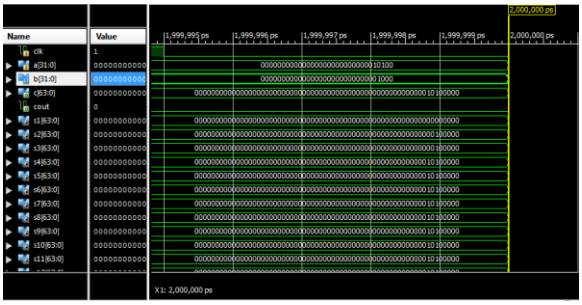

FIG. 5 OUTPUT WAVEFORMS

The below table 1 shows the comparison of existed system 32*32 and proposed system 32*32 with area and delay

System/parameter	Area[kb]	Delay[ns]
Existed System	316352	126.865
Proposed system	272000	110.363

TABLE.1 COMPARISON TABLE

The above comparison table shows that area of the proposed system is less than existed system and delay is also efficient.

V.CONCLUSION

The proposed system consists of two stages preprocessing and post processing interconnected blocks. The each block consists of gates and the row in the architecture is lesser than existed multiplier. By generating aproduct with Dual logic level multiplier 32*32 is obtained. Multiplication operation is performed by the Dual logic levelunit is better performance than existed multiplier. The required hardware and the chip memory reduces and it reduces delay i.e., speed is increased.

FUTURESCOPE: The same can be extended up to 64, 128, etc.., we can design an A.L.U by using proposed system.

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