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Architecture of error free content address memory on 16*8 sparse clustered networks

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ABSTRACT—We propose a low-power content-addressable memory (16*8-CAM) employing a new algorithm for associativity between the input tag and the corresponding address of the output data. The proposed architecture is based on a recently developed sparse clustered network using binary connections that on-average eliminates most of the parallel comparisons performed during a search. Therefore, the dynamic energy consumption of the proposed design is significantly lower compared with that of a conventional low-power 16*8- CAM design. Given an input tag, the proposed architecture computes a few possibilities for the location of the matched tag and performs the comparisons on them to locate a single valid match.

I.INTRODUCTION

A CONTENT-addressable memory (CAM) is a type of memory that can be accessed using its contents rather than an explicit address. In order to access a particular entry in such memories, a search data word is compared against previously stored entries in parallel to find a match. In the comparison process each stored entry is associated with a tag. Once a search data word is applied to the input of a CAM, the matching data word is retrieved within a single clock cycle if it exists. This prominent feature makes CAM a promising candidate for applications where frequent and fast look-up operations are required, such as in translation look-aside buffers (TLBs) [1], [2], network routers [3], [4], database accelerators, image processing, parametric curve extraction [5], Hough transformation [6], Huffman coding/ decoding [7], virus detection [8] Lempel–Ziv compression [9], and image coding [10]. Due to the frequent and parallel search operations, CAMs consume a significant amount of energy. CAM Architecture typically use highly capacitive search lines (SLs) causing them not to be energy efficient when scaled. For example, this power inefficiency has constrained TLBs to be limited to no more than 512 entries in current processors. In Hitachi SH-3 and StrongARM embedded processors, the fully associative TLBs consume about 15% and 17% of the total chip power, respectively. Consequently, the main research objective has been focused on reducing the energy consumption without compromising the throughput. Energy saving opportunities have been discovered by employing either a circuit-level techniques, architectural-level techniques, or the code sign of the two, some of which have been surveyed in although dynamic CMOS circuit techniques can result in low-power and low-cost CAMs, these designs can suffer from low noise margins, charge sharing, and other problems. A new family of associative memories based on sparse clustered networks (SCNs) has been recently introduced, and implemented using field-programmable gate arrays (FPGAs). In the conventional Hop field networks. we can store many short messages instead of few long ones and is made possible by such memories with a significantly lower level of computational complexity. Further more significant improvement is achieved in terms of the number of information bits stored per memory bit (efficiency). In this paper, a variation of this approach and a corresponding architecture are introduced to construct a classifier that can be trained with the association between a small portion of the input tags and the corresponding addresses of the output data.

II. EXISTED SYSTEM

The term CAM refers to binary CAM (BCAM) throughout this paper. Originally included in preliminary results were introduced for an architecture with particular parameters conditioned on uniform distribution of the input patterns. In this paper, an extended version is presented that elaborates the effect of the design's degrees of

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freedom, and the effect of non-uniformity of the input patterns on energy consumption and the performance. The architecture (SCN-CAM) consists of an SCN-based classifier coupled to a CAM-array. The CAM-array is divided into several a equally sized sub-blocks, which can be activated independently. For a previously trained network and given an input tag, the classifier only uses a small portion of the tag and predicts very few sub-blocks of the CAM to be activated. Once the sub-blocks are activated, The tag is compared against the few entries in them when the sub blocks are activated and keeping the rest deactivated one lowers the dynamic energy dissipation.

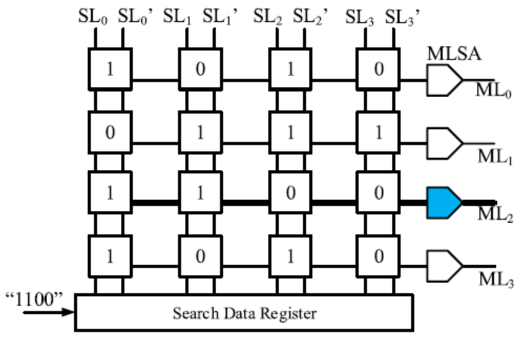

Fig. 1. Simple example of a 4×4 CAM array consisting of the CAM cells, MLs, sense amplifiers, and differential SLs.

III.PROPOSED SYSTEM

We extend this in to 16*8 cam as shown in below fig 2

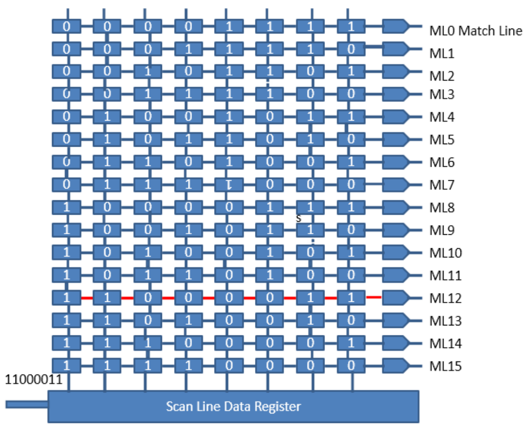

FIG. 2

This below tabular form gives the 16*8 cam T.T.

0	0	0	0	1	1	1	1
0	0	0	1	1	1	1	0
0	0	1	0	1	1	0	1
0	0	1	1	1	1	0	0
0	1	0	0	1	0	1	1
0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	0	0
1	0	0	0	0	1	1	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	0	0	0	0	1	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0

The proposed architecture consists of a neural-network based classifier coupled to a CAM array.To activate independently the CAM array is divided into several equally sized sub blocks. The classifier uses a small portion of it and will predict for a previously trained network and given input tag, on average the two out of several sub-blocks are activated in the CAM. Only two CAM entries should be compared to find the match with the cost of higher hardware complexity if the number of sub blocks is equal to the number of entries in the CAM . The tag is compared when the sub blocks are activated against the few entries in them and keeping the rest deactivated. Depending on the silicon area availability the total number of sub blocks are designed, since each sub-block will slightly increase the silicon area. More sub-blocks will be activated during a search if the input data is not a uniformly distributed and the accuracy of the final output is not affected. However, it is possible to select the reduced-length tag bits depending on the application instead of using the full length of the tag in the proposed architecture and according to a pattern to reduce the tag correlation.

The pre computation based CAM (PB-CAM) architecture(also known as one's count) was introduced in PB-CAM divides the comparison process and the circuitry into two stages. First, it counts the number of ones in an input and then

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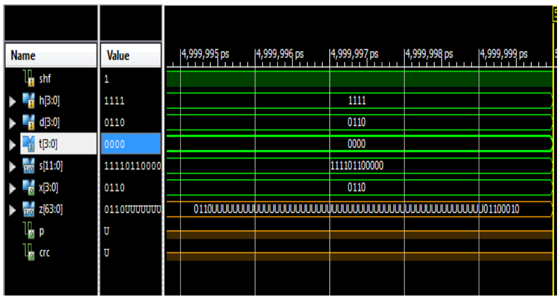
compares the result with that of the entries using an additional CAM circuit that has the number of ones in the CAM-data previously stored. This activates a few MLs and deactivates the others. In the second stage, a modified CAM hierarchy is used, which has reduced complexity, and has only one pull-down path instead of two compared with the conventional design. The modified architecture only considers0 mismatches instead of full comparison since the 1s have already been compared. The number of comparisons can be reduced to $M \times \_\log (N+2)\_+(M \times N)/(N+1)$ bits, where M is the number of entries in the CAM and N is the number of bits per entry. In the proposed design, we demonstrate how it is possible to reduce the number of comparisons to only N bits.Furthermore, in PB-CAM, the increase of the tag length affects the energy consumption, the delay, and also complicates the pre computation stage.

As shown in Fig. 2 the proposed architecture consists of a clustered-neural-network (CNN) connected to a modified CAM array. The CNN is at first trained with the association between a reduced-length tag and the address of the data to be later retrieved. The CAM array is divided into several sub-blocks based on a conventional architecture that can be compare enabled independently. Once an input tag is applied to the CNN, it will predict which CAM sub-block(s) need to be compare enabled and thus saves power by disabling the rest. If the full length of the tag is used, the classifier will be able to always point to a single sub-block. However, training the network with the full length of the tags will affect the hardware complexity of the CNN. On average only two possibilities are found with the right number of bits of the reduced-length tag if the reduced-length tags are uniformly distributed. On the other hand, in some cases, this truncation may cause ambiguities in finding the valid match causing more than one possible CAM sub-block to be activated. This effect will not affect the accuracy of the final result but will cost more power.

As shown in Fig. 2, the network consists of two parts: PI and PII . PI corresponds to the input tag and consists of neurons that are grouped to gather into l neurons each with equally sized clusters equally-sized clusters. Each neural value is binary, i.e. it is either activated or not. The processing of an input message can be within either of the two situations: training or decoding. In this paper, either for training or decoding purposes, the input tag is reduced in length to q bits, and then divided into c equally-sized partitions of length κ bits each. Each partition is then mapped into a neuron in its corresponding cluster using a direct binary-to-integer mapping from the tag portion to the index of the neuron to be activated. Thus l = 2κ . If l is a given parameter, the number of clusters is calculated to be c = q/ log2 (l). There are no connections within the neurons and clusters inside PI and it should be remembered .

In order to exploit the prominent feature of the CN-based associative memory in the classification of the search data, a conventional CAM array is divided into sufficient number of compared enabled sub-blocks such that: 1) the number of sub blocks are not too many to expand the layout and to complicate the interconnections and 2) the number of sub-blocks should not be too few to be able to exploit to energy-saving opportunity with the SCN-based classifier. Consequently, the neurons in PII are grouped and ORed as shown in Fig to construct the compare-enable signal(s) for the CAM array. Even the conventional CAM arrays need to be divided into multiple sub-blocks since long bit lines and SLs can slow down the read, write, and search operations due to the presence of drain,gate, and wire capacitances.

IV.RESULTS



V.CONCLUSION

In this paper, a low-power Content Addressable Memory (CAM) is introduced. The proposed architecture employs a novel associativity mechanism based on a recently developed family of neural-network-based associative memories. This architecture is suitable for low-power applications where frequent and parallel look-up operations are required. The proposed architecture employs a clustered-neural-network module which is connected to several independently-compare-enabled CAM sub-blocks. With optimized lengths of the reduced length tags, the network will eliminate most of the comparisons given a uniformly random distribution of the reduced length inputs. Non uniformly will cost power but will not affect accuracy. Conventional NAND and NOR-type architectures were also implemented for comparison purposes.

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