

Design an Aging Aware Hybrid Logic Level Multiplier

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ABSTRACT: This paper presents the design of a Hybrid logic level [H.L.L] multiplier for 32*32bit number multiplication. Modern computer system is a dedicated and very high speed unique multiplier. Therefore, this paper presents the design a Hybrid logic level multiplier. The proposed system generates M, N and interconnected blocks. By extending bit of the operands and generating an additional product the Hybrid logic level multiplier is obtained. Multiplication operation is performed by the Hybrid logic level is efficient with the less area and it reduces delay i.e., speed is increased.

Keywords: H.L.L, partial products, Hybrid level logic unit.

I.INTRODUCTION

In most signal processing algorithms multiplication is the fundamental operation. Multipliers have large area, long latency and consume considerable power. The important part in low-power VLSI system design is low power multiplier design. There has been extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally determined by the performance of the multiplier because the multiplier is generally the slowest element in the system.

Furthermore, it is generally the most area consuming .Hence, optimizing the speed and area of the multiplier is a major design issue. However, conflicting constraints are usually area and speed so that improving speed results mostly in larger areas. As a result, a whole spectrum of multipliers with different area-speed constraints has been designed with fully parallel.

For digital signal processing (DSP) applications such as for multimedia and communication systems the high speed multipliers and pipelined multipliers are used. High speed DSP computation applications such as Fast Fourier transform (FFT) require additions and multiplications.

II.LITERATURE SURVEY

An irregular partial product array is generated by the conventional modified encoding(MBE) Booth because of the extra partial product bit at the least significant bit position of each partial product row. A simple approach in paper [4] is presented to generate a regular partial product array with fewer partial product rows and negligible overhead, thereby reducing the area, lowering the complexity of partial product reduction delay, and power of MBE multipliers. But the drawback of this multiplier is that it function only for signed

number operands.

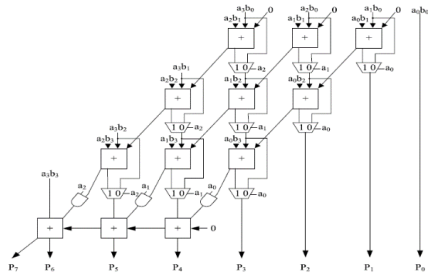


FIG. 1: EXISTED SYSTEM

The improvement on the normal array multiplier (AM) is by column-by passing multiplier. The multiplier array consists of $(n-1)$ rows of carry save adder (CSA), in which each row contains $(n-1)$ full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation.

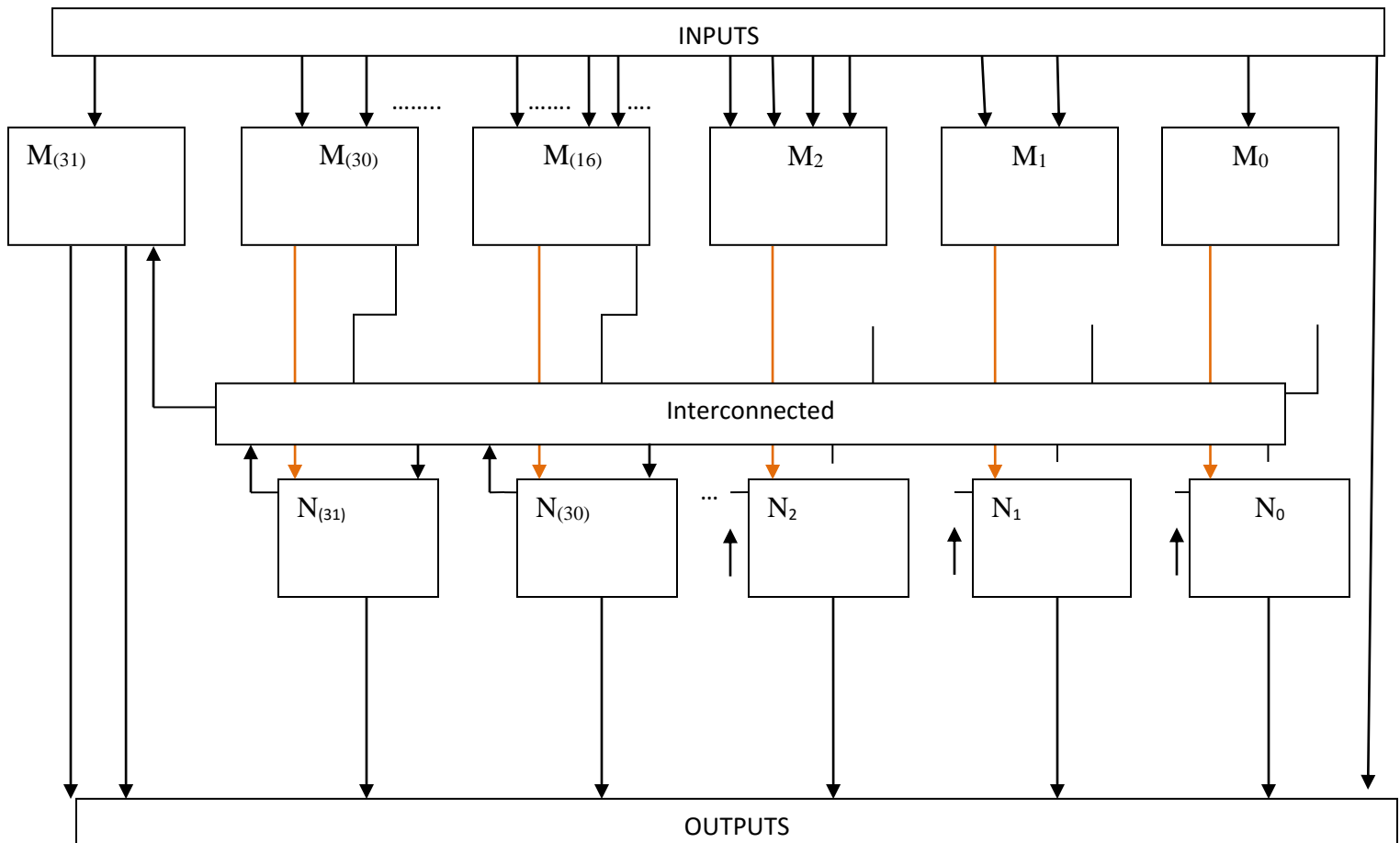


Fig. 2 32*32 HIGH PERFORMANCE HYBRID LOGIC LEVEL MULTIPLIER

III. PROPOSED SYSTEM

The gates in the Hybrid logic level [H.L.L] multiplier are always active regard of input logics. In, Hybrid logic level [H.L.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 2 shows a 32*32 Hybrid logic level [H.L.L] multiplier, it can be seen that the M_0, M_1, \dots, M_n done their operations and the outputs are passed to interconnected

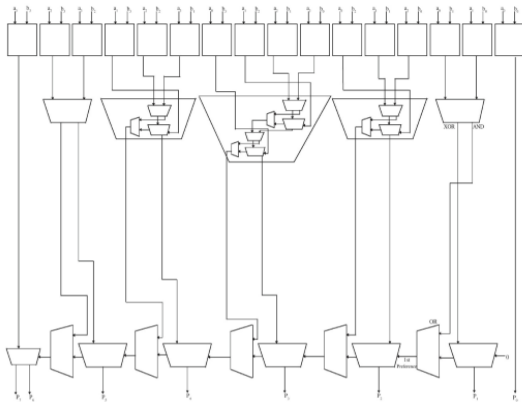


FIG. 3 PROPOSED SYSTEM [4*4 D.L.L]

Block and N-Block simultaneously. Depends on the preference of operation the Hybrid level logic gives the N-block output to interconnected block and vice versa.

Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit. The above fig. 3 shows the 4*4 high performance Hybrid logic level multiplier reduced the timing waste occurring in traditional circuits that use the critical path cycle as an execution cycle period. The basic concept is to execute a shorter path using Hybrid logic. Since

most paths execute in a cycle period that is much smaller than the critical path delay.

IV. RESULTS

To reduce the number of partial product rows to be added hybrid logic level has been adopted in multipliers, thus reducing the size and enhancing the speed of the reduction tree. The least significant bit position of each partial product row encoding, leading to an irregular partial product array and a complex reduction tree. Therefore, the Hybrid logic level multipliers with partial product array produce a very high speed.

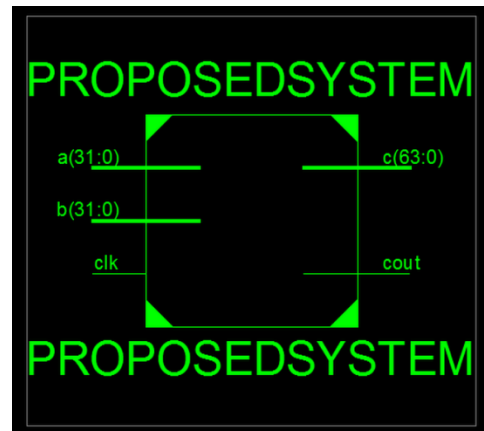


FIG. 4 R.T.L SCHEMATIC

The above fig. 4 shows the R.T.L schematic of high performance Hybrid logic level multiplier and fig. 5 shows the technical schematic one of the LUT block of high performance Hybrid logic level multiplier.

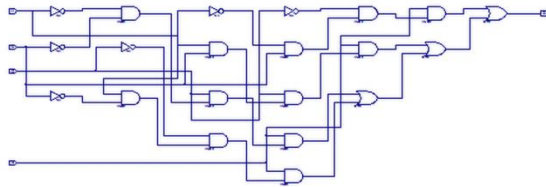


FIG. 5 LUT IN TECHNICAL SCHEMATIC

The below figure 6 shows the output waveform of 32*32 bit Hybrid logic level multiplier.

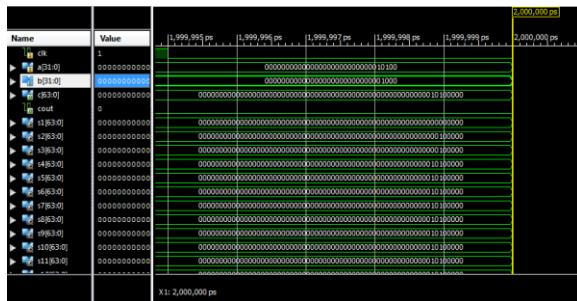


FIG. 6 OUTPUT WAVEFORMS

The below table 1 shows the comparison of existed system 32*32 and proposed system 32*32 with area and delay

System/parameter	Area[kb]	Delay[ns]
Existed System	316352	126.865
Proposed system	272000	110.363

TABLE.1 COMPARISON TABLE

The above comparison table shows that area of the proposed system is less than existed system and delay is also efficient.

V.CONCLUSION

The proposed system generates M, N and interconnected block. The each block consists of gates and the row in the architecture is lesser than existed multiplier.

By generating a product with Hybrid logic level multiplier 32*32 is obtained. Multiplication operation is performed by the Hybrid logic level unit is better performance than existed multiplier. The required hardware and the chip memory reduces and it reduces delay i.e., speed is increased.

VI.REFERENCES

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