International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 06
May 2017

DESIGN OF HIGH SPEED TRUNCATED PARALLEL PREFIX ADDER

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Abstract: In this paper discussed about a carry skip adder (CSKA) structure with P.P.A compared with the conventional adder. A parallel-prefix adder gives the best performance in VLSI design. However, performance of P.P.A adder through black cell takes huge memory. So, gray cell can be replaced instead of black cell which gives the Efficiency in P.P. Adder. The proposed system consists of three stages of operations they are pre-processing stage, carry generation stage, post-processing stage. The pre-processing stage focuses on propagate and generate, carry generation stage focuses on carry skip generation and post-processing stage focuses on final result.

Index Terms—Carry skip adder (CSKA), energy efficient, high performance, hybrid variable latency adders, voltage scaling.

I. INTRODUCTION

Adders are a key building block in arithmetic and logic units (ALUs) and hence increasing their speed and reducing their power/energy consumption strongly affect the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported obviously, it is highly desirable to achieve higher speeds at low-power/energy consumptions, which is a challenge for the designers of general purpose processors.

One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage.

In this paper, given the attractive features of the CSKA structure, we have focused on reducing its delay by modifying its implementation based on the static CMOS logic. The concentration on the static CMOS originates from the desire to have a reliably operating circuit under a wide range of supply voltages in highly scaled technologies. The proposed modification increases the speed considerably while maintaining the low area and power consumption features of the CSKA. In addition, an adjustment of the structure, based on the variable latency technique, which in turn lowers the power consumption without considerably impacting the CSKA speed, is also presented. To the best of our knowledge, no work concentrating on design of CSKAs operating from the super threshold region down to near-threshold region and also, the design of (hybrid) variable latency CSKA structures have been reported in the literature. Hence, the contributions of this paper can be summarized as follows.

1) Proposing a modified CSKA structure by combining the concatenation and the incrimination schemes to the conventional

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CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The modification provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer.

2) Providing a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay.

3) Investigating the impact of voltage scaling on the efficiency of the proposed CSKA structure (from the nominal supply voltage to the near-threshold voltage).

4) Proposing a hybrid variable latency CSKA structure based on the extension of the suggested CSKA, by replacing some of the middle stages in its structure with a PPA, which is modified in this paper.

II. EXISTED SYSTEM

The existed hybrid variable latency CSKA structure is shown in Fig.1 where an *Mp*-bit modified PPA is used for the *p*th stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) among the stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest off-critical paths. Thus, the use of the fast PPA helps increasing the available slack time in the variable latency structure. It should be mentioned that since the input bits of the PPA block are used in the predictor block, this block becomes parts of both SLP1 and SLP2

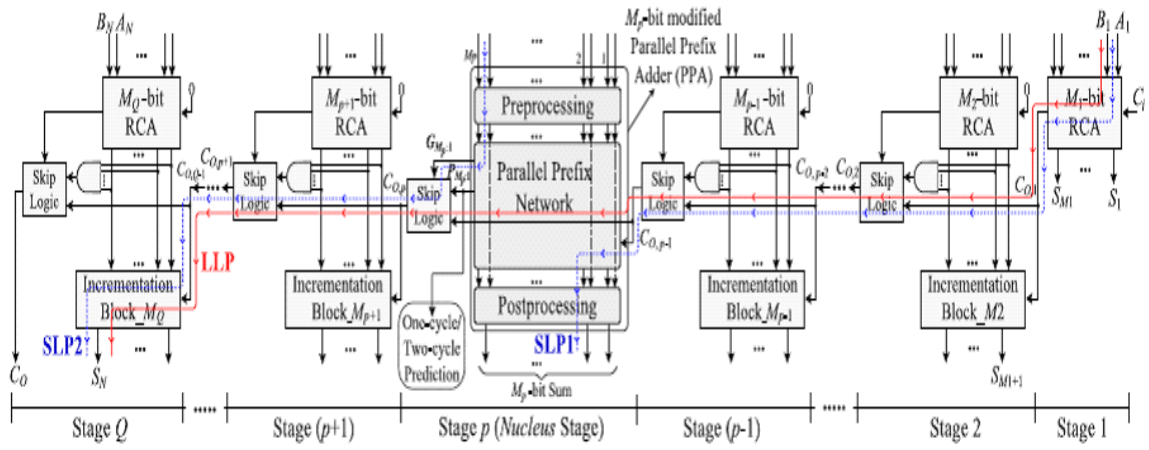

Fig.1 Structure of The Existed Hybrid Variable Latency

In the existed hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage (Fig. 2). One the advantages of this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout. The internal structure of the stage *p*, including the

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modified PPA and skip logic, is shown in Fig. 2. Note that, for this figure, the size of the PPA is assumed to be 8 (i.e., $Mp = 8$).

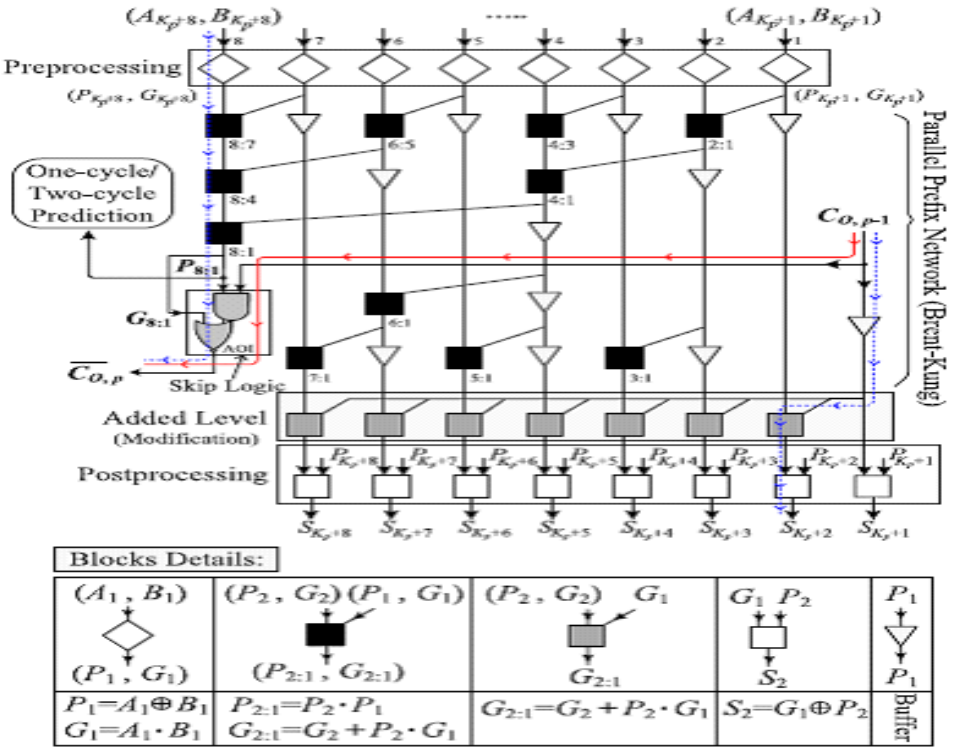

Fig.2 Internal structure of the *p*th stage of the existed hybrid variable latency CSKA.

As shown in the figure, in the pre processing level, the propagate signals (*Pi*) and generate signals (*Gi*) for the inputs are calculated. In the next level, using Brent–Kung parallel prefix network, the longest carry (i.e., *G*8:1*)* of the prefix network along with *P*8:1, which is the product of the all propagate signals of the inputs, are calculated sooner than other intermediate signals in this network. The signal *P*8:1 is used in the skip logic to determine if the carry output of the previous stage (i.e., *CO,p*−1*)* should be skipped or not. In addition, this signal is exploited as the predictor signal in the variable latency adder. It should be mentioned that all of these operations are performed in parallel with other stages. In the case, where *P*8:1 is one, *CO, p*−1 should skip this stage predicting that some critical paths are activated. On the other hand, when *P*8:1 is zero, *CO, p* is equal to the *G*8:1. In addition, no critical path will be activated in this case.

After the parallel prefix network, the intermediate carries, which are functions of *CO,p*−1 and intermediate signals, are computed (Fig. 2). Finally, in the post processing level, the output sums of this stage are calculated. It should be noted that this implementation is based on the similar ideas of the concatenation and incrimination concepts used in the CI-CSKA. It should be noted that the end part of the SPL1 path from *CO,p*−1 to final summation results of the PPA block and the beginning part of the SPL2 paths from inputs of this block to *CO, p*

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belong to the PPA block (Fig. 2). In addition, similar to the proposed CI-CSKA structure, the first point of SPL1 is the first input bit of the first stage, and the last point of SPL2 is the last bit of the sum output of the incrementation block of the stage *Q*. Since the PPA structure is more efficient when its size is equal to an integer power of two, we can select a larger size for the nucleus stage accordingly.

The larger size (number of bits), compared with that of the nucleus stage in the original CI-CSKA structure, leads to the decrease in the number of stages as well smaller delays for SLP1 and SLP2. Thus, the slack time increases further.

III. PROPOSED SYSTEM

In this system we use nuclear stages. In nuclear stages we have pre processing, parallel prefix network and post processing. One parallel prefix network is connected to other parallel prefix network through a skip logic. By using this proposed Hybrid Variable Latency the operation of the circuit is very fast.

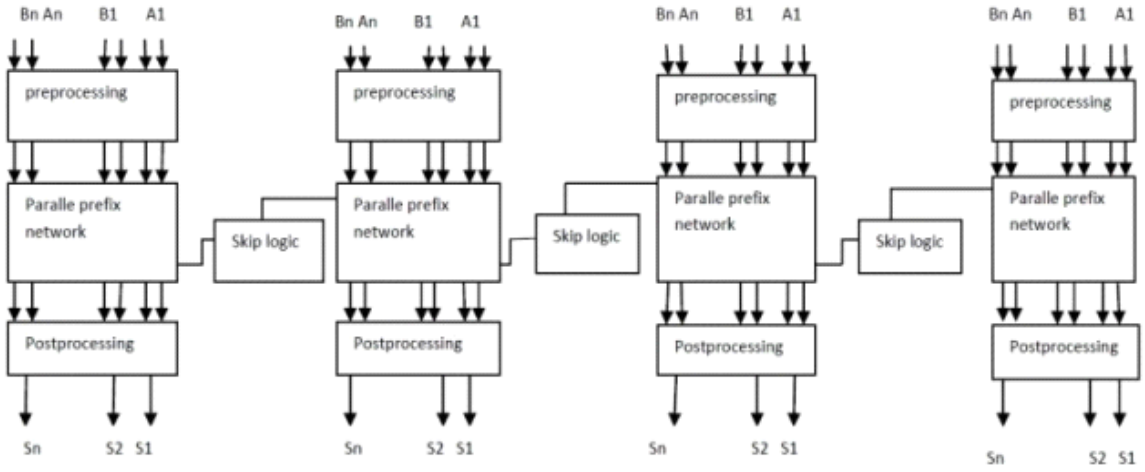

Fig.3 Structure of the proposed Hybrid Variable Latency

The skip logic is connected to interconnected blocks for every set of bits to make skipping operation at middle of the bits.

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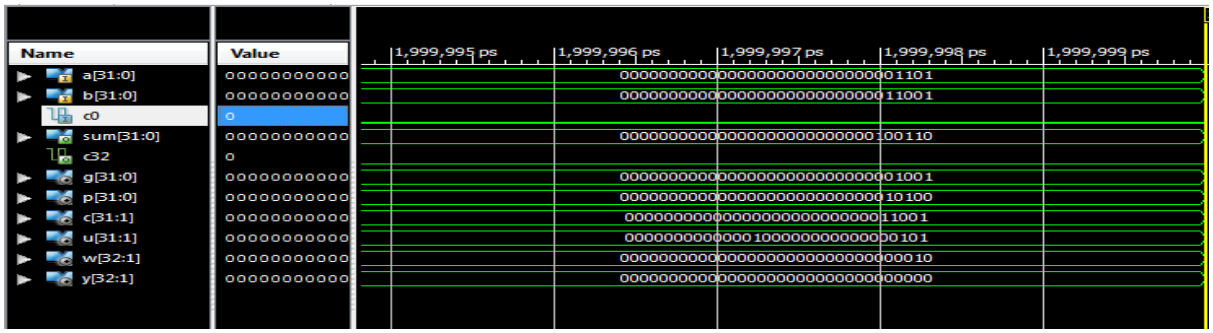
IV. RESULTS



V. CONCLUSION

In this paper, a static CMOS CSKA structure called CI-CSKA was proposed, which exhibits a higher speed and lower energy consumption compared with those of the conventional one. In this paper, a new approach to design a P.P adder concentrates on gate levels to improve the speed and decreases the memory. It is like tree structure and cells in the carry generation stage are decreased to speed up the binary addition. The proposed adder addition operation offers great advantage in reducing delay. The suggested structure showed the lowest delay and PDP making itself as a better candidate for high-speed low-energy applications.

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