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Multilevel Modular DC–DC Converter for (2n+1) Conversion Gain

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ABSTRACT

Recently, the interest in offshore wind farms has been increased significantly because of the stronger and more stable winds at sea, which will lead to a higher power production. DC/DC power conversion solutions are becoming more popular for fulfilling the growing challenges in the high voltage DC-connected offshore wind power industry. This paper presents several multilevel modular DC/DC conversion systems based on the capacitor-clamped module concept for high power offshore wind energy applications. Two types of the capacitor-clamped modules, the double-switch module and switchless module, are discussed. A soft-switching technique is adopted to achieve minimal switching losses and the maximum system efficiency. Theoretical analysis is carried out for the 2n+1 level cascaded configurations based on the capacitor-clamped modules. The inherent interleaving property of the proposed configurations effectively reduces the output voltage ripple without adding extra components. A cascaded hybrid topology is developed by the combination of double-switch and switchless modules. The proposed hybrid topology achieves higher efficiency and lower component count. The cascaded hybrid approach is evaluated in terms of the power device count, reliability, and efficiency against other high voltage DC/DC topologies to demonstrate its advantage for high voltage DC-connected offshore wind farms. The experimental results of two 5-kW prototype capacitor-clamped converters are presented to validate the theoretical analysis and principles as well as attest the feasibility of the proposed topologies.

Introduction

Wind energy systems have emerged as one of the most promising options among the renewable energy resource technologies to satisfy the growing urban and industrial demands. Offshore winds tend to blow harder and more uniformly than on land, providing the potential for increased electricity generation and steadier operation than land-based wind turbines. The reasonable economics of offshore wind farms are driving toward the development of larger wind turbines but high installation costs and maintenance difficulties are critical issues for minimizing the operating and maintenance (O&M) costs. With increasing distances from the shore, the wind turbine industry faces new challenges, such as long distance electrical transmission on high-voltage submarine cables and the reliability of turbine equipment. Therefore, an optimized design is needed to reduce the size and weight of the components, O&M costs, and power losses of offshore wind turbines.

With the increasing penetration of decentralized offshore wind generation into high voltage power grids, the transmission of electrical energy to the load centers is a major challenge. In this regard, larger wind turbines are leading to increased interest in high power DC/DC converters because of their rigid structure and easy controls . The DC/DC power converters raise the turbine output voltage to the high voltage (HV) level and to provide efficient transmission over long distances . High voltage transmission using DC technology allows decreases in power losses and cabling cost necessary for large current flow caused by the relatively low voltage of wind turbines. Alternatively, a higher output voltage could be advantageous in order to eliminate a step-up grid coupling transformer which is non-modular, heavy, and bulky . These bulky and huge electrical components incur high investment and maintenance costs due to more difficult erection, large cranes, lifting vessels, and equipment transportation from the shore to the installation sites.

One of the most important concerns for the converters used in offshore wind farms is their reliability due to the inherent lack of turbine access at sea. Using the modularity, if a single module fails, the converter can still function at a reduced power level. It is also feasible to localize any fault in the system; therefore, the system reliability can be improved. This feature facilitates easier maintenance and obtains a higher mean time between failures. In a modular structure, the total power handling can be allocated equally to multiple modules, allowing the use of cheaper components with low voltage/current stress in the system. Therefore, high power DC/DC conversion systems should be efficient, more compact, and highly reliable due to the more difficult equipment transportation from shore to the installation sites and maintainability of the wind turbines.

In this regard, step-up DC/DC power conversion systems were introduced for future wind farm DC layouts as shown in Fig. 1 to meet medium voltage (MV) DC and HVDC power requirements. Multiple-module boost converters were represented to achieve a high voltage conversion ratio for offshore wind energy applications connected to an HVDC line. Nevertheless, because of the large duty ratio of the main switch to achieve high voltage gain, the switching frequency is limited to reduce losses and obtain sufficient turn-off time for switches. Therefore, increasing the size of the passive components, such as boost inductors and filter capacitors, is inevitable due to the low switching frequency. In step-up resonant (SR) converter was introduced for MVDC levels, in which only one inductor and a single capacitor are used to achieve the high voltage gain and provide a soft-switching technique for the main switches. However, the converter suffers from large power device conduction losses and a high peak-to-peak voltage across the passive components. Moreover, these topologies have a non-modular structure that tends to increase the O&M costs at locations where the marine turbine accessibility is limited.

Module Structure

Fig. 5.1 presents a SL-based module, where a five-port system consists of two top and bottom cells. Each cell includes two capacitors, one inductor, and two diodes. The DS-based module is depicted in Fig. 5.2, which is a six-port system with two cells in the top and bottom of the module. Each cell of the DS-based module is composed of a single active switch, one diode, one inductor, and one capacitor. Fig. 5.3, 5.4 shows the 2n+1 level cascaded

configurations of the SL- and DS-based modules. For the cascaded SL-based circuit, an input module is connected to module #1, as shown in Fig. 5.3. For the cascaded DS-based topology, ports 5 and 6 of module #n are connected to an output module that consists of two capacitors and two diodes (see Fig. 5.4).

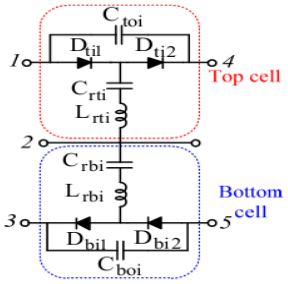


Fig: 5.1 Structure of SL-based module

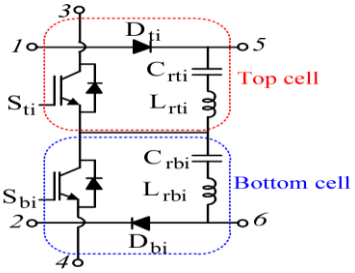


Fig: 5.2: Structure of DS-based module

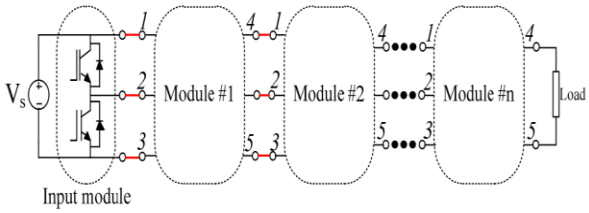


Fig: 5.3 SL-based module for 2n+1 level cascaded configurations.

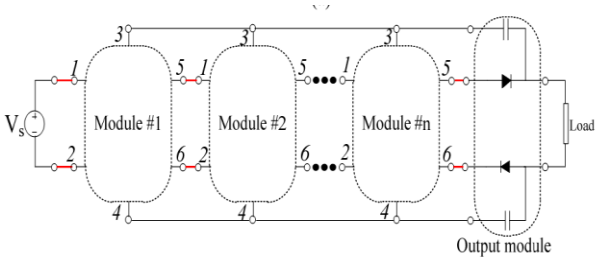


Fig: 5.4. DS-based module for 2n+1 level cascaded configurations.

5.2 Operating Principles of the MRCC Voltage Tripler Converter

To understand the operational principle, the MRCC voltage tripler converter is selected as the topology under analysis. Fig. 5.5 shows the MRCC voltage tripler converter based on an SL module and a DS module. The MRCC converter consists of an SL-based module indicated by a red-colored box and an input module, as shown in Fig. 5.5. The MRCC voltage tripler can also be realized with a DS-based module represented by a blue-colored box and an output module (see Fig. 5.6).

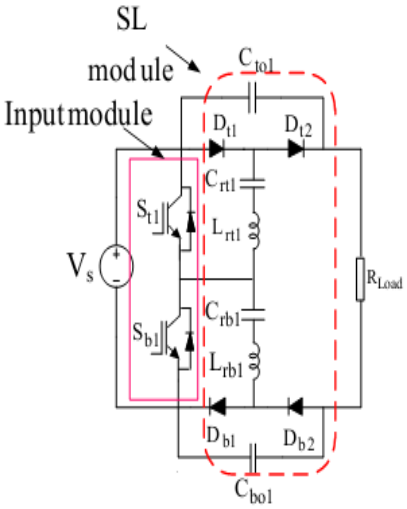


Fig: 5.5. Structure of MRCC voltage Tripler converter with SL-based module

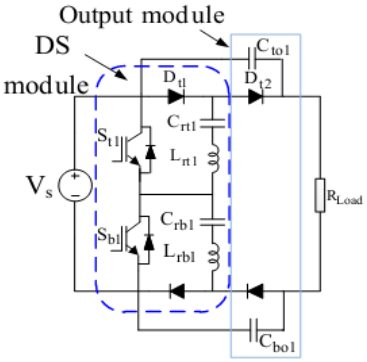


Fig: 5.6. Structure of MRCC voltage Tripler

converter with DS-based module

Therefore, both SL- and DS-based configurations have the same circuit for the voltage tripler converter. The active switches, Sb1 and St1, are controlled complementarily with a same duty cycle to minimize the conduction losses for the power devices and passive components 19. To simplify the analysis, the following assumptions are made:

1. All the switches, diodes, capacitors, and inductors are ideal;
2. The output capacitors, Cto1 and Cbo1, are large enough to be considered as voltage sources;
3. Two resonant inductors, Lrt1 and Lrb1, have the same inductances;
4. The resonant capacitors, Crt1 and Crb1, have identical values;
5. Vs is an ideal DC voltage source and the load is modelled by a pure resistor (Rload); and
6. The switching frequency is less than the resonant frequency to set aside enough dead time for two main switches and achieve a zero-current switching (ZCS). Therefore, the short time interval t1-t2 and t3-t4 are defined as the dead times between active switches to avoid a short circuit in each module.

1) State I t0-t1 Fig. 5.7

In the beginning of this mode (t = t0), the bottom switch, Sb1, is ON, whereas St1 is OFF in the top cell. The charging current flows through Dt1 and Sb1, as shown in Fig. 5.7. Therefore, Crt1 is charged by Vs, whereas Crb1 is discharged to Cto1 (Crb1 was previously charged at the input voltage level in Mode III) through the resonant loops (see Fig. 5.10 (f)). The energy of Rload is supplied by Cto1 and Crb1. At t = t1, Sb1 can be OFF under the zero-current condition (see Fig. 5.10(d)). The state equations of operating State I are

$$V_s = L_{rt1}\frac{di_{L_{rt1}}}{dt} + v_{C_{rt1}} \qquad 5.1$$

$$i_{L_{rt1}} = C_{rt1}\frac{dv_{C_{rt1}}}{dt} \qquad 5.2$$

By ignoring the impact of the short times, t1 < t < t2 and t3 < t < t4, it can be assumed that $t_0 = 0$, $t_1 = t2 \ll Ts/2$, and $t3 = t4 \ll Ts$. The initial conditions of (5.1) and (5.2) are

$$V_{Crt1}(0) = V_s - \frac{\pi P_o}{V_o C_{rt1}\omega_r}$$

and $I_L(0)=0$. Therefore, solving (5.1) and (5.2) gives the following:

$$i_{L_{rt1}}(t) = \frac{\pi P_o}{V_o}\sin(\omega_r t), \qquad 5.3$$

$$v_{C_{rt1}}(t) = V_s - \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t), \qquad 5.4$$

The state equations of the operating State I for the resonant capacitor and inductor in the bottom cell can be expressed as

$$v_{C_{bo1}} = L_{rb1}\frac{di_{L_{rb1}}}{dt} + v_{C_{rb1}} \qquad 5.5$$

$$i_{L_{rb1}} = C_{rb1}\frac{dv_{C_{rb1}}}{dt}, \quad 5.6$$

$$\frac{P_o}{V_o} + C_{bo1}\frac{dv_{C_{bo1}}}{dt} + i_{L_{rb1}} = 0. \quad 5.7$$

$$i_{L_{rt1}}(t) = -\frac{\pi P_o}{V_o}\sin(\omega_r t), \quad 5.8$$

$$v_{C_{rb1}}(t) = V_s + \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t) \quad 5.9$$

Equations (5.8) and (5.9) show that capacitor Crb1 is discharged in this mode (see Fig. 5.10(f)).

Fig: 5.7. Operating circuits in stages: Stage I t0—t1

2) State II t1-t2 Fig. 5.8

In this state, all the switches are turned OFF. The diodes are reversed-biased and the resonances stop, as shown in Fig. 5.8(b). Therefore, the inductor currents become zero (see Fig. 5.10(c)).

The resonant capacitor voltages of Crt1 and Crb2 are unchanged. Cto is connected in series to Cbo and both are discharged to the load terminal.

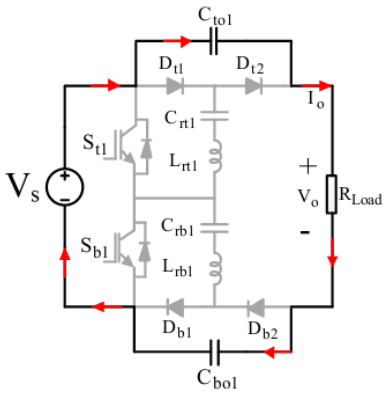


Fig: 5.8. Operating circuits in stages: Stage II t1—t2

3) State III t2-t3 Fig. 5.9

After a half period of the resonant frequency, St1 is turned ON while Sb1 is OFF. The diodes Dt1 and Db2 are reverse-biased by the capacitor voltages.

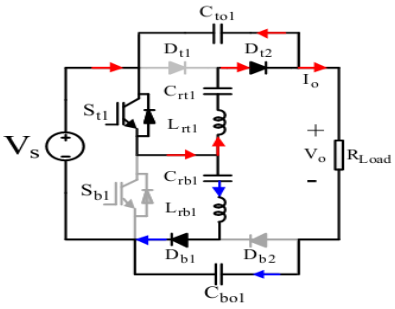


Fig: 5.9. Operating circuits in stages: Stage III t2—t3

Fig. 5.10(e) shows that the current through St1, is increased by a soft-switching operation with a half-cycle resonant shape. In this state, Crb1 is charged, whereas Crt1 is discharged through two resonant loops, as shown in Fig. 5.10. At time t3, St1 becomes OFF under the zero-current condition. This process can also be described mathematically as follows:

$$V_s = L_{rb1}\frac{di_{L_{rb1}}}{dt} + v_{C_{rb1}} \qquad 5.10$$

$$i_{L_{rb1}} = C_{rb1}\frac{dv_{C_{rb1}}}{dt} \qquad 5.11$$

$$v_{C_{to1}} = L_{rt1}\frac{di_{L_{rt1}}}{dt} + v_{C_{rt1}} \qquad 5.12$$

$$\frac{P_o}{V_o} + C_{to1}\frac{dv_{C_{to1}}}{dt} + i_{L_{rt1}} = 0 \qquad 5.13$$

Therefore, in this state, the capacitor voltages and inductor currents can be obtained as follows

$$i_{L_{rb1}}(t) = \frac{\pi P_o}{V_o}\sin(\omega_r t) \qquad 5.14$$

$$v_{C_{rb1}}(t) = V_s - \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t) \qquad 5.15$$

$$i_{L_{rt1}}(t) = -\frac{\pi P_o}{V_o}\sin(\omega_r t) \qquad 5.16$$

$$v_{C_{rt1}}(t) = V_s + \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t) \qquad 5.17$$

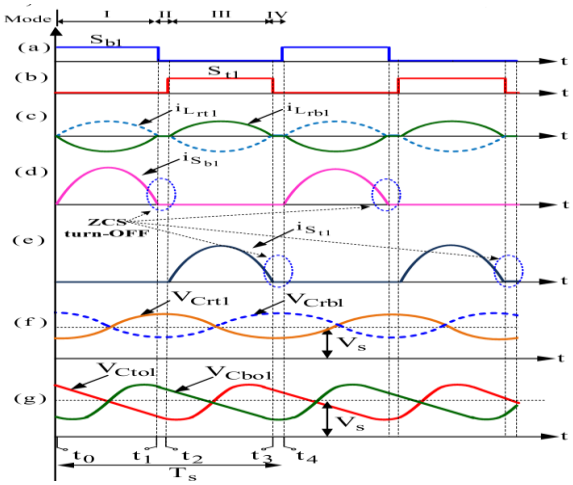


Fig: 5.10. Key current and voltage waveforms of the MRCC voltage Tripler converter.

It can be clearly observed from theoretical analysis and the operating principle of the MRCC converter that all the power devices and passive components have the same voltage and current stresses in this circuit.

4) State IV t3-t4 Fig. 5.8

The operation of this state is similar to that of State II.

5.3 Operating Principles of the 2n+1 level Cascaded SL- and DS-based Configurations

With the same principle, Figs. 5.11 to 5.14 show the 2n+1 level cascaded SL- and DS-based topologies, respectively. Note that n is an even number in Fig. 5.13 and 5.14.

5.3.1 Cascaded SL-based configuration

State I Fig. 5.11: During the period of t0 to t1, the bottom switch Sb is ON, whereas St is OFF. In each top cell, the diodes Dti1s (i=1, 2, ..., n) are forward-biased by Vs and Ctois. Therefore, Crtis are charged by Vs and Ctois (i=1, 2, ..., n-1), as shown in Fig. 7(a). In this state, Cton is discharged to the load. In contrast, in the bottom cells, Crbis are discharged to the output capacitors, Cbois. For the general 2n+1 level cascaded SL-based topology, the currents through the top and bottom capacitors are

$$i_{C_{rti}}(t) = \frac{\pi P_o}{V_o}\sin(\omega_r t) \quad (i = 1,2,...,n), \tag{5.18}$$

$$i_{C_{rbi}}(t) = -\frac{\pi P_o}{V_o}\sin(\omega_r t) \quad (i = 1,2,...,n). \tag{5.19}$$

$$v_{C_{rti}}(t) = iV_s - \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t) \quad (i = 1,2,...,n), \tag{5.20}$$

$$v_{C_{rbi}}(t) = iV_s + \frac{\pi P_o}{V_o C_{rt1}\omega_r}\cos(\omega_r t) \quad (i = 1,2,...,n). \tag{5.21}$$

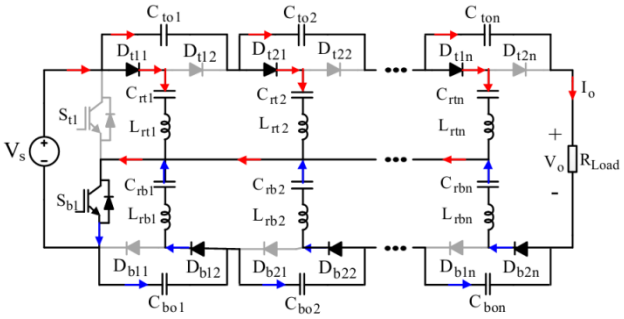


Fig: 5.11. Operation states of the 2n+1 level cascaded SL-based topology State – I

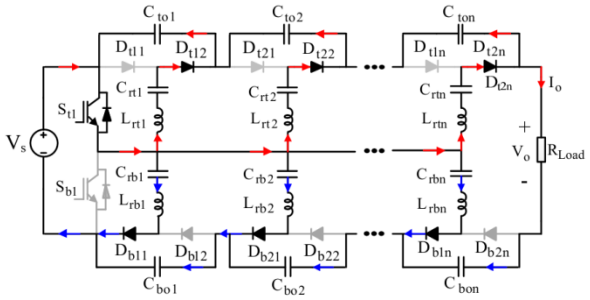


Fig: 5.12. Operation states of the 2n+1 level cascaded SL-based topology State – III

State III Fig. 5.9: State III begins when the top switch St is in the ON-state and Sb is in the OFF-state at t0. The top diodes Dti2s and bottom diodes Dbi1s are forward-biased, as shown in Fig. 7(b). In the bottom cells, Crbis are charged by Vs and Cbois (i=1, 2, ..., n-1), whereas Crtis are discharged to Ctois. As a result, the voltages of Crbis are equal to i times the input voltage level.

5.3.2 Cascaded DS-based configuration

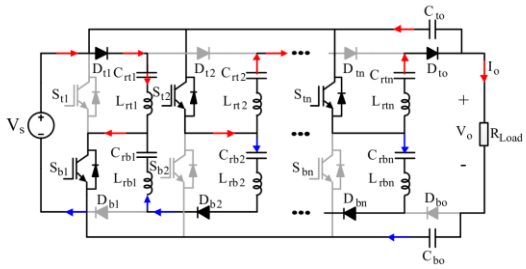
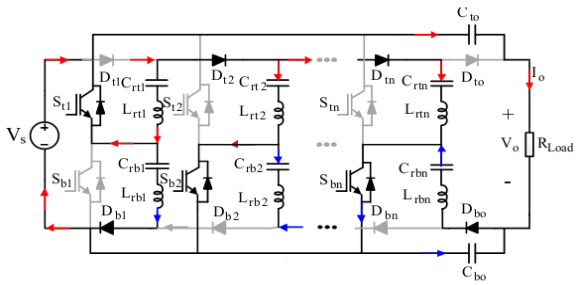


Fig: 5.13. Operation states of the 2n+1 level cascaded DS-based topology State I

State I Fig. 5.13: At t = t0, Sbi (i=1, 3, ... n-1) and Sti (i=2, 4, ..., n) are turned ON, whereas Sbi (i=even) and Sti (i=odd) are OFF in the top and bottom cells. Therefore, in the top and bottom cells, the odd numbered Crtis and even numbered Crbis are charged by Vs, Crtis (i=2, 4,..., n), and Crbis (i=1, 3, .,., n-1). In this state, the output capacitor Cto is charged by Crtn, whereas Cbo is discharged to the load, as shown in Fig. 5.13.

State III Fig.5.14: During this time interval, Sbis (i=1, 3, .,., n-1) and Stis (i=2, 4, ..., n) are OFF, whereas Sbis (for i even) and Stis (for i odd) are ON. Therefore, in the top cells, Crtis (i=1, 3 .,., n-1) are discharged to Crtis (i=2, 4, ..., n). On the other hand, the odd numbered Crbis are charged by Vs and the even numbered Crbis.



6.0 **Simulation & Results**

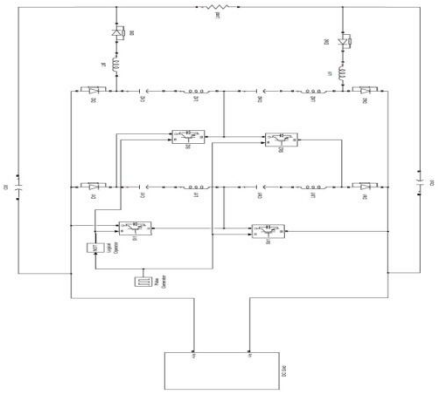


Fig: 6.1. MATLAB Based Simulation model of circuit under analysis

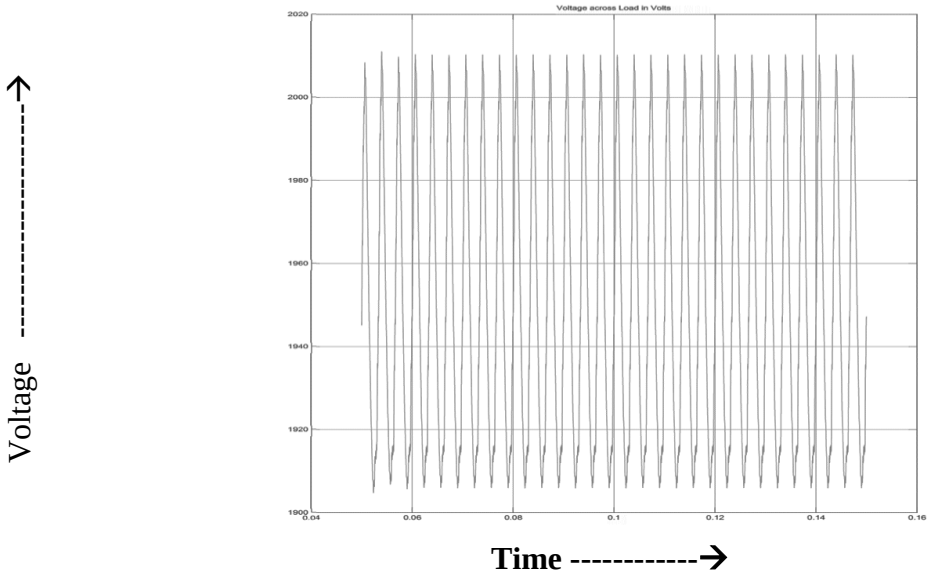


Fig: 6.2. Voltage Across Load in Volts

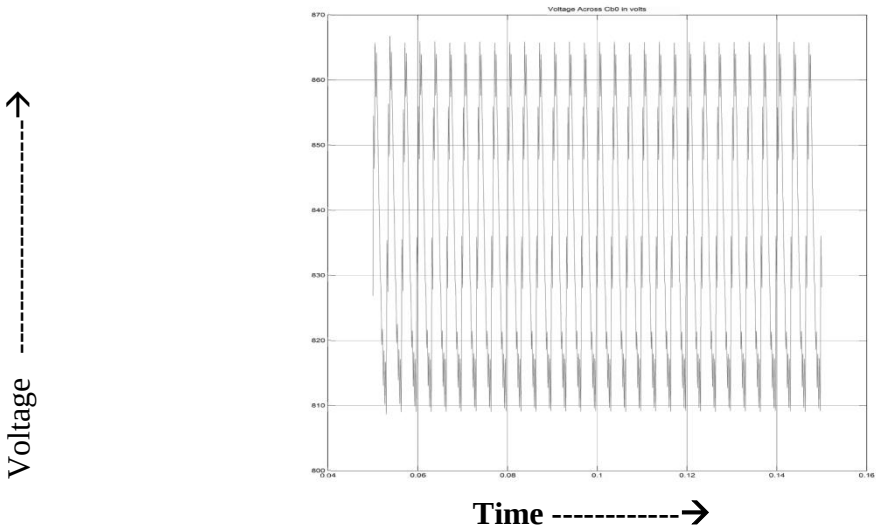


Fig: 6.3. Voltage Across Cb0 in Volts

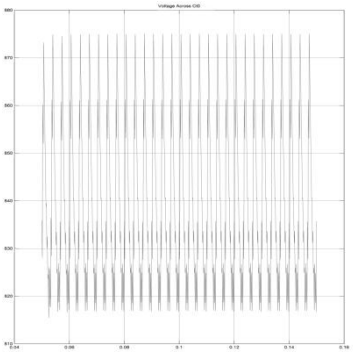


Fig: 6.4. Voltage Across Ct0 in Volts

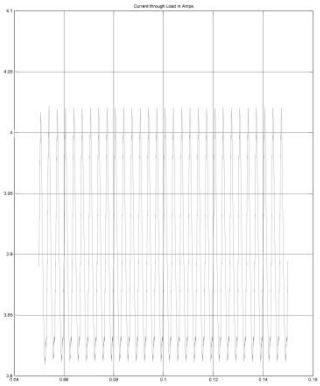


Fig: 6.5. Current through Load in Amps

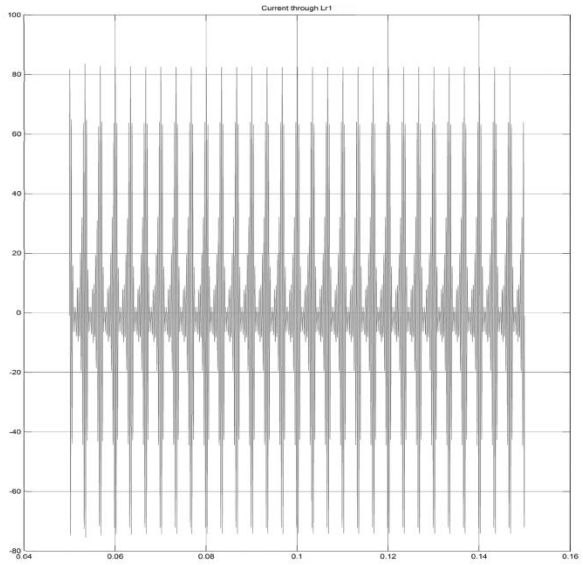


Fig: 6.6. Current through Lr1 in Amps

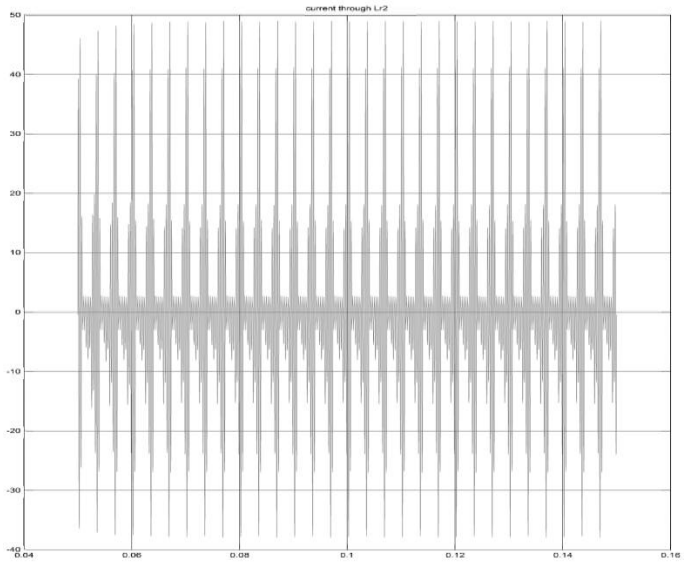


Fig: 6.7. Current through Lr2 in Amps

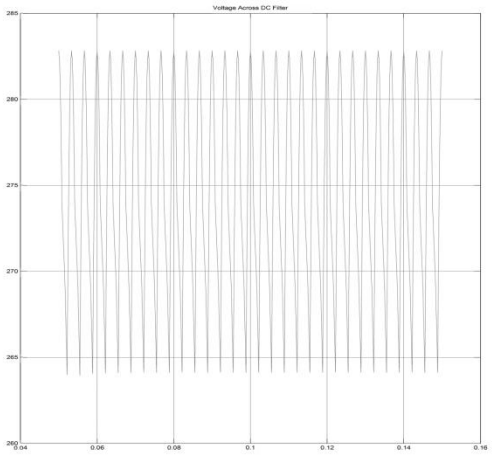


Fig: 6.8. Voltage across DC Filter in Volts

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