International Journal of Research
Available at https://edupediapublications.org/journals
p-ISSN: 2348-6848
e-ISSN: 2348-795X
Volume 04 Issue 06
May 2017

Switched Capacitor Based Two Switch Boost Converter for High Gain Applications

J BHANU KATYAYANI[1], S.RAJASEKHAR[2]

[1] **M.Tech Scholar, Dept of EEE, ASR College of Engineering and Technology, JNTUK, A.P**

[2] **Assistant Professor, Dept of EEE, ASR College of Engineering and Technology, JNTUK, A.P**

ABSTRACT

A family of "Two-switch Boosting Switched capacitor Converters (TBSC)" is introduced, which distinguishes itself from the prior arts by symmetrically interleaved operation, reduced output ripple, low yet even voltage stress on components, and systematic expandability. Along with the topologies, a modeling method is formulated, which provokes the converter regulation method through duty cycle and frequency adjustment. In addition, the paper also provides guidance for circuit components and parameter selection. A1KW 3X TBSC was built to demonstrate the converter feasibility, regulation capability via duty cycle and frequency, which achieved a peak efficiency of 97.5% at the rated power.

INTRODUCTION:

Switched Capacitor (SC) converter is an important branch of power electronics converters which is composed of capacitors and switches without the participation of inductors/transformers. It potentially has lower electromagnetic interference (EMI), lighter weight, lower cost, higher energy density, and the potential for full integration However, there are some intrinsic features related to SC converters as well as challenges in developing SC converters need to be recognized. First of all, the efficiency of SC converter is closely related to voltage gain Thus, when a voltage gain requirement and load range are given, it is essential to pair it with a proper topology and circuit parameters in order to achieve high efficiency. Additionally, pulsating input current and weak regulation capability is some of the weaknesses to overcome before SC converter can be widely dopted. It is desirable to develop SC converters with simple circuit structure, minimized pulsating input current, small output voltage ripple, good regulation capability, and scalability for power and gain.

Inspired by the work reported in the above-mentioned this project, a “Two-Switch Boosting Switched-capacitor Converter (TBSC) family” for unidirectional power conversion is proposed in this paper, with detailed evolution procedure starting from a

double switch core. It inherits s o m e of the advantages o f traditional ladder converter, but the proposed circuit provides symmetrical properties. Along with the topologies, duty cycle and frequency regulation are provoked through proposed model. The proposed TBSC

Family characterizes itself by following aspects:

1. Symmetrical structure with automatic interleaving operation.
2. Uncommon ground between input and output.
3. Capability of pulse width modulation and frequency modulation for output voltage.
4. Comparatively Low voltage rating of all components.
5. Flexible gain extension for different gain applications

PROPOSED TBSC FAMILY AND OPERATION

The proposed TBSC family contains n members, where n=1,2, 3 ... The first member is the 1X TBSC as shown in Figure 2.5 (a). It is merely a two-switch 3-terminal network with terminal0, 1, and 1'; nevertheless, it is the core to build the entire TBSC family. For all TBSC members, terminal 1-1' is defined as the low side, while terminal n-n', high side.

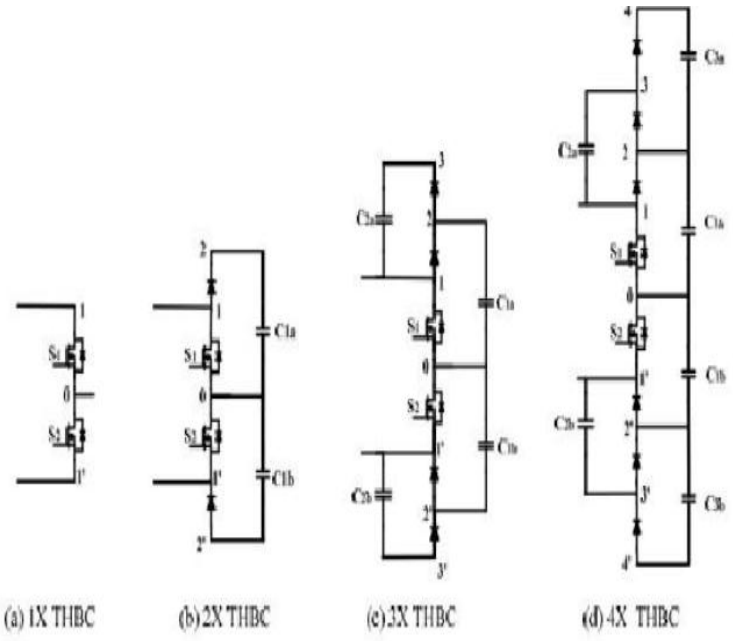


Figure 2.5 The proposed TBSC family

In order to obtain the second member in the TBSC family, a pair of n=2 gain-extension networks, the top one with terminals0, 1,and 2 and the bottom one with terminals 0', 1', and 2' as shown in figure Fig. 2 are added to the 1X TBSC

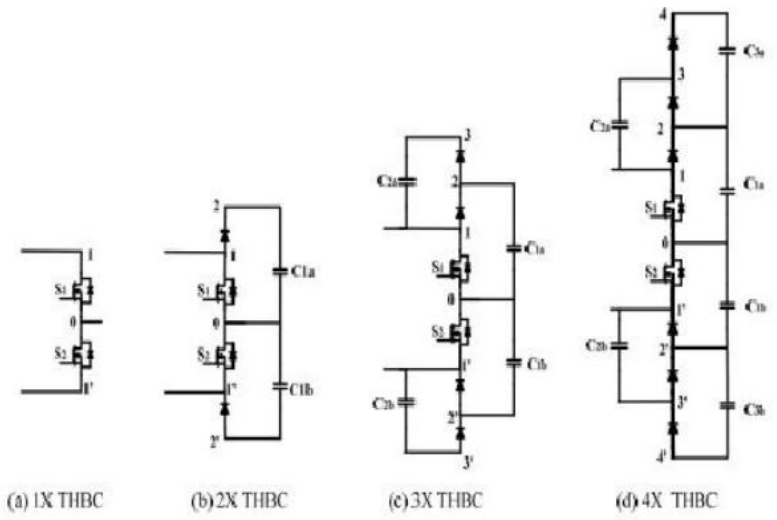


Figure 2.5(a).

F i g u r e 2 . 5 (a) By connecting the matching terminals of the gain-extension network and the 1X TBSC, the 2X TBSC is derived

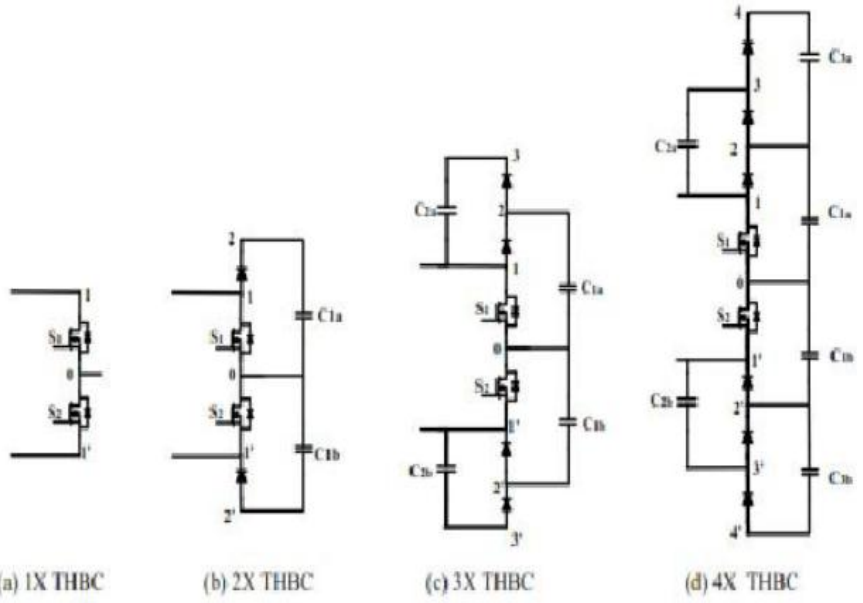


Figure 2.5(b).

Fig 2.5(b) The voltage at the high side of the 2X TBSC configurations is double of that of the low side under the case of no load and idea components (ideal condition), by operating the two switches S1 and S2 in an interleaved manner.

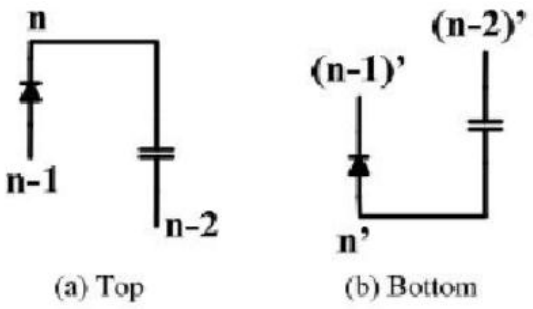


Figure 2.6 Gain-extension network (n=2, 4, 6…)

Further by adding a pair of n=3 gain-extension networks as shown in Fig. 2.6 to the 2X TBSC in a similar fashion, the 3X TBSC

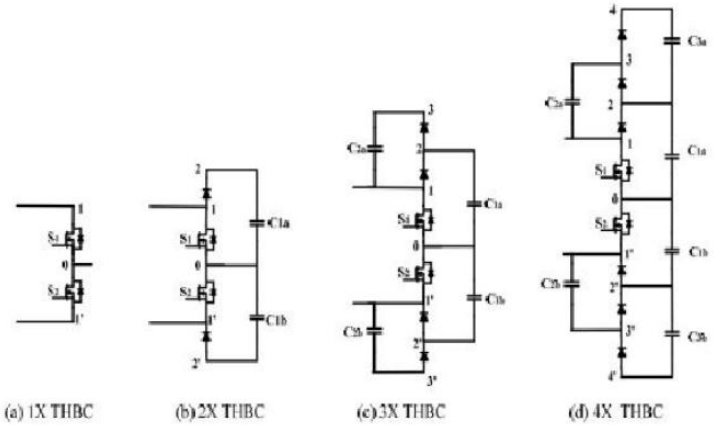


Figure 2.5 (c)

Fig. 2.5 (c). The new configuration triples the low-side voltage by operating the two active switches S1 and S2 in an interleaved manner under ideal condition.

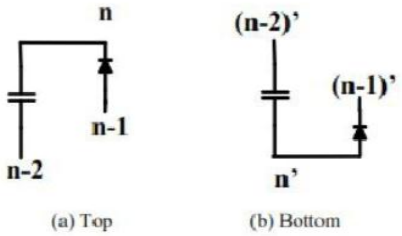


Figure 2.6 Gain-extension network

Fig. 2.7 Gain-extension network (n=3, 5, 7…) To synthesize the 4X TBSC topology, a pair of n=4 gain-extension networks in Fig. 2 are added to the 3X TBSC topology in a similar fashion. Thus, a new member with 4X gain

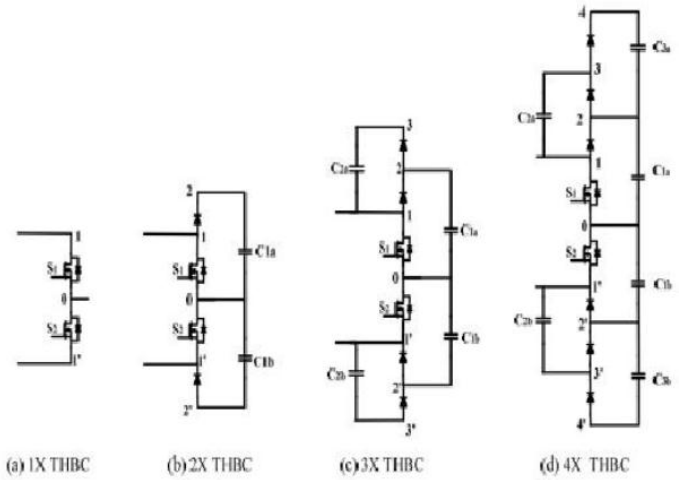


Figure 2.7

This process can continue indefinitely to obtain a TBSC with an ideal gain of arbitrary positive digital number n, by applying gain-extension network. In general, in order to obtain nX TBSC, a pair of 3-terminal gain-extension networks, the top one with terminals n-2, n-1, and n and the bottom one with terminals (n-2)', (n-1)', and n', as shown in Fig. 2 or Fig. 3, are added to the (n-1)X TBSC. By connecting the matching terminals of the gain-extension network to the (n-1) X TBSC, the nX TBSC configuration is derived. The voltage at the high side is n times of the low-side voltage (applied to terminal 1 and 1') by operating the two active switches S1 and S2 in an interleaved manner under ideal condition. Due to the symmetrical interleaved configuration of the circuit, the output voltage ripple is reduced.

Additionally, all components voltage rating is set by low side voltage. In 2X TBSC and 3X TBSC are illustrated as example, and experimental results of 3X TBSC converters are given.

OPERATION OF 2X TBSC WITH PWM CONTROL:

A simple voltage doublers as second member of TBSC family is shown in Fig.2. 8, with source and load connected. Note that output filter capacitor is not necessary due to serial connection of a1C The C 1 b switch

S1 and S2 will be controlled by interleaved P W M si gnal des cri bed b y two top waveforms shown as Fig. 2.8(a). The "dead-time" which indicates the time period when both switches are off is controlled intentionally to modulate the output voltage. Therefore, four operation states will be observed during a period

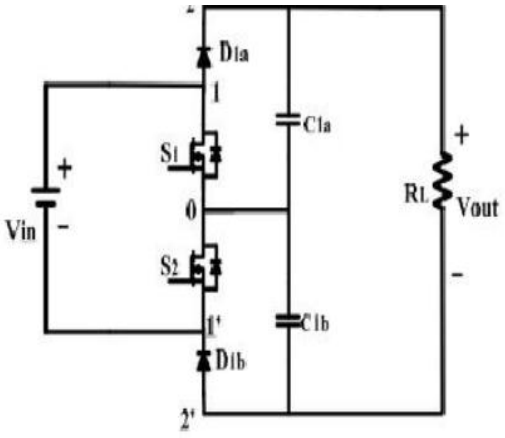


Figure. 2.8. Topology of 2X TBSC

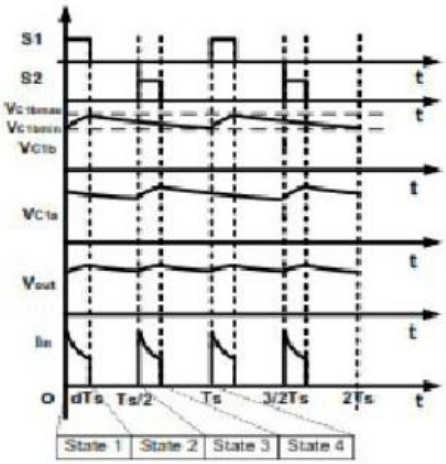


Figure2.8 (a) Key waveforms

State 1[0, dTs]:

Switch S1 is turned on during [0, dTs] while the duty cycle d is within the range of [0, 0.5]. When S1 is on, the energy from input source will partially charge C1b though D1b and partially provide the load current directly, Fig. 2.9. The output voltage equals to the sum of capacitor voltage Vc1a and Vc1b.

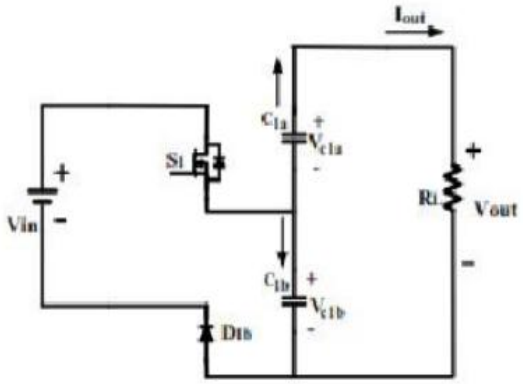


Figure 2.9 State-1

State 2[dTs, Ts/2]:

When S1 and S2 are both off, it comes to state 2 shown as Fig.2.10. Both diodes D1a and D2a become reversed biased and only capacitor C1a and C1b are connected in series to charge the load. Input current Iin becomes zero at this state.

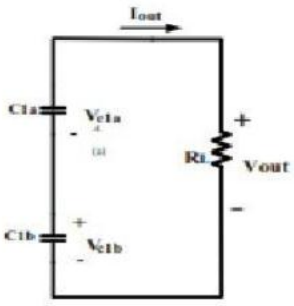


Figure 2.10 State-2

State 3[Ts/2, dTs+Ts/2]:

At this state, switch S2 is on while S1 is kept off, shown as Fig. 2.11. The energy from input source will be partially delivered to load and partially used to charge capacitor C1a.

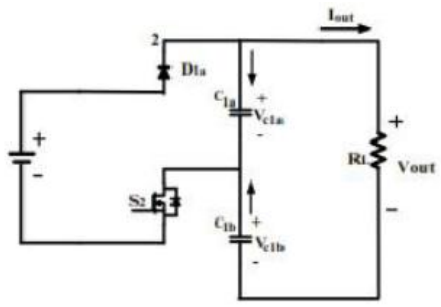


Figure 2.11 State-3

State 4[dTs+Ts/2, Ts]

This state repeats state 2. By interleaved operation of S1 and S2, the input current ripple has the frequency twice of the switching frequency. Moreover, based on the automatic interleaved structure, the output voltage ripple is smaller due the ripple cancellation of capacitors C1a and C1b. Key waveforms are shown in Fig. 2.12

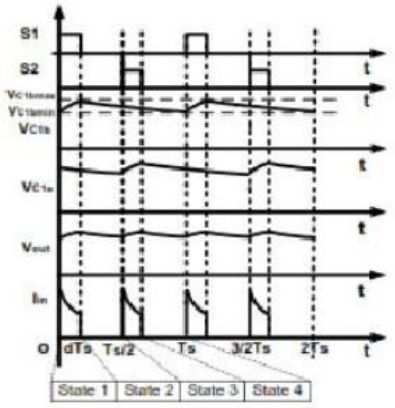


Figure 2.12 Output Waveform

Input current spike analysis:

the input current can be expressed as:

$$I_{in}(t) = \frac{V_{in} - V_{c1bmin} - V_d}{2R_{on} + r_d + r} e^{-\frac{t}{2R_{on}+r+r_d}} + I_{out}$$

Therefore, the input spike can be derived based on

$$I_{spike} = -\frac{V_d}{R} + \left(\frac{T_s}{RC}\frac{1}{1-e^{-\frac{dT_s}{RC}}} + 1\right)\frac{V_{out}}{R_L}$$

It can be seen that the input current spike is dependent on switching frequency, loop resistance
(Ron, ESR, Rd), flying capacitance and load.

Output ripples analysis:

For 3X TBSC, the output voltage ripple is determined by the voltage ripple of capacitor C2a and C2b, who have the same ripple cancelation mechanism as 2X TBSC. The output ripple magnitude is the same as describe in equation (2.30). Therefore, full ripple cancelation is also
achieved at duty cycle of 0.5 for 3X TBSC.

CIRCUIT PARAMETER ANALYSIS:

In order to investigate the influence of control parameters and circuit parameters, the voltage gain as function of C, R, f, d, are plotted in Fig. 13, based on formula (17). Their default values are shown as Table III. Fig. 2.21(a) indicates larger capacitance leads to higher voltage gain and higher efficiency as confirmed by many other papers. This is because large capacitance leads to smaller voltage difference between two interacting capacitors in each cycle and the efficiency of
power delivery between capacitors is determined by the voltage difference.

TABLE III
DEFAULT VALUES OF PARAMETERS

C(uF)	R(Ω)	fs(Hz)	d
100	0.15	10k	0.45

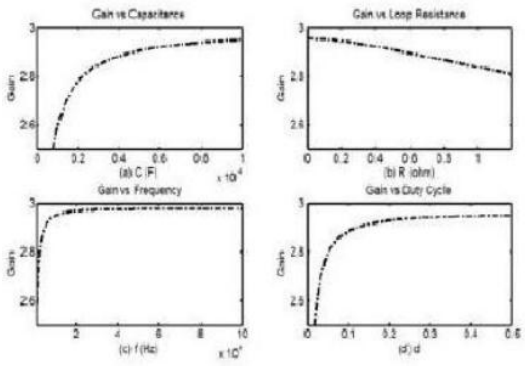


Figure.2.21. Parameters effect of voltage gain of 3 X TBSC converters

Fig. 2.21(b) reveals a larger loop resistance degrades the voltage gain, which means the efficiency will drop. This statement is under the condition when output voltage is not regulated. In reality, larger loop resistance will reduce the power deliver capability of circuit, thus the maximum gain will be limited. Therefore, maximum efficiency will be lowered. Fig. 2.21(c) shows that frequency can be used to regulate the output voltage because higher frequency leads to higher voltage gain. However, the frequency regulation is evident in low frequency range while in higher frequency range, the regulation curve tends to be flat based on the given condition of other parameters. Higher

frequency tends to result in higher voltage gain.

Therefore, increasing frequency can increase efficiency. This statement is made when ESL is not considered. Fig. 2.21(d) shows that duty cycle can be used to regulate the output voltage, known as PWM control strategy. The voltage gain will rise with the increase of duty cycle. When the output voltage is left unregulated, increasing the duty cycle will lead to higher system conversion efficiency. The introduced modelling method can be used for parameters trade-off. For other converters among the proposed step-up SC converter family, the voltage gain of nX TBSC converter can also be derived using similar modelling method. However, a general voltage gain

expression has not been derived. High order TBSC loop decoupling is much more complex, which is out the scope of in this paper.

SIMULATION CIRCUITS & RESULTS
MAIN CIRCUIT DIAGRAM:

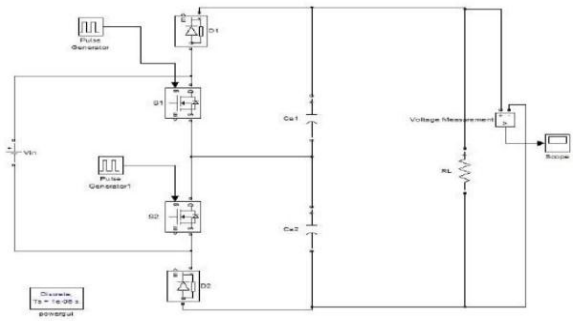


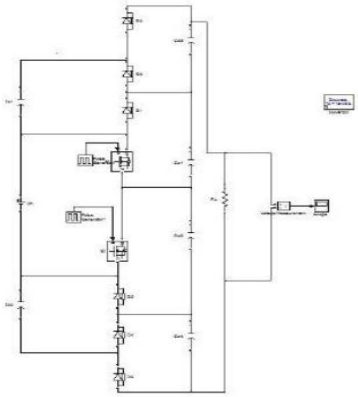
Fig 4.1 Main Circuit Diagram

The above figure shows the main circuit diagram as shown in above figure 4.1. In this figure the input voltage is taken into PV cell (i.e. Renewable energy source). The voltage measurement is connected across the output terminal of the PV array the main purpose voltage measurement hoe much of voltage is generated in PV cell.

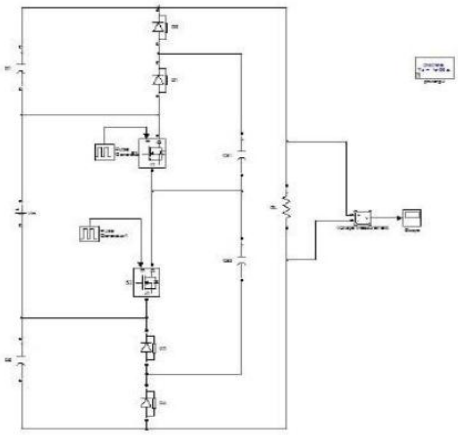
Same output voltage of PV cell is connected to the bridge network this bridge network will act as two half-cycles i.e. one for positive half cycle and another for negative half cycle. In positive half-cycle the upper side of converter will act into operation and in negative half-cycle the down side of the converter will act into operation. The main purpose of the IGBT is acting as a switch. The switch is operated depending upon the clock pulse. The clock pulse is generated within the Boost converter control (MPPT).

The inductor is connected in series to the IGBT and finally RL load is connected as shown in above fig 4.1

Sub Circuit-1:



Sub circuit-2:



CONCLUSION

A family of "Two-switch Boosting Switched capacitor Converters (TBSC)" is introduced, which distinguishes itself from the prior arts by symmetrically interleaved operation, reduced output ripple, low yet even voltage stress on components, and systematic expandability. Along with the topologies, a modeling method is formulated, which provokes the converter regulation method through duty cycle and frequency adjustment.

In addition, the paper also provides guidance for circuit components and parameter selection. A 1KW 3X TBSC was built to demonstrate the converter feasibility, regulation capability via duty cycle and frequency, which achieved a peak efficiency of 97.5% at the rated power.

REFERENCESS

[1] Bin Wu, Shouxiang Li **A Family of Two-Switch Boosting Switched-Capacitor converter,** *IEEE Trans.Power Electronics, Vol 28, no. 4 pp. 2014-2013 Apr.2016*

[2] W. Chen, A. Q. Huang, C. Li, G. Wang, and W. Gu, "Analysis **and comparison of medium voltage high power DC/DC converters for off- shore wind energy systems,"***IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 2014–2023, Apr. 2013.

[3]. J. A. Starzyk, "A **DC-DC charge pump design based on voltage doublers,"** *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.*, vol. 48, no. 3, pp. 350–359, Mar. 2001.

[4] F. L. Luo and H. Ye, "Positive **output multiple-lift push–pull switched-capacitor luo-converters,"** *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 594–602, Jun. 2004.

[5] N. Vazquez, L. Estrada, C. Hernandez, and E. Rodriguez, "The **tapped-inductor boost converter,"** in Proc. *IEEE Int. Symp. Ind. Electron.*, Jun. 2007, pp. 538–543.

[6] R. Wai, C. Lin, R. Duan, and Y. Chang, "High-efficiency **DC-DC con- verter with high voltage gain and reduced switch**

stress," *IEEE Trans. Ind.Electron.*, vol. 54, no. 1, pp.
354–364, Feb. 2007.

[7] J. Lee, T. Liang, and J. Chen, "Isolated **coupled-inductor-integrated DC– DC converter with nondissipative snubber for solar energy applications,"** *IEEE Trans. Ind.*
Electron., vol. 61, no. 7, pp. 3337–3348, Jul. 2014.

[8] M. Delshad and H. Farzanehfard, "High **step-up zero-voltage switch- ing currentfed**
isolated pulse width modulation DC–DC converter," *IET Power Electron.*, vol. 4, no. 3, pp. 316–322, Mar. 2011.

[9] A. Lamantia, P. G. Maranesi, and L. Radrizzani, "Small-signal **model of the Cockcroft-Walton voltage multiplier,"** *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 18–
25, Jan. 1994.

[10] P. Lin and L. Chua, "Topological **generation and analysis of voltage multiplier circuits,"** *IEEE Trans. Circuits Syst.*, vol. 24, no. 10, pp. 517–530, Oct. 1977.