Nano-electronics

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Abstract –

This paper emphasize on nano-electronics and reviews the current progress made in research in the areas of technologies, architectures, fault tolerance, and software tools. ano-electronics (circuits built with components on the scale of 10nm) seem to be the most promising successor to lithographic based ICs. Molecular scale devices including diodes, bistable switches, carbon nanotubes, and nanowires have been fabricated and characterized in chemistry labs. Techniques for self-assembling these devices into different architectures have also been demonstrated in this paper and used to build small scale prototypes. While these devices and assembly techniques will lead to nanoscale electronics, they also have the drawback of being prone to defects and transient faults. Fault tolerance techniques will be crucial to the use of nano-electronics. Finally, changes to the software tools that support the fabrication and use of ICs will be needed to extend them to support nano-electronics.

Keywords – Lithographic, fault tolerance, fabrication, CNT (Carbon Nano Tubes) .

1. Introduction

In 1975 Gordon Moore, cofounder of Intel, predicted that the number of transistors that could be placed on a chip would double every two years [Moore65]. Chip manufacturers have relied on the continued scaling down of the transistor size to achieve the exponential growth in transistor counts, but the scaling will soon end. Three obstacles stand in the way: the rising costs of fabrication, the limits of lithography, and the size of the transistor.

Process scaling is fundamental to most of the benefits achieved by modern electronics. For some applications, scaling allows for more devices to be integrated on a single die, and thus provide greater functionality per chip. Scaling also allows the same circuit to be smaller, cheaper, faster, and consume less power, thus driving new applications such as the cheap mobile electronics we now take for granted. Unfortunately, the scaling down of lithographically patterned transistors cannot continue forever, but nano-electronics may be able to continue the scaling when transistors hit their limit [1]. Before we discuss nano-electronics, we first cover the structure and operation of MOSFETs, the building block of modern digital electronics. This will provide the necessary background to understand the

issues that complicate the continued scaling of MOSFETs and provide a contrast to the nano- devices that will be surveyed later in this paper.

1.1 MOSFET Basics

MOSFET showing gate (G), body (B), source (S) and drain (D) terminals. The gate is separated from the body by an insulating layer (white). Two power MOSFETs in the surface-mount package D2PAK. Operating as switches, each of these components can sustain a blocking voltage of 120 volts in the OFF state, and can conduct a continuous current of 30 amperes in the ON state, dissipating up to about 100 watts and controlling a load of over 2000 watts. A matchstick is pictured for scale. A cross section through an nMOSFET when the gate voltage VGS [2] is below the threshold for making a conductive channel; there is little or no conduction between the terminals drain and source; the switch is off. When the gate is more positive, it attracts electrons, inducing an n-type conductive channel in the substrate below the oxide, which allows electrons to flow between the n-doped terminals; the switch is on. Simulation result for formation of inversion channel (electron density) and attainment of threshold voltage (IV) in a nanowire MOSFET.

The operation of a p-type MOSFET (where the drain and source are p-type semiconductors and the channel is n-type) is illustrated in Figure 2. Figure 2a shows a MOSFET in the "off" state, where no current it present in the channel. With no voltage potential across the gate and bulk, a depletion region forms around the drain and source blocking any current flow. A depletion region forms at a p-n junction when holes from the p-type material (source and drain in Figure 2) and electrons from the n-type material (channel in Figure 2) combine around the interface to create a region void of any free carriers. As the gate voltage drops, the electrons in the bulk are "pushed" away from the gate. When the voltage drops enough (beyond the threshold voltage), and enough electrons have left, the region just below the gate inverts to become p-type material (more holes than free electrons). There is now a continuous band of p-type material from the source to drain. This, along with an electric field set up from source to drain, causes electrons to move from hole to hole, creating a current .

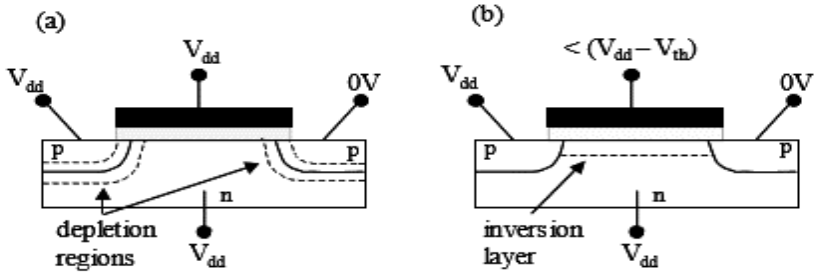

Figure 2: Illustration of the operation of a p-type MOSFET. (a) With no potential difference between the gate and bulk, a depletion region forms around the source and drain blocking current flow. (b) When the gate voltage drops a threshold voltage (V_{th}) below V_{dd}, the bulk just below the gate inverts to p-type, allowing current flow from the source to drain.

1.2 Nano-electronics

The phenomenal growth in the CMOS technology over the past four decades has enabled very high performance computing and storage systems, powering the information technology revolution. The MOS transistor has meta-morphed from a few 10s of micron dimension in 1970s to a few 10s of nanometer today. Semiconductor memory and high performance logic circuits have been the technology drivers to architect the miniaturization of the MOS transistor and this will continue in the foreseeable future. The underlying premise of this growth is the ability to miniaturize the MOS transistor dimension by 30%, in every two year cycle on an average [3]. The scaling of MOS transistor in Nanoelectronics era, necessitates the exploration of new materials (high-k gate dielectrics such as HfO2, Er2O3, Gd2O3; new channel materials such as Germanium, III-V and Graphene) and new device structures (Double gate FET, FinFET, Schottky source/drain FET). The facilities available at the centre provide an opportunity to carry out both experimental research and design and modelling research for Nanoelectronics devices. There are several groups in the Institute, working on various aspects of synthesis of new materials, processing techniques, device structures, modelling and simulation. Some recent highlights from the centre are summarized below. This is just a representative sampling, and not an exhaustive list of topics.

2. Technologies

The fundamental element of any nano-electronic circuit is the devices used to build it. For current VLSI systems these include silicon transistors and copper wires. For nano-electronics, it appears that the copper wires will be replaced by either carbon nanotubes (CNT) or silicon nanowires (SNW). The move to CNT or SNW [4] is because they can be chemically assembled at much smaller sizes than copper wires can be patterned with lithography. There are a number of technologies that could replace the transistor as the basic logic device, these include negative differential resistors, nanowire or carbon nanotube transistors, quantum cellular automata, and reconfigurable switches. These devices offer sizes of a few nanometers, can be self-assembled.

2.1 Carbon Nanotubes

Carbon nanotubes (**CNTs**) are allotropes of carbon with a cylindrical nanostructure (in figure 2) . Nanotubes have been constructed with length-to-diameter ratio of up to 132,000,000:1, [5] significantly larger than for any other material. These cylindrical carbon molecules have unusual properties, which are valuable for nanotechnology, electronics, optics and other fields of materials science and technology. In particular, owing to their extraordinary thermal conductivity and mechanical and electrical properties, carbon nanotubes find applications as additives to various structural materials. For instance, nanotubes form a tiny portion of the material(s) in some (primarily carbon fiber) baseball bats, golf clubs, or car parts.[6]

Nanotubes are members of the fullerene structural family. Their name is derived from their long, hollow structure with the walls formed by one-atom-thick sheets of

carbon, called graphene. These sheets are rolled at specific and discrete ("chiral") angles [7], and the combination of the rolling angle and radius decides the nanotube properties; for example, whether the individual nanotube shell is a metal or semiconductor. Nanotubes are categorized as single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs). Individual nanotubes naturally align themselves into "ropes" held together by van der Waals forces, more specifically, pi-stacking.

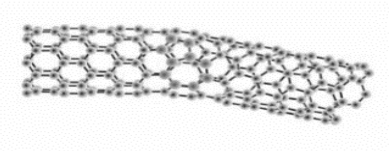

Figure 2: Illustrations of a single wall carbon nanotube.

2.2 Semiconducting Nanowires

Semiconducting nanowires (NWs), like CNTs, can be used as interconnect wires (shown in figure 3) to carry signals as well as be used as an active device. While one CNT is either an active device or a wire, a single NW can be both an active devices and an interconnect wire. NWs are long thin wires made up of semiconducting materials, such as silicon or germanium that have been fabricated with a diameter as small as 3nm[Cui01a, Morales98] and a length of up to hundreds of micrometers [Wu00]. The diameter is about eight times smaller than lithographic-based fabrication methods will likely ever be able to achieve.

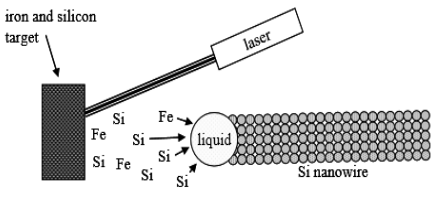

Figure 3: A proposed silicon nanowire growth method. Laser ablation is used to vaporize an iron and silicon target. The hot vapor condenses in a liquid catalyst, and the temperature is kept such that the iron/silicon seed remains liquid. The silicon nanowire grows as the catalyst absorbs more silicon and becomes saturated. [Morales98]

Molecular Devices Even though NWs and CNTs can be used as active devices as well as wires in nano- electronics, there is also a set of molecules that could be used as the active devices. These molecules behave as diodes or programmable switches that can make up the programmable connections between wires. Chemists have designed these carbon-based molecules to have electrical properties similar to their solid-state counterparts. Molecular devices have one huge advantage over solid-state devices: their size. Thousands of molecules can be sandwiched between two crossing micro-scale wires to create an active device that takes up very little area. Current VLSI crosspoints made of pass transistors are 40-100 times larger than a wire crossing or via [Butts02]. Since molecular devices fit between the wires, large area savings could be achieved. For example, it has been estimated that the use of nanowires and molecular switches could reduce the area of an FPGA by 70% over a traditional SRAM [8] based design at a 22nm process [Gayasen05]. In addition to being very small, molecular devices tend to be non-volatile: the configuration of the molecules remains stable in the absence of electrical stimulation. In the presence of electrical stimulation, programmable molecular device can be turned “on” and “off”, which can be used to perform logic.

3.1 Fault Tolerance

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of (or one or more faults within) some of its components. If its operating quality decreases at all, the decrease is proportional to the severity of the failure, as compared to a naïvely designed system in which even a small

failure can cause total breakdown. Fault tolerance is particularly sought after in high-availability or life-critical systems.

A **fault-tolerant design** enables a system to continue its intended operation, possibly at a reduced level, rather than failing completely, when some part of the system fails. The term is most commonly used to describe computer systems designed to continue more or less fully operational with, perhaps, a reduction in throughput or an increase in response time in the event of some partial failure. That is, the system as a whole is not stopped due to problems either in the hardware or the software. An example in another field is a motor vehicle designed so it will continue to be drivable if one of the tires is punctured. A structure is able to retain its integrity in the presence of damage due to causes such as fatigue, corrosion, manufacturing flaws, or impact. Fault tolerance is not just a property of individual machines; it may also characterise the rules by which they interact. For example, the Transmission Control Protocol (TCP) is designed to allow reliable two-way communication in a packet-switched network, even in the presence of communications links which are imperfect or overloaded. It does this by requiring the endpoints of the communication to *expect* packet loss, duplication, reordering and corruption, so that these conditions do not damage data integrity, and only reduce throughput by a proportional amount.

Recovery from errors in fault-tolerant systems can be characterised as either **roll-forward** or **roll-back**. When the system detects that it has made an error, roll-forward recovery takes the system state at that time and corrects it, to be able to move forward. Roll-back recovery reverts the system state back to some earlier, correct version, for example using check pointing, and moves forward from there. Roll-back recovery requires that the operations between the checkpoint and the detected erroneous state can be made idempotent. Some systems make use of both roll-forward and roll-back recovery for different errors or different parts of one error.

Within the scope of an *individual* system, fault tolerance can be achieved by anticipating exceptional conditions and building the system to cope with them, and, in general, aiming for self-stabilization so that the system converges towards an error-free state. However, if the consequences of a system failure are catastrophic, or the cost of making it sufficiently reliable is very high, a better solution may be to use some form of duplication. In any case, if the consequence of a system failure is so catastrophic, the system must be able to use reversion to fall back to a safe mode. This is similar to roll-back recovery but can be a human action if humans are present in the loop.

3.2 Run time fault tolerance

There are some fault tolerance techniques that can handle both defects and transient faults. This is accomplished mostly through hardware redundancy. This approach means that defects are characterized on a statistical level instead of specifically mapped. In other words, for a given technique, it is known that a given percentage of faults can be mitigated whenever they may occur. In the 1950's computers were unreliable in large part because the valves that made up the switches were prone to burning out. This prompted John von Neumann [9] to study the task of building reliable computers with unreliable components [von Neumann 56]. Specifically, von Neumann developed two hardware redundancy schemes, NMR and multiplexing, to achieve reliability. With the invention of the silicon transistor and

the subsequent advances in manufacturing, these two techniques were somewhat forgotten. However, they are still used in very critical hardware that cannot afford an upset due to radiation or some other random event. Now that it is evident that nanotechnology will also be unreliable, these ideas have received renewed interest.

3.3 Inherently fault tolerant architectures

Some proposed architectures are inherently fault tolerant because of the manner in which they are configured. Nanocells (section 3.2) use a genetic algorithm to "train" cells to perform a certain function [Husband03, Tour03]. By using a genetic algorithm to create the configuration stream on the actual hardware, any defects are avoided. This is very similar to reconfiguration, but the faults are not mapped. It is also less susceptible to transient faults because the output of a cell is determined by a current ratio. This means that if a switch malfunctions, it may not change the output current enough to change the output logic state

4. Software tools

A transition to nano-electronics will require modifications and additions to current computer aided design (CAD) flows to accommodate the unique properties of nano-electronics . CAD software tools for integrated circuits have been the subject of intense research for many years. These tools leverage the power of computers to assist circuit designers in implementing a circuit. The level of assistance can vary from completely implementing a circuit from a high-level language description to merely providing a GUI for implementing a circuit by hand [10]. CAD tools are becoming more important as designs increase in size and complexity. The number of devices and presence of defects expected in nano-electronics will only increase their importance. While many parts of current FPGA CAD flows can be directly migrated to tools for nanotechnology, there are unique challenges that will require additions and changes to the current tools. Before we discuss the unique challenges of CAD for nano-electronics, the traditional FPGA flow will be discussed (in figure 4)to give an indication of what parts will be migrated and what needs to be added.

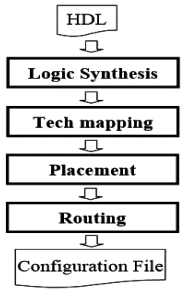

Figure 4. CAD flow for FPGAs.

A CAD tool's primary goal is to create the most efficient implementation of a design within the constraints of the target technology. Thus, the steps shown in Figure 34 are largely dependent on that technology. FPGAs represent a premade chip technology, where a flexible chip architecture is programmed to implement a user's design. This is similar to how nano-electronics are expected to be used.

6. Conclusion

The invention of the transistor in 1947 is one of the most important inventions [11] of the 20th century. Since its inception, the transistor has been reduced so that now modern devices are orders of magnitude smaller than their earliest counterparts. Unfortunately, the scaling down must eventually end. Increasing power, capital costs, and ultimately theoretical size

limitations, are poised to halt the process of continually shrinking the transistor. Nano-electronics show promise as a technology to continue the miniaturization of ICs. However, whether nano-electronics will be a replacement for conventional ICs, or as a complimentary technology, is yet to be determined. What has already been shown is that components such as wires and molecular switches can be fabricated and integrated into architectures. It is also known that these devices will be prone to defects and that fault tolerance schemes will be an integral part of any architecture. Finally, the preliminary research indicates that while existing parts of the CAD tools will be useful for nano-electronics, there will need to be some additions and changes made.

The greatest progress has been made in the research of the components that may make up nano-electronics. Chemists have been able to fabricate molecules that have two states, such that the molecules can be switched "on" and "off". Some of these molecules have shown the functionality of diodes or variable resistors. Chemists have also been able to fabricate silicon nanowires and carbon nanotubes. Both of these technologies can be used as wires or devices, and in some cases both. Nanoimprint lithography, probably the most promising wire fabrication technique, has been used to produce working memories on the nanometer scale. While all of these devices have been demonstrated, more lot of research is required to reliably produce these devices, and to create better devices.

One of the big questions for the future nano-electronics is whether nano-scale devices can be reliably assembled into architectures. Some small-scale successes have been achieved, but the benefit of nano-electronics is the enormous integration levels they may be able to achieve. The most promising architectures to date are array based. This is because arrays have a regular structure which is easier to build with self-assembly. Arrays also make good use of the available devices (nanowires, carbon nanotubes, and molecular electronics), and they are easy to configure in the presence of defects. There are other more random architectures that would require even less stringent fabrication techniques, but there is some doubt about how they will scale to larger systems. Overall, it is difficult to evaluate architectures as the underlying components are not fully understood nor developed yet. One thing that seems clear is that nano-electronics will, at least for the first few generations, need the support of conventional lithography based electronics for things such as I/O, fault tolerance, and even simple signal restoration.

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